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Smart Electrical Screening Methodology for Channel Hole Defects of 3D Vertical NAND (VNAND) Flash Memory

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Abstract: In order to successfully achieve mass production in NAND flash memory, a novel test procedure has been proposed to electrically detect and screen the channel hole defects, such as Not-Open, Bowing, and Bending, which are unique in high-density 3D NAND flash memory. Since channel hole defects lead to catastrophic failure (i.e., malfunction of basic NAND operations), detecting and screening defects in advance is one of the key challenges of guaranteeing the quality of flash products in the NAND manufacturing process. Based on analysis of the physical and electrical mechanisms of the channel hole defect, we have developed a two-step test procedure that consists of pattern-based and stress-based screen methodologies. By optimizing test patterns depending on the type of defect, the pattern-based screen is effective for detecting the type of `Hard` channel hole defects. The stress-based screen is carefully implemented to detect hidden `Soft` channel hole defects without degrading the reliability of NAND flash memory. In addition, we have attempted to further optimize the current version of our technique to minimize test time overhead, thus enabling 72.2% improvement in total test time. Experimental results using real 160 3D NAND flash chips show that our technique can efficiently detect and screen out various types of channel hole defects with minimum test time and negligible degradation in the flash reliability.

Keywords: 3D NAND flash memory; test methodology; screen; channel hole; defect; mass production; quality control

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1. Introduction

NAND flash memory has played an important role in realizing various innovative digital products such as digital cameras, smart-phones, and ultra-high-capacity SSDs [1,2]. Especially since the late 2000's, 3D vertical-NAND (VNAND) flash memory [3–6] has been a key technology for sustaining a continuous capacity growth in flash-based storage systems by overcoming various technical challenges in scaling 2D NAND flash memory [7,8]. For example, 2D NAND flash memory technologies had encountered the fundamental limits to scale below the 10 nm process technology [6] because of the low device reliability (due to severe cell-to-cell interference and the reduced number of stored charges in a flash cell (a flash cell is the basic unit that stores charge, i.e., bit information)) and high manufacturing complexity (e.g., EUV lithography equipment). However, by increasing the number of vertical stack layers, 3D VNAND flash memory has successfully contributed to sustaining the 50% per year growth rate in the NAND flash capacity [9], which established flash-based storage systems as de facto standards from mobile systems to high-performance enterprise environments.

Although 3D process technology successfully enabled us to break through the scaling-down limit of conventional 2D planar NAND flash memory, 3D VNAND flash memory has encountered new challenges due to its unique 3D architecture and new flash cell structure [10–19]. For example, due to the three-dimensional (like cubic structure) block

organization of the 3D VNAND device, there is a strong variability in electrical characteristics between flash cells depending on their vertical locations within a block,which was not shown in 2D planar NAND device [10–12,14,16]. (In NAND flash memory, a *page* is the unit of read and write operations, and hundreds of pages (e.g., 576 pages [20]) compose a *block*, the unit of erase operations.) Furthermore, most commercial 3D VNAND flash memories adopt cylindrical charge trap (CT)-type cell structures (e.g., TCAT [5], p-BICs [21] and SMArT [22]). The 2D planar NAND flash memory stores charges in a conductor called *the floating gate*, whereas the 3D VNAND flash memory stores bit information in a non-conductive (i.e., dielectric) layer within a CT-type cell called the *SiN trap layer*. The different cell structure of 3D VNAND flash memory causes new reliability issues such as early charge loss [15,17,18] or lateral charge spreading [13,14,19], which did not need to be considered in 2D planar NAND flash memory (more details are described in Section 2).

Although many researchers have attempted to improve the performance or reliability of the 3D NAND device based on the understanding of its electrical and physical characteristics, there are few studies to optimize the manufacturing process for the successful mass production of this new device. As explained before, since the overall organization and basic cell structure of 3D NAND flash memory are considerably different from those of 2D NAND flash memory, its failure mechanisms are also quite different from those of the 2D planar device. For example, the process of stacking layers can introduce a variety of new failure sources along the vertical direction. Moreover, the vertical etching process can cause severe attacks on flash cells, which is fatal to the quality of flash memory. Therefore, to efficiently guarantee the quality of 3D NAND flash memory with a high yield and low cost, it is necessary to revisit the test methodology suitable for the new 3D VNAND device.

Unlike the existing 2D planar device, each flash cell in the 3D VNAND device is serially connected along the "`channel hole`" manufactured using a *vertically successive* etching process from the topmost layer to the bottom layer. The channel hole acts as a substrate of a 2D planar flash cell, and forming channel holes is the most critical process in determining not only various characteristics (such as reliability, performance, and quality) but also the manufacturing yield of 3D NAND flash memory. For example, if we fail to form the uniform channel hole, flash memory will not work correctly as a memory device or will die (i.e., it will be a bad or failed chip) within a short time. However, since forming channel holes requires a highly complex process, it is a great challenge to achieve a uniform channel hole profile in trillions of channel holes within a 3D VNAND flash chip. Furthermore, as the number of vertically stacked layers increases (i.e., the vertical height of 3D flash memory becomes higher to increase flash capacity), forming the channel hole becomes more complex and challenging due to its high aspect ratio [23]. Hence, in a high-capacity 3D flash chip, there can be a large number of new failures resulting from various abnormal profiles in channel holes during NAND flash memory manufacturing (we collectively call these failures *channel hole defects*).

In this paper, we propose novel test approaches to efficiently screen out new failures in 3D NAND flash memory, focusing on different channel hole defects resulting from abnormalities in the channel hole profile. We classified the channel hole defects into four types depending on the abnormal shape in the channel hole profile: `not-open`, `bowing`, `tilting`, and `bending`. For each channel hole defect, we derived failure mechanisms based on electrical and physical analysis. In addition, we attempted to electrically screen out the channel hole defects by designing test methodologies (e.g., inventing new test patterns or setting efficient stress conditions). To validate the effectiveness of our proposed techniques, we conducted comprehensive experiments using 320 real 3D flash chips. Experimental results show that our new techniques can efficiently detect and screen out channel hole defects in 3D NAND flash memory without unexpected side effects such as flash reliability or performance degradation.

The rest of this paper is organized as follows. Before our techniques are presented, we review the organizational basics of 3D NAND flash memory and the manufacturing process in Section 2. In Section 3, we report our key findings for each channel hole abnormality. We

describe the proposed screening methodologies in Section 4. Experimental results follow in Section 5, and Section 6 concludes with a summary and future work.

2. Background

We provide a brief background on NAND flash memory and 3D vertical manufacturing processes necessary to understand the rest of the paper.

2.1. Basics of NAND Flash Memory

NAND Flash Organization

The NAND flash memory consists of flash cells, which store data, and peripheral circuits, which support flash commands such as read, write, and erase. Flash cells are grouped into a page, and multiple pages form a block. Figure 1 illustrates a typical flash block organization (i.e., conventional 2D NAND device). There are n word lines (WLs) in this block, and each WL has m flash cells. The common WL_i signal from the row decoder module is shared by the flash cells on the same WL, and they are read or programmed together as a unit. A WL can store more than one page (up to four pages) depending on how many bits can fit into a single flash cell. All flash cells along the same column are connected in series to form a bit line (BL_i). BLs are shared by all of the blocks in a flash chip and connected to the page buffer module, which is used for off-chip data transfers through the data-in/out circuit. The source select line (SSL) and ground select line (GSL) of a block are also composed of two select transistors, one at the top and one at the bottom of a BL. We can activate the flash block for flash operations by supplying proper voltages on the gate of GSL and SSL transistors.

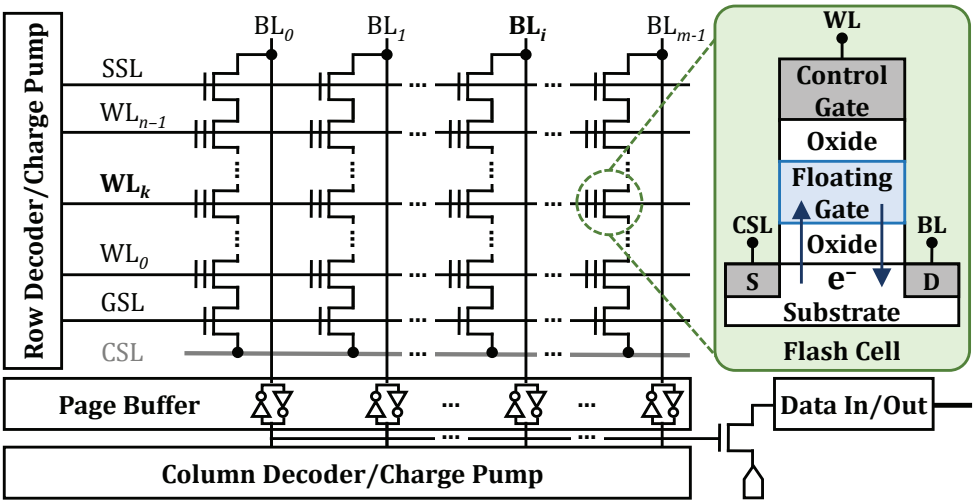


Figure 1. An overview of a conventional 2D NAND flash block.

Although the flash cell, shown in Figure 1, is structurally similar to a normal MOS transistor, it is unique in that it can adjust its threshold voltage V_{th} by injecting electrons into (or ejecting electrons from) the floating gate. Depending on the amount of electrons in the floating gate, therefore, the flash cell may work as an off switch or an on switch under a given control gate voltage, thus effectively storing bit data. For example, we can assign '0' state when the flash cell has a high V_{th} and '1' state when the flash cell has a low V_{th}.

NAND Flash Operation

NAND flash memory has three basic operations to act as non-volatile memory. The program operation, which increases V_{th} of selected flash cells, transfers electrons from the substrate into the floating gates of the selected flash cells using FN tunneling [24] by applying a high voltage (>20 V) to WL gates. On the other hand, to erase programmed cells, a high voltage (>20 V) is applied to the substrate (while WL gates are set to a low

voltage such as 0 V) to remove electrons from floating gates, which decreases the V_{th} of the flash cells. Since the program operation can only change the bit value of a flash cell from '1' to '0', all the flash cells of a page should be erased to program data on the page (*erase-before-program*). The erase operation works in a block granularity because the high voltage is applied to the entire substrate that underlies the flash blocks, enabling a high erase bandwidth.

In order to read the stored data from flash cells, the V_{th} level of the flash cells on the selected WL is probed by using a read reference voltage V_{ref}. In Figure 1, when WL_k is selected for read (since other WLs (e.g., WL_{k+1} or WL_{k-1}) should not affect the read operation of WL_k, all the flash cells in other WLs should behave like pass transistors, and therefore, their gate voltage is set to V_{READ} (>6 V) which is much higher than the highest V_{th} value of a flash cell), if V_{th} of the i-th flash cell in WL_k is higher than V_{ref}, the i-th flash cell turns off, so the cell current of BL_i is blocked (i.e., the flash cell is identified as '0'). On the other hand, if the V_{th} of the i-th flash cell is lower than V_{ref}, the i-th flash cell turns on, so the cell current can flow through BL_i (i.e., the flash cell is identified as '1'). By sensing BL_i's from the selected WL_k, the stored data are read out to the page buffer. Note that if we can prevent the page buffer from reading the data in a flash cell or inhibit the data in the page buffer from transferring out of the flash chip via a data-out path, its effect will be equivalent to destroying the stored page in the selected WL.

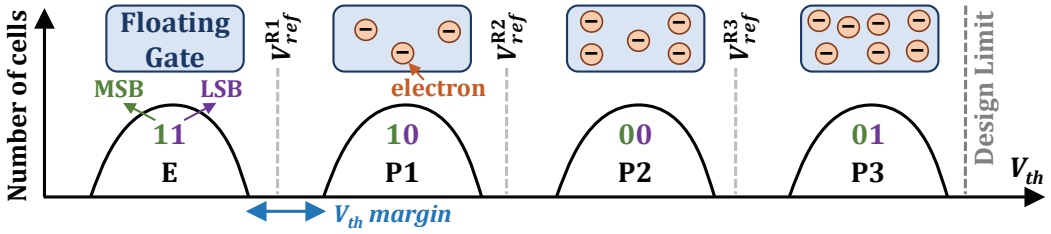
Multi-level Cell Flash Memory

In order to reduce the cost per bit value of flash memory, multi-leveling techniques are widely used. The multi-level cell (MLC) technology was initially developed for storing 2 bits per cell, but it was extended to support TLC (triple-level cell, 3 bits/cell) and QLC (quadruple-level cell, 4 bits/cell). Figure 2 illustrates V_{th} distributions for 2^m-state NAND flash memory, which stores m bits within a single flash cell by using 2^m distinct V_{th} states (i.e., m is 2 and 3 for MLC and TLC, respectively). As m is increased to store more bits within a flash cell, more V_{th} states should be put into the limited V_{th} window, which is fixed at the flash design time. Therefore, a more careful management is required for multi-level flash memory to form finer V_{th} states, as m increases. Furthermore, as m increases, a V_{th} margin (i.e., a gap between two neighboring V_{th} states) inevitably becomes narrower as shown in Figure 2a,b. When the V_{th} margin becomes smaller, two neighboring V_{th} states are more likely to be overlapped under various noise conditions, thus degrading the reliability of the NAND flash memory. For example, the MLC flash memory can tolerate up to 3000 program and erase (P/E) cycles, while the TLC flash memory can tolerate only 1000 P/E cycles. As a result, as m increases, many optimization techniques that were effective for smaller m become less effective or inapplicable because of the worsened flash reliability.

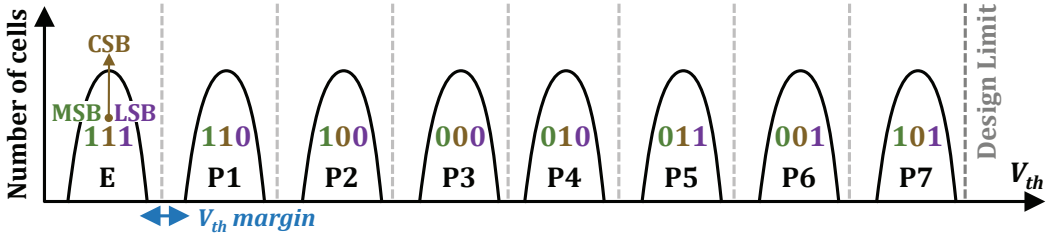
2.2. Organizational Basics of 3D Vertical Nand Flash Memory

Figure 3 illustrates an organizational difference in a NAND block between 2D NAND flash and 3D NAND flash memory. Although the architecture of 3D NAND flash memory is conceptually described as if multiple 2D NAND flash layers are stacked in a vertical direction [25], the inner organization of 3D NAND flash memory is quite different from this logical explanation. In the example shown in Figure 3, the 2D NAND flash memory has a *2D matrix* structure in which four WLs and three bitlines (BLs) intersect at 90 degrees. On the contrary, the 3D NAND flash memory has a *cube-like* structure. The 3D NAND flash block consists of four vertical layers (v-layers) on the y-axis, where each v-layer has four vertically stacked WLs separated by select-line (SSL) transistors. As shown in Figure 3, when the 2D NAND flash block is rotated by 90° in a counterclockwise direction using the x-axis as an axis of rotation (i.e., if the WLs are set vertically), it corresponds to a single v-layer. Similarly, the 3D NAND flash block can be described as having four horizontal layers (h-layers) stacked along the z-axis, and each horizontal layer consists of four WLs. In order to increase the capacity of a 3D flash chip, the most effective approach is to increase the number of h-layers in 3D NAND flash memory (i.e., stacking more h-layers along the z-axis). As the number of h-layers increases, the block size increases as well (the advanced

3D NAND flash memory has more than 200 layers, and the capacity of one flash chip reaches 1Tb [26]).



(**a**) m = 2: MLC flash memory.



(**b**) m = 3: TLC flash memory.

Figure 2. V_{th} distributions of 2^m-state multi-level cell NAND flash memory.

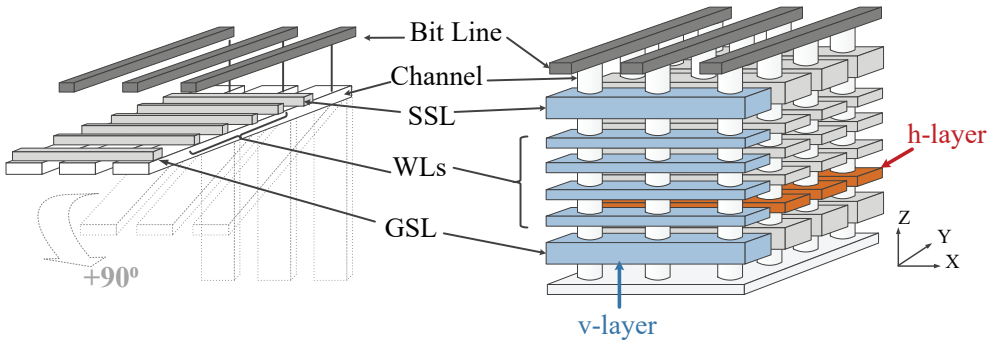


Figure 3. Illustration of organizational difference between 2D and 3D NAND flash memory.

To achieve a vertical architecture, the 3D NAND device employs a new revolutionary flash cell structure called charge trap (CT)-type flash cell. Figure 4 shows a flash cell in 3D NAND flash memory. Compared to the flash cell of 2D NAND flash memory shown in Figure 1, the most noticeable innovation is the switch from a floating gate (conductor) to a charge trap layer (non-conductive material) as the space for storing electric charges. The working principles of both cell types are relatively similar, but in a charge trap (CT)-type cell, the trap layer is an insulator (usually silicon nitride, SiN), significantly reducing the electrostatic interference between neighboring cells. (In 2D NAND flash memory, the scaling-down process for achieving a high-capacity NAND flash memory inevitably narrows the physical distance between flash cells, which considerably increases the cell-to-cell interference effect. Since the cell-to-cell interference causes additional bit errors by widening V_{th} distribution, it is one of the key factors limiting the continuous shrink in 2D NAND flash memory.) This charge trap cell is now the base of most commercial 3D NAND flash memory.

The channel is created by etching a hole through the stack layers and then forming the transistor structure with the deposition of three layers in order, such as tunnel oxide, charge trap layer (SiN layer), and blocking oxide. After that, the poly-silicon channel fills in the middle of the hole. Finally, the cell gates are constituted by the poly-silicon horizontal

layer (or metal-like composite of tungsten) surrounding the vertical channel forming a Gate-All-Around (GAA) structure, which looks like a macaroni structure.

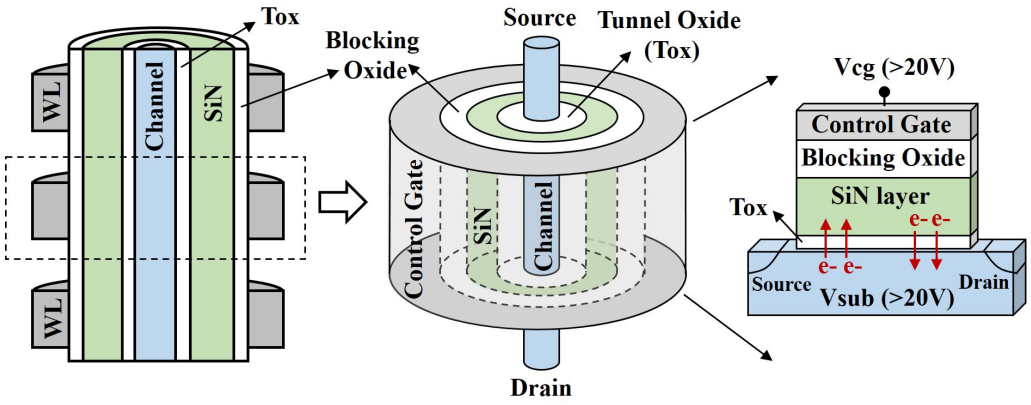


Figure 4. Schematic diagram of the flash cell of 3D NAND flash memory.

2.3. Three-Dimensional NAND Manufacturing Process

Figure 5 shows a detailed organization of a vertical layer in 3D NAND flash memory using a cross-sectional view (along the x-z plane) and a top-down view (of three cross sections along the x-y plane). The stacked cells are vertically connected through *cylindrical* channel holes. The channel holes are formed at the early stage of 3D NAND flash manufacturing by an etching process [5]. Since the dimension of the flash cells is greatly dependent on the structural shape of the underlying channel hole, the etching process is regarded as one of the most critical steps for manufacturing 3D NAND flash memory.

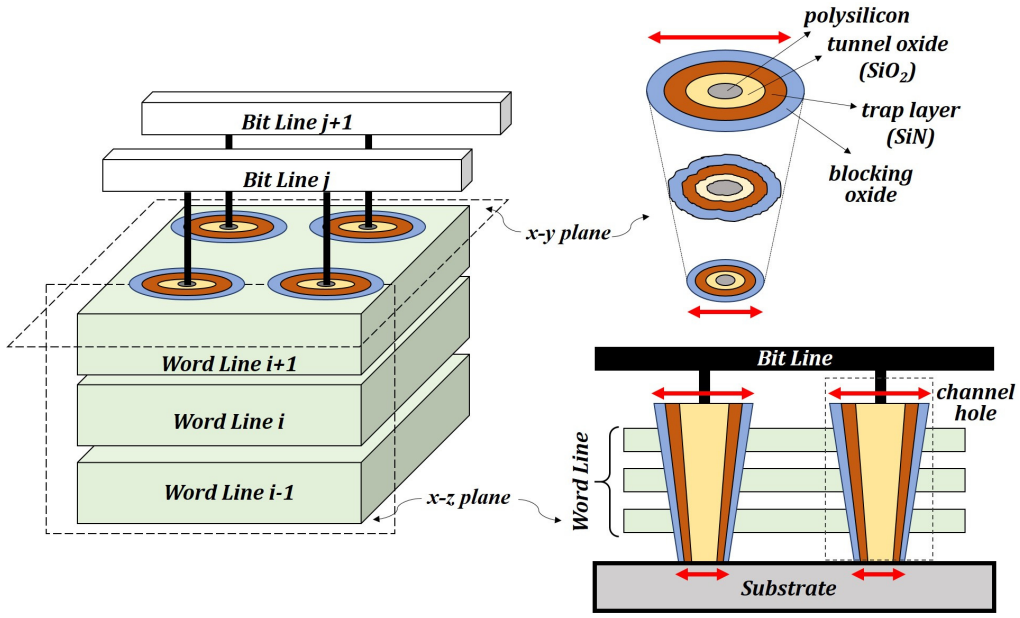


Figure 5. Schematic diagram of a 3D NAND flash cell and its operations.

Ideally, we expect that each channel hole has the same geometrical structure regardless of its physical location to achieve uniform characteristics between flash cells. However, while the etching process proceeds from the topmost layer to the bottom substrate, it introduces structural variations to channel holes depending on their vertical locations. For example, as shown in Figure 5, the diameter of the channel holes varies significantly depending on the vertical height. These unexpected phenomena are caused by a high *aspect ratio* (HAR) of the cylindrical channel hole. (The aspect ratio of a channel hole can

be defined as the ratio of width to height. In 64-layer 3D NAND flash memory, the aspect ratio of channel holes is expected to be more than 60:1.) During the etching process, the deeper the depth of the channel hole, the fewer etchant ions it reaches and the less chance of reaction for etching. Therefore, the channel hole diameter in the topmost layer is wider than that in the bottom layer (i.e., the flash cell in the topmost layer has a larger cell size than that in the bottom layer). Furthermore, the shape of channel holes in some layers is an ellipse or a rugged shape unlike the circle due to the variance of etchant fluid dynamics with a vertical position. These structural variations, in turn, cause significant differences in flash cells' characteristics.

The complex dynamics of the etching process can lead to more severe problems in high-capacity 3D NAND flash memory. As the number of stacked layers increases, the non-ideal process effect gets higher, resulting in a variety of abnormalities in the channel hole profile. The abnormal profile of channel holes not only causes unexpected malfunctions of the NAND device but also becomes the root cause of the high failure rate in flash-based storage systems. Therefore, in order to successfully accomplish mass productions with a high yield and quality, it is crucial to develop test methodologies that effectively detect and screen out the channel hole defects based on the precise analysis of the channel hole abnormalities.

3. Types of Channel Hole Defect

Before designing test methodologies for screening channel hole defects, we attempted to categorize different channel hole defects based on two criteria: (1) the types of abnormal profiles in the channel hole, and (2) whether abnormal channel hole profiles simply increase bit errors (i.e., degrade the flash reliability) or cause malfunctions (i.e., flash chip failure).

Figure 6 illustrates different abnormalities in the channel hole profile due to the non-ideal etching process during 3D NAND manufacturing. As described in Section 2, it is quite difficult (or mostly impossible) to form the channel hole as a right rectangular shape due to non-ideal effects (e.g., fluid dynamics of etchant) during the etching process. Even though various conditions in the etching process can be controlled carefully, the best result we can obtain is a reverse rhombus-shaped profile, denoted as *normal* in Figure 6a. In our study, compared to the normal profile, we define three different abnormalities in the channel hole profile: `Not-open`, `Bowing`, and `Bending`. Furthermore, depending on the degree of abnormality in the channel hole profile, channel hole defects are divided into two categories: `Soft` defects and `Hard` defects. Based on this classification, we will take type-oriented optimized approaches to detect and screen out channel hole defects.

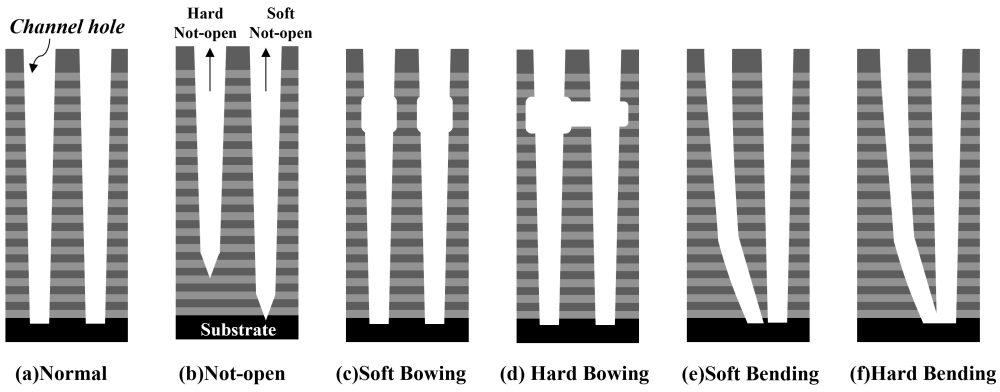


Figure 6. Schematic diagram of various abnormalities in the channel hole profile.

3.1. Channel Hole Not-Open

In 3D NAND flash memory, it is natural that the diameter of the channel hole becomes narrower as the layer goes down because both vertical and lateral etching rates are not uniform but vary depending on the vertical locations of stacked layers. Unfortunately, some channel holes cannot successfully reach the substrate during the etching process,

and we call this type of abnormality `Hard Not-Open`. As shown in the left channel hole of Figure 6b, the not-opened channel holes are not fully punched-through, so they fail to connect to the substrate physically. Because the not-opened channel holes are isolated from the substrate, the electrical voltage for NAND operations cannot be applied to flash cells in a block. Therefore, flash cells along the not-opened channel hole become electrically disabled, making it impossible to perform flash operations correctly. Since the `Hard Not-Open` defect causes malfunctions of the NAND device (i.e., we cannot complete the erase, program, or read operations.), it can be easily screened out by a simple test pattern during post-manufacturing testing procedures (more details in Section 4).

There can be another type of not-open abnormality. The right channel hole in Figure 6b shows another type of channel hole that is not open. In this case, the end of the channel hole succeeds in reaching the substrate. However, its connection is relatively weaker compared to the normal channel holes (i.e., the channel hole diameter of the bottom layer is much narrower than that of a normal channel hole), called `Soft Not-Open`. This type of channel hole works well at first and shows no difference from other normal channel holes in performing NAND operations. However, physically weak connections between the substrate and channel hole can be easily broken by even a small amount of electrical stress (i.e., repetitive program and erase operations, P/E cycles), which eventually leads to the `Hard Not-Open` channel hole defect. Compared to the `Hard Not-Open`, the `Soft Not-Open` channel hole defect in flash memory products causes more severe problems for two reasons. First, it cannot be detected by conventional standard test procedures, which consist of function checks based on various test patterns. Second, since it can be easily turned into device failure even when the user has utilized the flash product only for a short time, the initial quality of the flash product is considerably worsened (i.e., infant mortality failure is dramatically raised). Therefore, it is crucial to apply different approaches to detect and screen out the `Hard Not-Open` and `Soft Not-Open` channel hole defects.

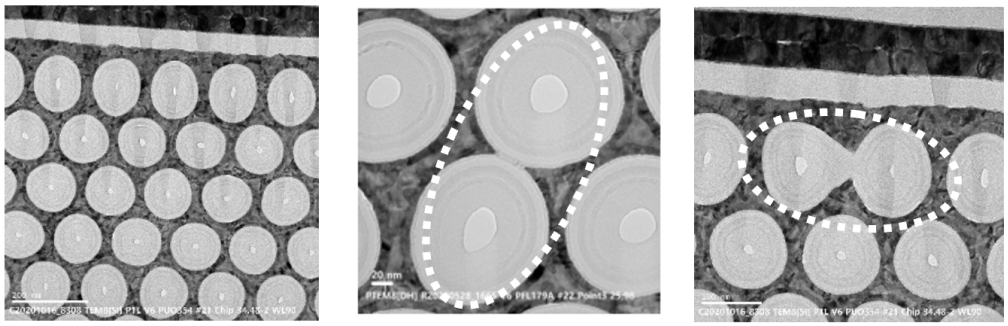
3.2. Channel Hole Bowing

`Bowing` is an abnormal profile resulting from the unexpected increase in the channel hole diameter in a particular vertical location. (Remember, the channel hole has a 3D cylindrical structure.) Figure 6c,d describe two types of bow defects: `Soft Bowing` and `Hard Bowing`. `Bowing` is generated when the non-ideal effects of the etching process are exacerbated in the specific stacked layers during channel hole formation, especially near the top layers. When the etching process starts to form channel holes, the lateral and vertical etching rates can be controlled precisely. However, as the etching process proceeds, it shows a relatively unstable state due to the complex fluid dynamics of the etchant, so the lateral etching rate near the topmost layer can unusually become higher than the vertical etching rate (i.e., the channel hole diameter of near the topmost layer is enlarged). Therefore, there is a high possibility that an unexpected shape in the channel hole can be created in the upper layers rather than the lower layers. (Note that the etching process proceeds from the topmost layer to the bottom layer.) Furthermore, an unstable etching process makes the shape of channel holes a rugged shape, unlike a uniform circle. As shown in Figures 4 and 5, since a channel hole can be seen as a physical barrier to the charge flow along WLs in h-layers, the fluctuations in the channel hole diameters can increase the parasitic resistance or capacitance, thus resulting in large variations in the error characteristics between different layers in a flash block.

When the degree of `Bowing` becomes more severe, neighboring channel holes become punched-through and connected, which is called `Hard Bowing`. As shown in Figure 4, the major components that make up the flash cell (e.g., tunnel oxide, SiN trap layer, blocking oxide, and metal gate) should be deposited in order along the cylindrical channel hole. Once `Hard Bowing` occurs, flash cells in the corresponding layers cannot avoid an abnormal or incomplete structure, which prevents NAND operations from working properly.

3.3. Channel Hole Bending

`Bending` can be generated when uncontrolled differences in the chemical composition or density of a specific stacked layer impose unusual effects on the fluid dynamics of the etchant, resulting in unexpected changes in the vertical etching direction. As a result, the bottom region of two adjacent channel holes can get closer to each other or, in the worst case, can be attached together. Figure 6e,f show two types of channel hole `Bending` defects: `Soft Bending` and `Hard Bending`. Similar to `Bowing`, `Soft Bending` leads to variations in flash cell geometry structure, which impacts the error characteristics of the flash cells. On the other hand, since `Hard Bending` prevents adjacent channel holes from physically or electrically separating, it can cause catastrophic failures in normal NAND operations. Figure 7 shows the transmission electron microscope (TEM) images of bending defects in the bottom region, showing the neighboring channel holes stuck together. TEM images show that `Bending` occurs not only between horizontally adjacent channel holes but also between diagonally adjacent channel holes.



(a) **(b)** **(c)**

Figure 7. (**a**) TEM images of normal channel hole. (**b**) TEM images of bending defect caused by diagonal line. (**c**) TEM images of bending defect caused by horizontal line.

4. Defect-Centric Screen Methodology

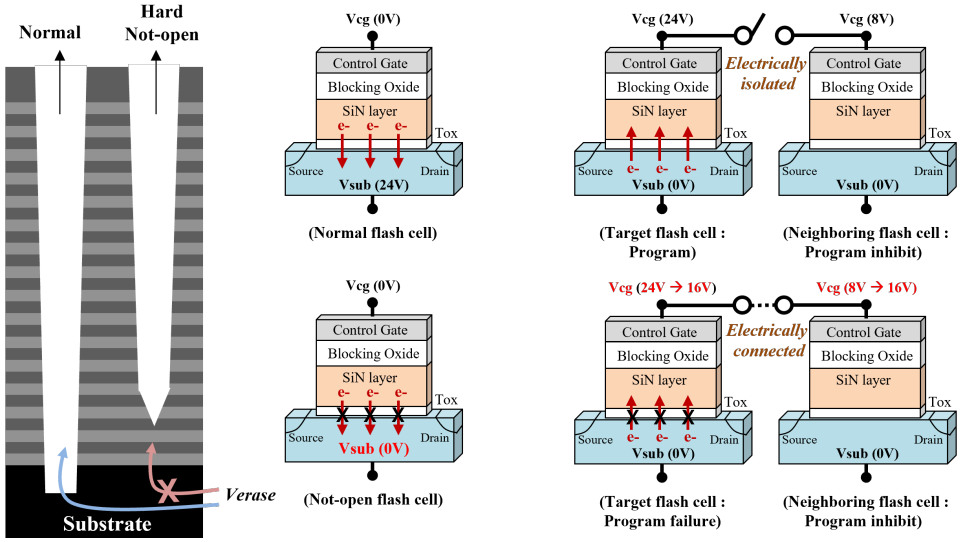
In this section, we introduce test methodologies to detect and screen out channel hole defects effectively. Our test methodology consists of two approaches, depending on the classification of the channel hole defects explained in Section 3. First, `Hard` channel hole defects can be electrically detected by a combination of function checks using various test patterns. (We call it *pattern-based screen methodology*). Second, `Soft` channel hole defects need a more sophisticated test procedure because these types of defects cannot be detected by a simple pattern-based screen methodology. In order to effectively reveal `Soft` channel hole defects, it is required to apply electrical stress to accelerate the shift of `Soft` defects into `Hard` defects. Once `Soft` defects are switched into `Hard` defects, they can be easily detected by a pattern-based screening methodology. (We call it *stress-based screen methodology*).

4.1. Pattern-Based Screen Methodology

Pattern-based screen methodology consists of a combination of NAND functions and target patterns. The most important thing in performing pattern-based evaluation is determining the optimal test pattern when performing basic NAND operations such as erase, program, and read. To effectively distinguish various channel hole defects, each test pattern should be carefully selected, considering the type of anomaly in the channel hole profile and the electrical mechanism by which the NAND operations are performed. For example, certain channel hole defects can be readily apparent in the erase pattern but can be hardly identified in the program pattern. Furthermore, among the possible candidates, it is necessary to choose the target test pattern with the highest detection probability and the least time required. In the following, we will try to derive which test pattern is optimal for individual channel hole defects based on an accurate understanding of the physical phenomena caused by channel hole anomalies.

Channel Hole Not-Open

The key phenomenon of the `Hard Not-Open` defect is that the substrate and the channel hole are physically and electrically separated. As explained in Section 2, to perform an erase operation, it is required to apply the high erase voltage (V_{ERS}) to the channel of the flash cell. V_{ERS} (more than 20 V) is transferred into the channel through the substrate, as shown in the left figure of Figure 8a. In the channel hole where the `Hard Not-Open` defect occurs, there is no path to deliver V_{ERS} to the target flash cells. Since there is no voltage difference between the WL gate (V_{cg}) and the channel substrate, electrons trapped in the SiN layer cannot be removed. Therefore, the `Hard Not-Open` defect results in the erase failure (i.e., the erase operation fails to complete within pre-defined time criteria called *Max. erase time*). We can easily check the erase failure during test procedures by monitoring the *status* pin implemented in a flash chip. If the state of the *status* pin turns to *"high (H)"* after an erase operation, the target flash block is regarded as an erase failure (i.e., having the `Hard Not-Open` defect), thus being imprinted as a *"Bad Block"*.



(a) Erase operation in Not-open flash cell **(b) Program operation in Bowing flash cell**

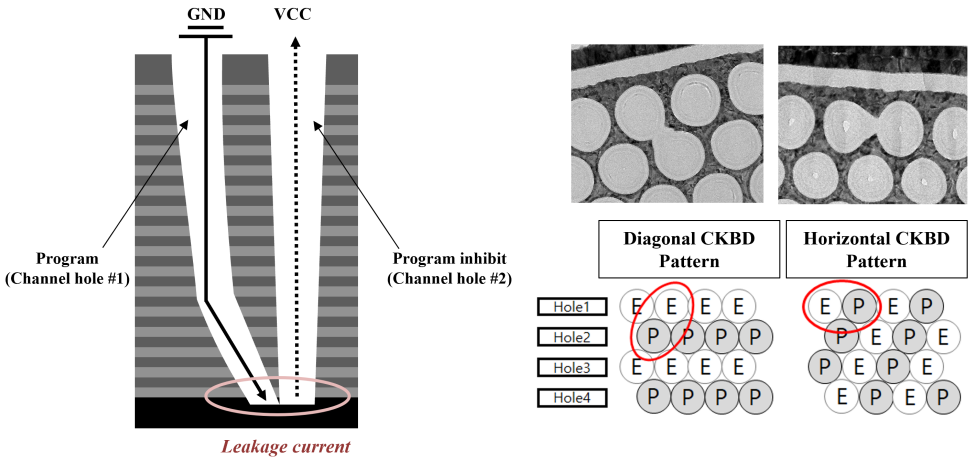
Figure 8. Different mechanism of NAND operations depending on the channel hole anomalies.

Channel Hole Bowing

Unlike the `Hard Not-Open` defect, the `Hard Bowing` defect can be effectively detected during a program operation because the `Hard Bowing` defect leads to an electrical connection between flash cells in a specific region of the channel hole. In a NAND program operation, the WL gate of the target flash cell is set to a high voltage (i.e., a large enough voltage difference to move electrons from the substrate to the SiN trap layer), so the target flash cell has a high V_{th} and '1' state. On the other hand, the WL gate of the neighboring non-target flash cell is set to a low voltage (i.e., a small voltage difference not to move electrons), V_{th} of the flash cell maintains a low V_{th} and '0' state (i.e., program inhibited). If two adjacent flash cells are attached due to `Hard Bowing` defect, the WL gates of two flash cells are electrically connected, and the voltage level of the target flash cell is lowered by the voltage sharing effect, resulting in program failure (i.e., the program operation fails to complete within pre-defined time criteria called *Max. program time*). The mechanism of program failure is illustrated in the left figure of Figure 8. Program failure can be also checked by monitoring the *status* pin in a flash chip. If the state of the *status* pin turns to *"high (H)"* after a program operation, the target flash block is regarded as a program failure (i.e., having the `Hard Bowing` defect), thus being imprinted as *"Bad Block"*.

Channel Hole Bending

The `Hard bending` channel hole defect originates when the bottoms of two adjacent channel holes are slightly stuck to each other. Similar to the `Hard Bowing` defect, the `Hard bending` defect can be detected using a program operation, but the test pattern should be modified due to its unique fail mechanism. Figure 9 shows the schematic of how to detect the `Hard bending` channel hole defect. As shown in Figure 9a, channel holes ♯1 and ♯2 are assumed to be programmed and inhibited, respectively. When a channel hole is close to the neighboring one (i.e., `Hard bending` defect occurs), a leakage current will be observed between the two channel holes. However, the amount of leakage current is too low to measure using a normal program operation. To boost the amount of leakage current, we maximized the potential difference between channel holes by applying a 3D checkerboard (CKBD) pattern [27]. Figure 9b shows the CKBD pattern in a diagonal and horizontal direction, respectively. ("P" indicates programmed ('0') states, and "I" indicates inhibited ('1') states). We used four different CKBD patterns to detect ChB defects: diagonal CKBD, reversible diagonal CKBD, horizontal CKBD, and reversible horizontal CKBD. (The reversible CKBD is a pattern in which the "P" and "I" of the original pattern are swapped.) Due to leakage current, the threshold voltage (V_{th}) of the program-inhibited flash cells (i.e., flash cells not to be programmed) in the bending channel hole increases compared to other normal channel holes. (The erased flash cells are not inhibited enough from being programmed, so they are partially programmed.) Therefore, after program operations with four 3D CKBD patterns, we can efficiently detect the `Hard bending` defect just by sensing the V_{th} of flash cells using the proper read level.



(a) Fail mechanism of Bending defect **(b) Different CKBD pattern for Bending defect**

Figure 9. Screening method and test pattern for Bending defect.

4.2. Stress-Based Screen Methodology

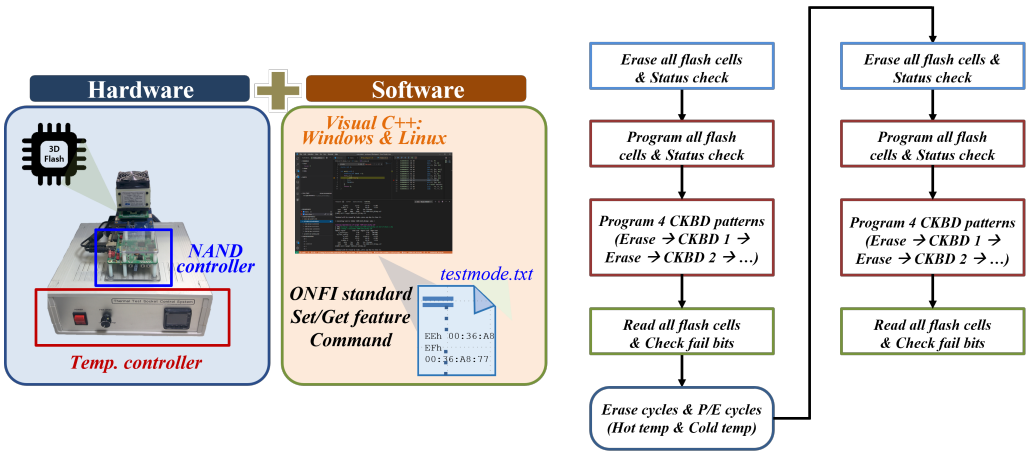
As explained in Section 3, the type of `Soft` channel hole defects cannot be screened out by a simple pattern-based screen methodology. In order to activate hidden defects, we introduced electrical stress (e.g., erase-only cycles or P/E cycles) before the function check step in our test procedure. (In industry, this type of test is usually called a *burn-in* test. Various burn-in tests have been widely used in the quality assessment and certification of various electronic devices [28]). Since we aim to screen out only infant mortality in the bath-tub curve [29], we should precisely control the stress conditions, such as voltages, timing, and the number of cycles. For example, under-stress conditions result in a long test time without accelerating `Soft` channel hole defects, thus eventually raising the cost of flash products. On the contrary, over-stress conditions inflict unnecessary damage to the flash cells, thus degrading the reliability or lifetime of flash products. Therefore, establishing the stress conditions is the most important factor in determining the effectiveness of the stress-based screen methodology.

5. Experimental Results

5.1. Experimental Settings

In order to verify the effectiveness of our proposed technique, data-centric screen methodology based on the combination of pattern-based and stress-based screen methodology, we have performed comprehensive evaluations using real 160 48-layer 3D TLC flash chips. (We also confirmed the effectiveness of our technique in 3D MLC flash chips and obtained similar evaluation results. Therefore, our technique can be extended to all types of 3D NAND flash memories, including advanced 3D QLC and xLC NAND flash memories.) To minimize the potential distortion of the evaluation results from process variations, we evenly selected 120 test blocks from each chip at different physical locations and tested a total of 11,520,000 pages (i.e., 3,840,000 WLs) in our evaluations. By using an in-house custom test board (equipped with a flash controller and a thermal controller), we performed various test scenarios and measured the reliability and performance of the test flash blocks. The test program was written in the programming language of Visual C++ on a Linux-based computing system. The test scenario comprised a mixture of NAND operations that have different patterns and modified internal operating conditions. Since flash memory vendors provide the low-level NAND flash memory interface function, we can access the current settings of internal NAND flash memory (including modifications of operating voltage) and check the current BER value of each WL after program operation (e.g., Set/Get-Features) [30]. In addition, the flash reliability was measured while varying the number of P/E cycles and the data retention time. A long-term lifetime test can be performed using an accelerated lifetime test. For example, to emulate a 12-month retention time condition, we baked the flash chips at 85 °C for 13 h, which is equivalent to 1 year at 30 °C by the Arrhenius's law [31].

All our test procedures follow the JEDEC standard, which is the common industry practice for flash products. The industrial JEDEC standards [32,33] specify the test methodology (e.g., a sample size or test conditions) and qualification criteria for evaluating NAND flash memory. To ensure the confidence of reliability tests, these standards recommend that more than 39 flash chips from three different wafers should be tested. Since we have used a total of 160 flash chips from five wafers for evaluations, we believe that our sample size is sufficient to obtain statistically meaningful results. Figure 10 shows test equipment and the overall test procedure. Remember that due to erase-before program constraints explained in Section 2, an erase operation should always proceed a program operation.



(a) Hardware/Software test infrastructure **(b) Overall test flow of proposed data-centric screen methodology**

Figure 10. Schematics of test infra and the overall test procedure.

In this section, to validate our proposed technique, we focus on three criteria: The first is how to accurately distinguish a channel hole defect compared to a normal channel

hole (i.e., *detection accuracy*). The second is whether the reliability and performance of flash cells are degraded during the test procedures (i.e., *side effects*). The last is whether the time required for the test can be tolerable for mass production (i.e., *test time overhead*).

5.2. Detection Accuracy Analysis

Channel Hole Not-Open

Figure 11 shows the experimental results for detecting channel hole `Not-Open` defects. This type of defect is detected by monitoring the state of the status pin after performing an erase operation to target flash blocks. When the state of the status pin is high (i.e., erase status fail), the target block is regarded as having `Not-Open` defects, thus being numbered as a bad block. Figure 11a shows how many bad blocks are generated after an erase operation while varying the erase voltage (V_{ERS}). The Y-axis denotes the distribution of bad blocks of our tested flash blocks. Even though V_{ERS} is raised from 20 V to 24 V, there is no significant change in detection accuracy. It means that the operating conditions for a single erase operation alone do not affect whether `Not-Open` defects are detected or not. To efficiently reveal the hidden `Soft Not-Open` defects, we re-count the number of bad blocks after performing erase cycle stress. As shown in Figure 11b, the more erase cycles, the more bad blocks occur. As the number of erase cycles increases, the joint region between the substrate and the channel hole suffers from electrical stress, so the `Soft Not-Open` defect can be efficiently switched into the `Hard Not-Open` defect that is easily detected by a simple function check. Figure 11c shows how our proposed technique can reduce the infant mortality of flash products due to channel hole `Not-Open` defects. In the case of 50 erase cycles, additional bad blocks are found even in the early stage of the flash lifetime. However, in the case of 200 erase cycles, no bad block was found up to 100 P/E cycles. (It is known that commercial TLC NAND flash memory can tolerate 1000 P/E cycles. In our study, 100 P/E cycles (i.e., 10% of a total lifetime) are regarded as the early stage of flash lifetime.) It indicates that the combination of erase cycles and erase function check is an effective solution to screen out hidden `Not-Open` defects.

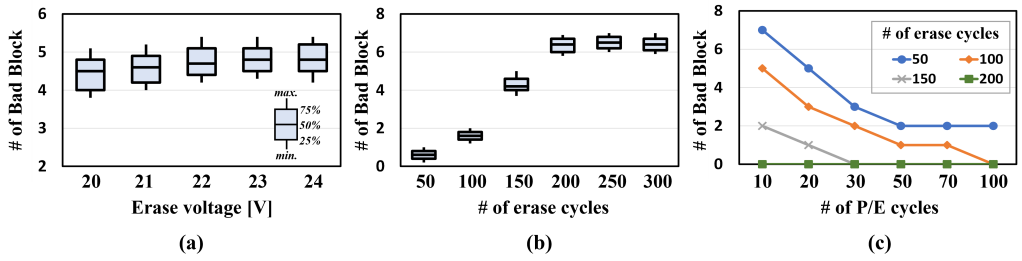


Figure 11. Experimental results for channel hole `Not-Open` defects. (**a**) Detection accuracy vs. erase voltage. (**b**) Detection accuracy vs. erase cycles. (**c**) Infant mortality in a flash chip.

Channel Hole Bowing

Figure 12 shows the experimental results for detecting channel hole `Bowing` defects. In the `Soft Bowing` case, it does not cause a chip failure but only affects the error characteristics in specific WL regions. As shown in Figure 12a, WL regions where `Bowing` occurs exhibit higher raw bit error rates (RBERs) compared to other WLs. A large and distorted channel hole shape due to `Bowing` makes flash cells in WLs more vulnerable to noise or stress, which gets more severe as P/E cycles increase. Therefore, managing error-prone WLs due to `Bowing` is one of the key challenges in developing 3D NAND flash memory. As explained in Section 4.2, `Bowing` defects can be detected by monitoring the state of the status pin after programming all WLs in the target flash blocks. Figure 12b shows the results of the change in bad block counting as the program voltage (V_{PROG}) is raised. Similar to the case of the `Not-Open` defect, even though V_{PROG} is raised from 20 V to 24 V, there is no significant change in detection accuracy for the `Bowing` defect. Figure 12c shows the effect of pre-condition P/E cycles to eliminate infant mortality originating from `Soft`

`Bowing` defect. (Conceptually, a program-only cycle can be a good solution to apply stress. However, due to the erase-before-program property of NAND flash memory, the P/E cycle was selected as a practical solution.) From the results, we observed that by applying just 50 pre-condition P/E cycles, `Hard` and `Soft Bowing` defects could be efficiently screened out, so we can secure the quality of a flash product.

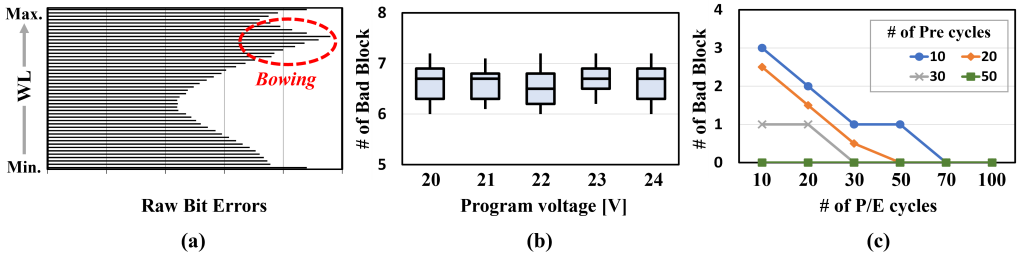


Figure 12. Experimental results for channel hole. `Bowing` defects (**a**) Error characteristics between WLs. (**b**) Detection accuracy vs. program voltage. (**c**) Infant mortality in a flash chip.

Channel Hole Bending

As explained in Section 4.1, unlike other channel hole defects, it is required to exploit the various CKBD patterns to detect `Bending` defects. Figure 13a shows V_{th} distributions of the target flash block after programming CKBD patterns. In the channel hole where `Bending` occurs, since the erased flash cells are not fully inhibited during a program operation, their V_{th} is slightly increased, called the *erase disturb* phenomenon. These abnormal flash cells are sensed as a programmed state (data '0') even though their real state is an erased state (data '1'). Therefore, by performing a read operation with the appropriate read level, we can detect `Bending` defects. Figure 13b shows the relationship between the detection accuracy for `Bending` defect and the level of VCC. As VCC is raised from 2.8 V to 3.6 V (in the datasheet of commercial NAND flash memory, VCC cannot exceed 3.6 V), the detection accuracy is also enhanced because the amount of leakage current between two adjacent channel holes is proportional to VCC (i.e., voltage difference). Figure 13c shows the effect of the number of P/E cycles to screen out the `Soft Bending` defect. From the results, we observed that by applying just 50 P/E cycles, `Soft Bending` defects were efficiently activated into `Hard Bending` defects (i.e., no additional bad blocks during the early stage of flash lifetime).

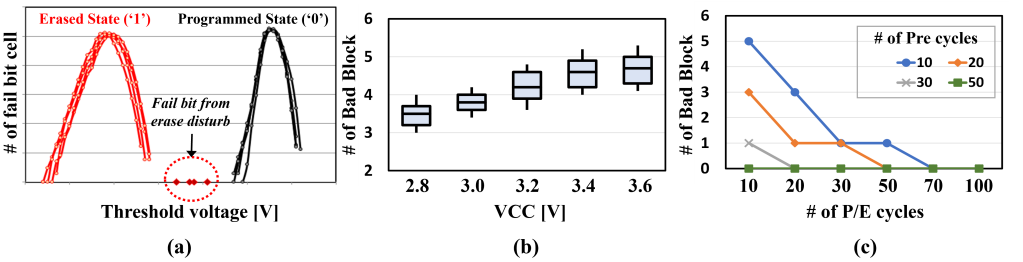


Figure 13. Experimental results for channel hole `Bending` defects (**a**) V_{th} distribution after programming CKBD pattern (**b**) Detection accuracy vs. VCC (**c**) Infant mortality in a flash chip.

5.3. Side Effects Analysis

The key challenge in designing the stress-based screen methodology is suppressing the adversary effect on the flash reliability (i.e., error characteristics) due to electrical stress added to detect the `Soft` defect. Figure 14 shows how electrical stress affects RBERs of flash memory quantitatively. From the evaluation results in Figure 14a,b, we know that the effect of 200 erase cycles on RBER can be neglected even at the end-of-life (EOL) stage. Although there is an RBER difference of 1∼2 bits, it results from an avoidable noise effect such as RTN (Random Telegraph Noise) [34], not a reliability difference. However, when we apply

the pre-condition P/E cycles as a source of electrical stress, we should consider how much flash reliability can be degraded as the number of P/E cycles increases. Figure 14c,d show how much RBER can worsen due to the pre-condition P/E cycles. Although the effect of 50 pre-condition P/E cycles is negligible at the early stage of flash lifetime, at the EOL of a flash block, the RBER difference increases up to 5 bits, and RBER variations between flash blocks in a chip are also enlarged. Therefore, it is necessary to implement new stress conditions to maintain stress effects on defect activation while avoiding adverse impacts on flash reliability.

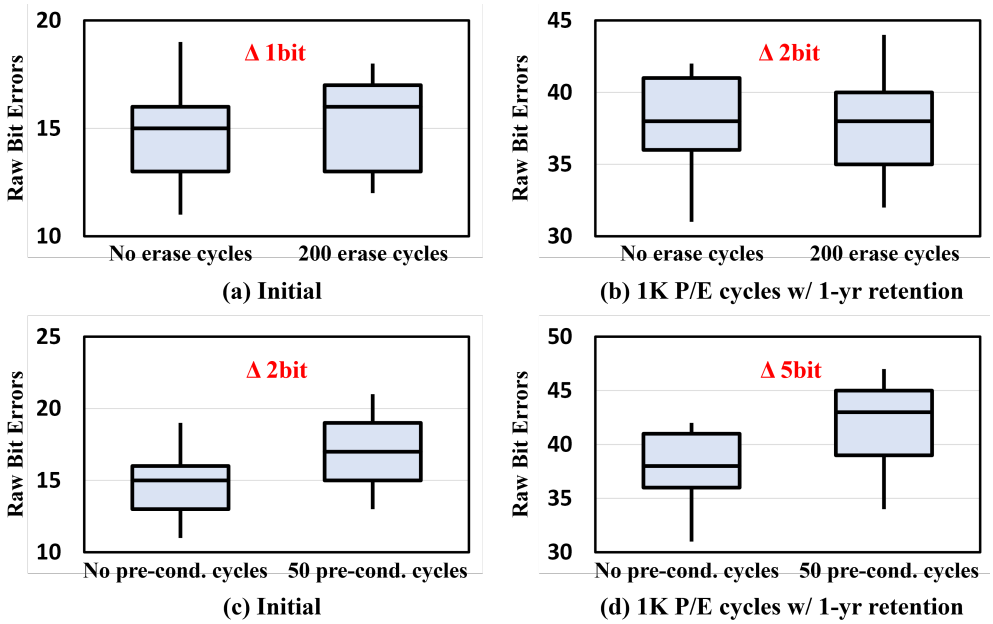


Figure 14. The effect of electrical stress on flash reliability.

Before redesigning the stress condition, we first explored the maximum allowable number of pre-condition P/E cycles. Figure 15a shows that the maximum allowable number of pre-condition P/E cycles needs to be limited by 30 to avoid flash reliability degradation. However, as shown in Figure 14b, 30 pre-condition P/E cycles are insufficient to activate all hidden channel hole defects at room temperature (25 °C). To find out the optimal stress condition, we examined additional bad blocks during the early stage of the flash lifetime while varying the number of pre-condition P/E cycles and operating temperature. Evaluation results in Figure 15d confirmed that when the operating temperature is set to 85 °C, additional bad blocks (i.e., infant mortality) can be removed with only 30 pre-condition P/E cycles without degrading the flash reliability.

5.4. Time Overhead Analysis and Optimization

Since the time required for the test directly increases the production cost, it is one of the key challenges to minimize test time for the successful mass production process of NAND flash memory. To this end, we introduce two approaches to optimize time overhead in our proposed test procedure. One is eliminating redundant test steps, denoted as *Optimized-1*. In our test procedure, to distinguish the `Hard` and `Soft` defects, we performed two function check steps, which are totally identical, before and after the test steps of applying stress. Therefore, the test procedure can be optimized by performing the function check steps only once after the test steps of applying stress. The other is that only defect-prone WLs are tested considering the type of channel hole defects, denoted as *Optimized-2*. For example, the `Bowing` defects are more likely to occur in the WLs near the top layer, whereas the `Bending` defects are concentrated in the bottom WLs. If we select the upper 24 WLs for the `Bowing` defect screen and the bottom 24 WLs for the `Bending` defect screen, respectively, only 48 WLs, which is 1/4 of the total 192 WLs, will require program or read operations

during the function check. (Note that our tested flash block has 48 layers, and each layer has different four WLs that consist of three pages). As a result, with additional optimization, test time can be improved by 72.2% on average without damaging detection accuracy.

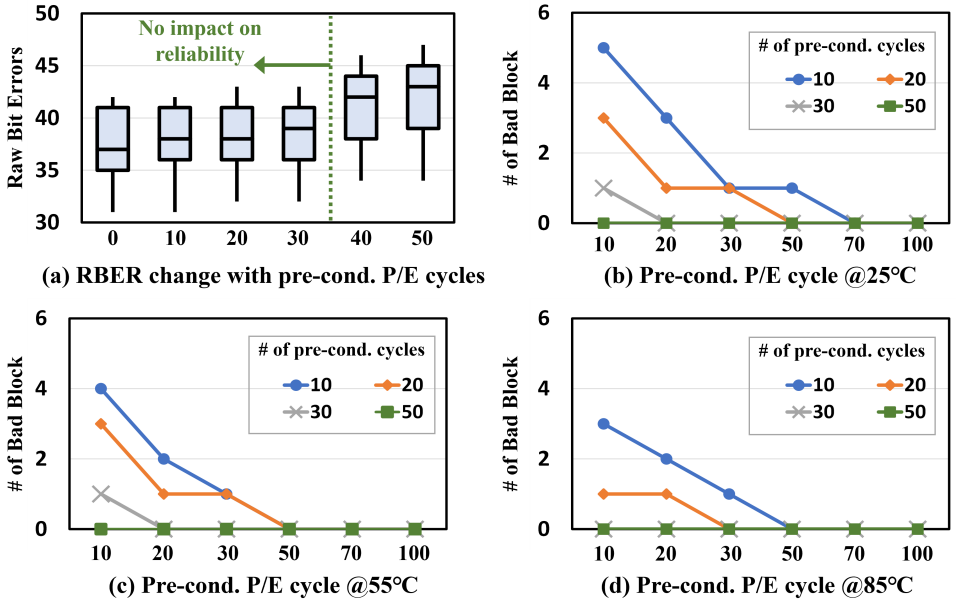


Figure 15. Temperature effect on electrical stress.

Table 1 shows measurement results for test time for a single flash block. Three-dimensional TLC NAND flash memory performs an erase operation at *block* granularity, which causes erase latency `tBERS` to be significantly higher than program latency `tPROG` and read latency `tR` (e.g., `tBERS` = 3.5 ms, `tPROG` = 400 µs, and `tR` = 40 µs [35]). Although the test time in Table 1 seems insignificant (less than 10 sec), it can cause serious issues in advanced modern 3D TLC/QLC NAND flash memory. First, since the capacity of 3D NAND flash memory depends on the number of vertical layers in a flash chip, as the capacity of 3D NAND flash memory increases, the number of WLs tends to increase as well. For example, a flash block of modern 3D TLC NAND flash memory has more than 200 vertical layers [26] that consist of four different WLs, and the number of pages in a single block has increased by 5.3 times in 4 years [12]. Since reading and programming all pages in a block takes up most of the function check time, as the number of pages increases, the function check time also increases linearly. (Note that tERS has a fixed value of 3.5 ms, regardless of the number of pages in a block.) Second, the test time is proportional to the number of blocks in a single flash chip. For example, if there are 2000 blocks in a flash chip, the total test time exceeds 5000 s. Therefore, to overcome the time overhead of the test procedure, a more optimized technique, such as aggressive sampling for WLs or blocks, is required in the future.

Table 1. Test time measurement for a single flash block.

Test Procedure	Function Check Time	Stress Time (200 Erase Cycles and 30 P/E Cycles)	Total Test Time per Block
Proposed	2498.2 ms	7717 ms	10,215.2 ms
Optimized-1	1249.1 ms	7717 ms	8966.1 ms
Optimized-2	314.54 ms	2533 ms	2847.54 ms

6. Conclusions

We have proposed a new defect-centric screen technology that detects and screens out various channel hole defects caused by unique abnormalities in the channel hole profile

of 3D NAND flash memory, such as `Not-Open`, `Bowing`, and `Bending`. Our test procedure consists of two steps depending on the type of channel hole defects: a pattern-based screen and a stress-based screen. The pattern-based screen is effective for detecting the type of `Hard` channel hole defects, whereas the stress-based screen is introduced for detecting the type of `Soft` channel hole defects. Experimental results show that our proposed technique can screen out channel hole defects without degrading flash reliability. In addition, our current version of defect-centric screen methodology has been further optimized to address time overhead problems, thus resulting in 72.2% improvement in total test time. Our technique can be a key solution to enabling mass production of 3D NAND flash memory, even if 3D NAND flash memory continuously increases its capacity.

Author Contributions: Conceptualization and supervision, M.K.; methodology and validation, B.K. and G.S.; formal analysis, B.K.; investigation, G.S.; writing—original draft preparation, M.K. All authors have read and agreed to the published version of the manuscript.

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