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A CMOS Rectifier with a Wide Dynamic Range Using Switchable Self-Bias Polarity for a Radio Frequency Harvester

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Abstract: This paper presents a switchable self-bias polarity on the CMOS complementary cross-coupled rectifier to improve the rectifier's power conversion efficiency (PCE) profile across a wide input power (P_{IN}) dynamic range. This technique achieves this by adaptively switching the polarity of the bias on the n-MOS to overdrive it during low P_{IN} to improve the sensitivity and underdrive it during high P_{IN} to suppress the shoot-through loss and the unnecessary discharge of the coupling capacitor. The popular self-biased p-MOS is also implemented further to reduce the reverse conduction loss during high P_{IN}. The proposed rectifier is fabricated in a 40 nm CMOS process and operates at 900 MHz with a load of 50 kΩ. The proposed rectifier achieved a peak PCE of 72.1% and maintained a 0.8xPCE_{PEAK} across a P_{IN} dynamic range of 11.5 dB.

Keywords: cross-coupled; energy harvesting; power conversion efficiency; RF-DC converter; wireless power transfer

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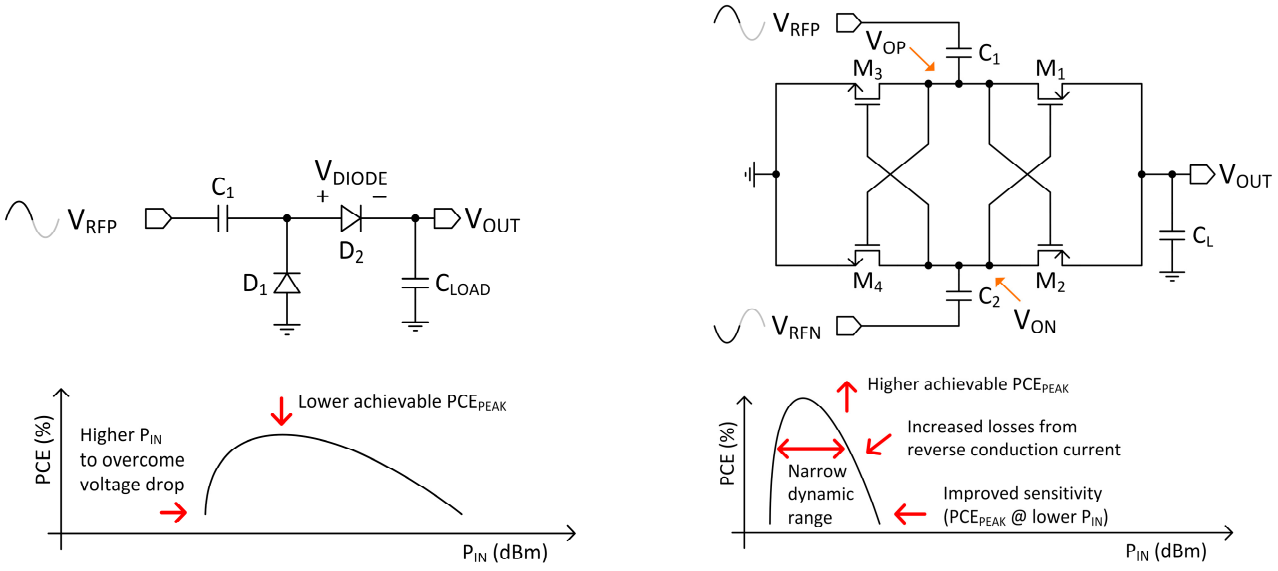
1. Introduction

The adoption of dedicated wireless power transfer (WPT) and energy harvesting (EH) is important to realize a wireless sensor network (WSN) on a massive scale. It relieves the reliance on an onboard battery and reduces the node form factor to achieve a reasonable economy of scale in areas such as structural health monitoring and logistic tracking. The front-end of the RF energy harvesting (RFEH) system is widely implemented with the cross-coupled rectifier for having higher power conversion efficiency (*PCE*) and sensitivity than the Dickson rectifier [1], as summarized in Figure 1. It is the diode voltage (V_{DIODE}) drop in the Dickson rectifier in Figure 1a that reduces the maximum output voltage (V_{OUT}) of the rectifier. As a result, a larger chip area is required to accommodate a greater number of cascading Dickson rectifiers to achieve the required V_{OUT}. Instead of a diode, a diode-configured MOS transistor can be utilized to potentially lower the dropout voltage to the MOS threshold voltage (V_{TH}). Exploitation of the body effect of the MOS was demonstrated by [2–4] to improve further the sensitivity by reducing the V_{TH} at the expense of higher losses at high input power (P_{IN}). The cross-coupled rectifier in Figure 1b eliminates the V_{DIODE} by operating the transistors as switches and having a dropout voltage based on their on-resistance (r_{ON}). It adopts the back-to-back inverter feedback structure similar to the static random-access memory (SRAM) structure. Inevitably, the cross-coupled rectifier also inherited some of the drawbacks, such as the shoot-through current (I_{SHOOT}). Currently, RFEH systems that utilize RF energy as their primary source are plagued by a slew of losses, such as free-space path loss and obstruction between the line-of-sight when operating at far field. Even though these losses are of lesser concern when operating in the near field, the

non-linear rectifier exhibits rapid *PCE* degradation when high P_{IN} incidence on the rectifier leads to a limited and narrow P_{IN} dynamic range. The PCE of the rectifier can be calculated as follows:

$$PCE = \frac{V_{OUT}^2 / R_{LOAD}}{P_{IN}} \quad (1)$$

where R_{LOAD} is the resistive load at the output of the rectifier, and P_{IN} is the input power at the rectifier.



(**a**) (**b**)

Figure 1. Overview of the commonly used rectifiers: (**a**) the Dickson rectifier and (**b**) the cross-coupled rectifier.

Figure 2a shows the block diagram of a typical RFEH system, and Figure 2b shows the details of the proposed rectifier in this work. The cascading DC–DC boost converter provides a regulated supply voltage (V_{SUP}) for the sensor node and, most importantly, functions as a regulated R_{LOAD} to the rectifier to provide optimal *PCE* performance. A buck-boost converter operating in the discontinuous current mode (DCM) by [5] was able to maintain the rectifier *PCE* above 70% across an R_{LOAD} from 10 Ω to 10 kΩ. It was achieved by regulating the input impedance of the converter, making it independent of the converter input voltage (V_{OUT} of the rectifier) while also providing decoupling of the actual R_{LOAD} from the rectifier. In contrast, the study in [6] proposed using a maximum power point tracking (MPPT) algorithm to maintain impedance matching at the interface between the rectifier and DC–DC converter by reconfiguring the number of rectifier stages to achieve a dynamic range from –20 dBm to 20 dBm. At the same time, in addition to modulating the input impedance like [5], the study in [7] also changes the matching network at the input of the rectifier to achieve both input and output matching for its rectifier front-end. However, in applications without the boost converter, an *N*-stage cascading rectifier offers V_{OUT} boosting at a low P_{IN} to meet the minimum V_{SUP} but incurs a higher loss at a high P_{IN} [8]. Furthermore, to achieve an overall higher system efficiency, the rectifier must also address the varying P_{IN}.

Figure 3 shows the concept of the multi-path approach demonstrated by [9,10] achieved an improved P_{IN} dynamic range by dynamically switching between two rectifiers optimized at two targeted P_{IN}. The two rectifiers need not be of the same structure as reported in [11–13], where the cross-coupled and Dickson rectifiers were used for low and high P_{IN}, respectively. It allows the effective use of the Dickson rectifier at a higher P_{IN} when the dropout voltage is of lesser concern. It avoids the drawback of the increased losses in

the cross-coupled rectifier. However, it is challenging to predetermine the optimal transition between the two rectifiers, resulting in sub-optimal performance and power loss. A series-parallel reconfiguring of an N-stage rectifier also demonstrates an improved P_{IN} dynamic range [14,15]. A 6-stage to 12-stage Dickson rectifier by [14] was able to achieve a 15 dB dynamic range but suffered from downtime due to the difficulty of the control circuit to discern the appropriate configuration. An interesting reconfiguring approach was proposed in [15] by stacking different V_{TH} devices to achieve a dynamic range of 22.8 dB. It uses native devices for low P_{IN} and sequentially stacks higher V_{TH} devices in series to limit the losses and obtain an equivalent longer channel length device. It is important to note that [15] requires extensive and careful optimization due to the use of different devices, which severely limits its practicality against device variation during mass production. However, the rectifier input impedance (Z_{REC}) also requires meticulous optimization [16] or an adaptive matching network [17,18] to address the change in Z_{REC} based on the configuration. Lastly, self-biasing improves the P_{IN} dynamic range by reducing the reverse conduction loss (P_{REV}) from the p-MOS by limiting the reverse conduction current (I_{REV}) and improves the sensitivity by increasing the overdrive on the n-MOS [19,20]. However, this also results in a reduced p-MOS forward conduction current (I_{FWD}) [19] and introduces a conduction imbalance between the p-MOS and the n-MOS, resulting in the inefficiency of the voltage boosting introduced by the coupling capacitors. The study in [21], moreover the study in [22], proposed the underdrive of the n-MOS to mitigate the conduction imbalance at high P_{IN}, which requires extensive optimization to ensure reasonable sensitivity at low P_{IN}. Furthermore, the diode-configured transistors used to generate the self-bias voltage are also susceptible to process and temperature variation with minimally accessible tune options. The studies in [23,24] addressed this issue by tracking V_{OUT} and providing continuous active compensation on the n-MOS.

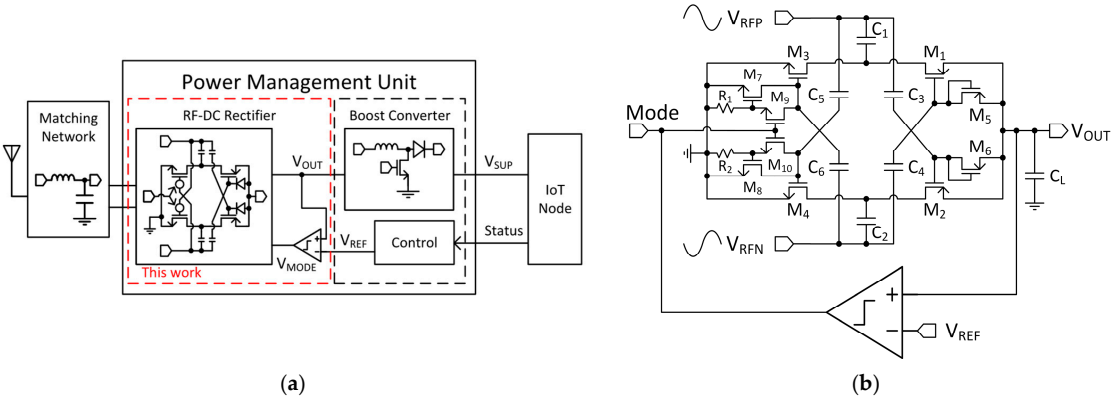


Figure 2. Block diagram of the (**a**) RF energy harvesting system and (**b**) the proposed rectifier.

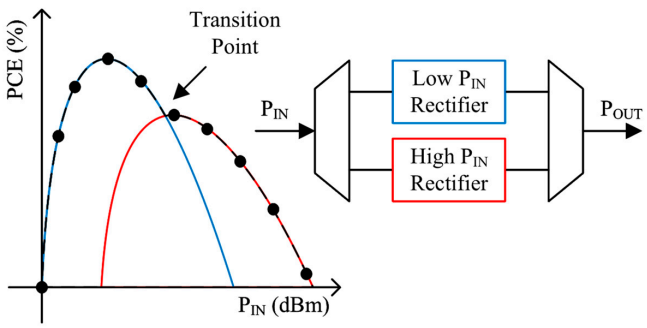


Figure 3. An illustration of a typical PCE versus P_{IN} for a multi-path rectifier for P_{IN} dynamic range improvement.

This paper proposes a simpler approach suitable for low-cost systems by switching the polarity of the self-bias voltage applied to the gate terminal of the n-MOS to achieve

two different PCE_{PEAK} at two different P_{IN}. The advantage of this approach is that it provides two distinct PCE profile transitions with a single rectifier and offers a tuning option. Section 2 discusses the operating principle of the rectifier; Section 3 presents the measurement results of the rectifier; Section 4 provides the conclusion.

2. Proposed Rectifier Analysis and Description

2.1. The Cross-Coupled Rectifier and Its Issues

The cross-coupled rectifier is fundamentally formed by two inverter structures in feedback. When considering half of the period, the differential input V_{RFP} and V_{RFN} is rectified by transferring charges from C_1 to C_L when $V_{OP} > V_{OUT}$ and replenishing the charges in C_2 from the ground (V_{SS}) when $V_{SS} > V_{ON}$. The sinusoidal V_{OP} or V_{ON} results in I_{REV} when $V_{OUT} > V_{OP}$ or V_{ON} due to the p-MOS bidirectional characteristic. The single-sided self-bias by [19] reduces I_{REV} by introducing a clamping voltage for the p-MOS at the expense of I_{FWD}. The role of the n-MOS is often treated as a means for current continuity. However, due to the sinusoidal nature of V_{OP} and V_{ON}, the n-MOS also experiences a similar issue as the p-MOS. The double-sided self-bias in [19] positively bias the n-MOS to lower the overdrive to improve the sensitivity. However, this resulted in severe *PCE* degradation at high P_{IN} due to the timing mismatch between the p-MOS and n-MOS. Figure 4a shows half of the cross-coupled rectifier, along with Figure 4b illustrates the timing mismatch between M_1 and M_3. The charges are transferred by $I_{FWD,M1}$ from C_1 to C_L through M_1 when $V_{OP} > kV_{OUT}$. As V_{OP} transit, M_1 discharges C_L when $kV_{OUT} > V_{OP}$ and until M_1 turns off when $kV_{OUT} - V_{ON} < |V_{THP}|$ shown in $I_{REV,M1}$. At the same time, M_3 also turns on when $V_{ON} - V_{SS} > V_{THN}$ resulting in an $I_{REV,M3}$ discharging C_1. M_3 is only able to replenish the charges in C_1 with $I_{FWD,M3}$ when $V_{SS} > V_{OP}$ and $V_{ON} - V_{OP} > V_{THN}$. The key observations are: (1) an overlap of I_{REV} provides a conduction path from V_{OUT} to V_{SS}, resulting in I_{SHOOT}, and (2) if I_{REV} for M_3 is longer than M_1, it reduces of number of charges stored in C_1 and degrades the effectiveness of the voltage boosting provided by the coupling capacitor. This can be expressed as follows:

$$V_{OP} = \frac{1}{2} kV_{OUT} + \eta_{COUPLING}\, V_{RFP} \tag{2}$$

$$\eta_{COUPLING} = \frac{C_1}{C_1 + C_{PARASITIC}} \tag{3}$$

where k factors the deviation from the analytical result of ½ [25], and $\eta_{COUPLING}$ is the coupling efficiency between C_1 and the parasitic capacitance ($C_{PARASITIC}$) on node V_{OP} in Equation (3). The equivalent $C_{PARASITIC}$ is the sum of the gate-drain overlap capacitance, gate-source overlap capacitance and gate-body oxide capacitance contributed by the p-MOS and n-MOS [25]. Under a steady-state operation, the variation in V_{OUT} is minimal with a suitable C_L and can be regarded as an ac virtual ground.

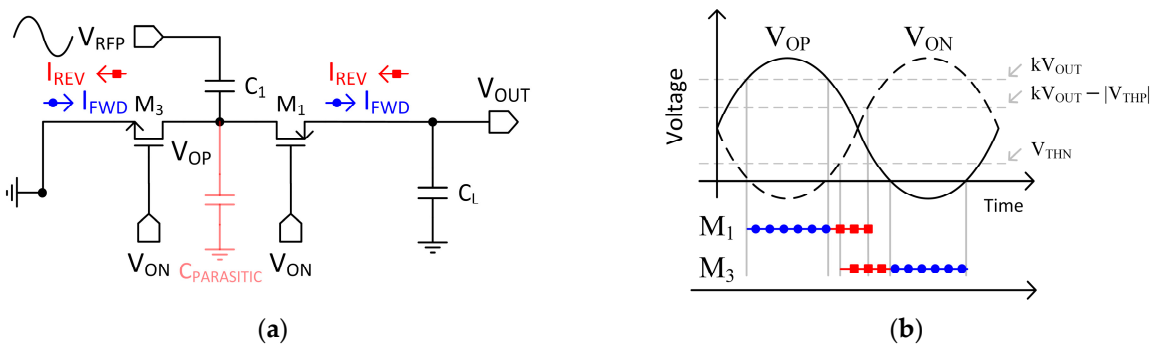


Figure 4. Illustration of the (**a**) half-circuit cross-coupled rectifier and its (**b**) timing analysis of I_{REV} and I_{FWD} for M_1 and M_3.

2.2. Description of the Proposed Rectifier

Figure 5 shows the schematic of the proposed rectifier with a switchable self-bias polarity. The main cross-coupled rectifier is formed by M_1–M_4 and C_1–C_2 similar to Figure 1b. The low V_{TH} (LVT) core devices are used for M_1–M_4 to achieve better sensitivity. On the other hand, metal-insulator-metal (MIM) capacitors are used for C_1–C_2 to minimize the amount of bottom plate parasitic capacitors while maximizing the amount of capacitance per unit area. Unlike Figure 1b, the gate terminal of M_1–M_4 is not connected to V_{OP} and V_{ON}, but instead, the V_{RFP} and V_{RFN} are coupled through C_3–C_6. It allows the voltage stored in C_3–C_6 to assist or restrict the overdrive to turn on M_1–M_4. The p-MOS positive self-bias voltage is generated using the diode-configured M_5–M_6 and C_3–C_4. In this diode configuration, M_5–M_6 provide a unidirectional conducting path to charge and store the charges in C_3–C_4. It only happens when V_{OUT} is sufficiently large to forward bias M_5–M_6. M_5–M_6 are implemented with high V_{TH} (HVT) core devices to prevent degrading the I_{FWD} at low P_{IN} due to the generated p-MOS self-bias voltage. The p-MOS positive self-bias voltage is crucial during high P_{IN} to limit I_{REV}. The n-MOS positive and negative self-bias voltage is generated with LVT M_7–M_{10}, R_1–R_2 and C_5–C_6. The performance at low P_{IN} is improved using a positive n-MOS self-bias voltage similar to [19]. This is performed by turning off M_9–M_{10} and allowing R_1–R_2 to provide a dc-short between the gate-source terminal of M_7–M_8. The conducting path of the diode-configured M_7–M_8 allows charges to flow from V_{SS} to C_5–C_6. The positive n-MOS self-bias voltage makes it easier to turn on M_3–M_4 even with a smaller V_{RFP} and V_{RFN}. However, an n-MOS positive self-bias voltage introduces conduction mismatch during high P_{IN}, as illustrated in Figure 4. As such, a negative n-MOS self-bias is generated by turning on M_9–M_{10} to address the conduction mismatch. It reconfigures M_7–M_8 by providing a dc-short between the gate-drain terminal to change the conducting path from C_5–C_6 to V_{SS}. This operation depletes the charges stored in C_5–C_6, resulting in a negative self-bias voltage. The r_{ON} of M_9–M_{10} is much smaller than R_1–R_2.

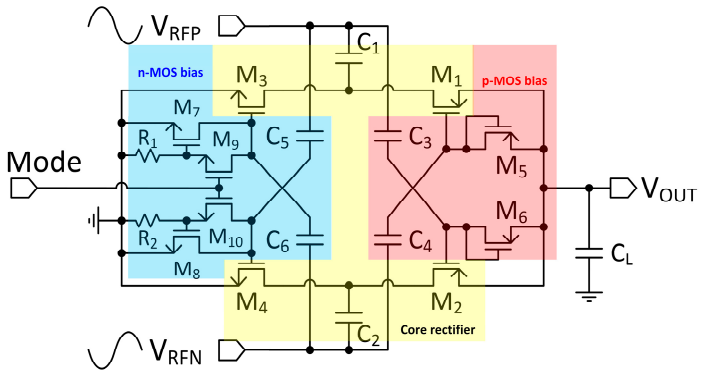


Figure 5. Schematic of the proposed rectifier with switchable self-bias polarity on n-MOS.

2.3. Operation of the Proposed Rectifier

The symmetry of the rectifier simplifies the analysis by considering $V_{RFP} > V_{RFN}$ in Figure 6a,c; as such, only M_1 and M_4 are involved in the main rectifying path (red path). The p-MOS bias is generated with M_5 and stored in C_4 (blue path). Figure 6a does not indicate the blue path due to the use of high V_{TH} (HVT) M_5 that prevents generating a bias voltage for p-MOS M_1. Different sets of devices are involved in generating the n-MOS bias at different P_{IN} modes. M_7, M_9, C_6 and R_1 are involved during low P_{IN}, while M_8, M_{10}, C_5 and R_2 are involved during high P_{IN}. In Figure 6a, M_9 is disabled and allows R_1 to diode-configured M_7 to provide a conducting path (green path) to charge C_6 at a low P_{IN}. Figure 6c shows a different conducting path (green path) when M_{10} is enabled. It reconfigures M_8 to provide a discharging path for C_5 at high P_{IN}. Similar analysis can be performed when $V_{RFP} < V_{RFN}$ in Figure 6b,d. The body-terminal of all p-MOS and n-MOS have been connected to V_{OUT} and V_{SS} (ground), respectively. For the following analysis,

the voltages are mentioned in the format of $V_{X,Y,P}$ where X indicates the voltage type, Y represents the device when applicable, and P indicates the phase as $\phi1$: $V_{RFP} > V_{RFN}$ and $\phi2$: $V_{RFP} < V_{RFN}$ when applicable.

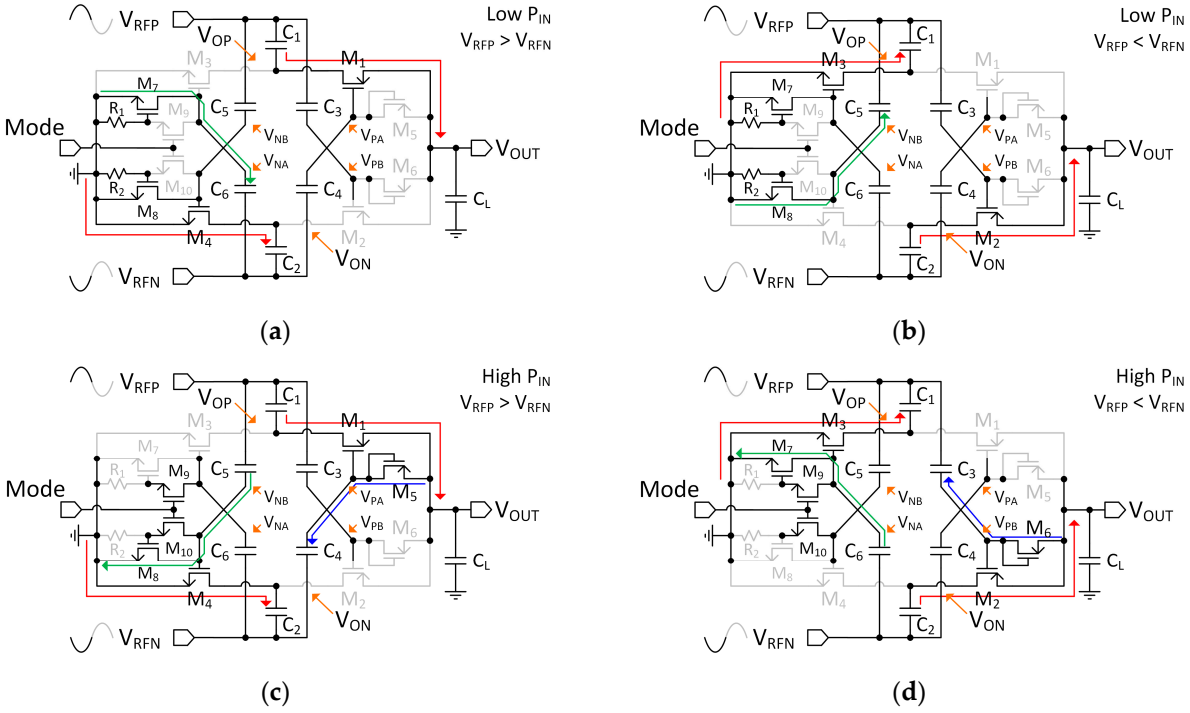


Figure 6. Operation of the proposed rectifier for low P_{IN}: (**a**) $V_{RFP} > V_{RFN}$, (**b**) $V_{RFP} < V_{RFN}$ and high P_{IN}, (**c**) $V_{RFP} > V_{RFN}$, and (**d**) $V_{RFP} < V_{RFN}$.

During low P_{IN} operation (mode = 0), the diode-configured M_5 inhibits the conduction path from V_{OUT} due to the high V_{TH} (HVT) device where $V_{OUT} - V_{PA,\phi1} < |V_{THP,M5}|$ and as such, $V_{PA,\phi1} \approx V_{RFN,\phi1}$. The reverse overdrive of M_1 $V_{SG\text{-}REV,M1,\phi1} = V_{OUT} - V_{PA,\phi1}$ due to the bidirectional conduction characteristics of the device ($V_{OUT} > V_{OP,\phi1}$). The reverse conduction current (I_{REV}) is still manageable due to a small $V_{SG\text{-}REV,M1,\phi1}$ at low P_{IN}. It favors maintaining a larger forward conduction current (I_{FWD}). I_{FWD} occurs only when $V_{OP,\phi1} > V_{OUT}$; where the forward overdrive of M_1 $V_{DG\text{-}FWD,M1,\phi1} = V_{OP,\phi1} - V_{PA,\phi1} = (½V_{OUT} + V_{RFP,\phi1}) - V_{RFN,\phi1}$. As for M_4, the study in [19] demonstrated an improved sensitivity by providing a positive bias onto the gate terminal of M_4 to lower the overdrive V_{GSN} required to turn M_4 on. The proposed rectifier adopted a similar configuration using M_8 and R_2. The bias is generated with R_2 providing a dc-short between the gate terminal and the source terminal of M_8 and stored in C_5 as $V_{C5,\phi2} = V_{SS} - V_{THN,M8} - V_{RFP,\phi2}$ during $\phi2$. At $\phi1$, $V_{GSN,M4,\phi1} = V_{RFP,\phi1} + V_{C5,\phi2} - V_{SS}$. It can be observed in Figure 7a that V_{C5} increases with P_{IN}. Despite the improved sensitivity at low P_{IN}, it is irrefutable that the assistance in the overdrive also leads to difficulty in turning off M_4. Consequentially, it results in a rapid *PCE* degradation due to a conduction mismatch between the p-MOS and n-MOS, resulting in the unnecessary discharge of C_1 and C_2 and reduced efficiency of the voltage doubling functionality. This effect can be observed in Figure 7b for mode = 0 with the rapid decrease in $½k = V_{C1}/V_{OUT}$ with increasing P_{IN}.

During high P_{IN} operation (mode = 1), M_1 is self-biased with M_5 as $V_{PA,\phi1}$ is sufficient to forward bias and turn on M_5 to charge C_4 to generate $V_{C4,\phi1} = V_{OUT} - |V_{THP,M5}| - V_{RFN,\phi1}$ when $V_{OUT} - V_{PA,\phi1} > |V_{THP,M5}|$. The bias reduces I_{REV} by limiting $V_{SG\text{-}REV,M1,\phi1} = V_{OUT} - V_{PA,\phi1} = |V_{THP,M5}|$. The reduced I_{REV} comes at the expense of I_{FWD} when the charges in C_1 are transferred to the output. I_{FWD} occurs when $V_{OP,\phi1} > V_{OUT}$ with $V_{DG\text{-}FWD,M1,\phi1} = V_{OP,\phi1} - V_{PA,\phi1} = (½V_{OUT} + V_{RFP,\phi1}) - (V_{C4,\phi1} + V_{RFN,\phi1}) = V_{RFP,\phi1} - ½V_{OUT} + |V_{THP,M5}|$. As for M_4, to address the concern in the previous mode = 0, M_{10} is introduced as a switch

to reconfigure the conduction direction of M_8 to limit the V_{GSN} permissible to $V_{GSN,M4,\phi1} = V_{DS,M10} + V_{THN,M8}$. It is equivalent to providing a negative bias to reduce $V_{GSN,M4,\phi1}$ by depleting charges in C_5, thereby generating a negative bias $V_{C5,\phi1} = -(V_{RFP,\phi1} - V_{SS} - V_{THN,M8})$ with a negative charge pump. The r_{ON} of M_{10} is designed to be much smaller than R_2. It can be observed in Figure 7a that a negative bias V_{C5} is generated. Subsequently, it is clamped and reversed due to the presence of the body diode in the CMOS transistor. Unlike the low P_{IN} condition, ½k remains relatively stable at ½ and does not exhibit rapid reduction with increasing P_{IN} in Figure 7b. In this mode, a higher V_{OUT} is generated at a lower P_{IN} due to an increased PCE. As such, an excessively high P_{IN} must not be applied to the rectifier to prevent overvoltage beyond the rated $|V_{DS}|$ across M_2 and M_3 in the off state. The transient simulation in Figure 8 further shows a reduced $+I_{DN,M3}$. It indicates the reduction in unnecessary discharge of C_1. However, there is a reduced $|-I_{DN,M3}|$ from 454 µA to 78 µA, which hinders the ability to replenish C_1 with M_3. Therefore, during the design of the proposed rectifier, the net flow of charges to C_1 and C_2 $\Delta Q = Q_{N\text{-}MOS} - Q_{P\text{-}MOS} \geq 0$ C is considered to ensure the effectiveness of M_3 and M_4 and prevent excessive negative bias.

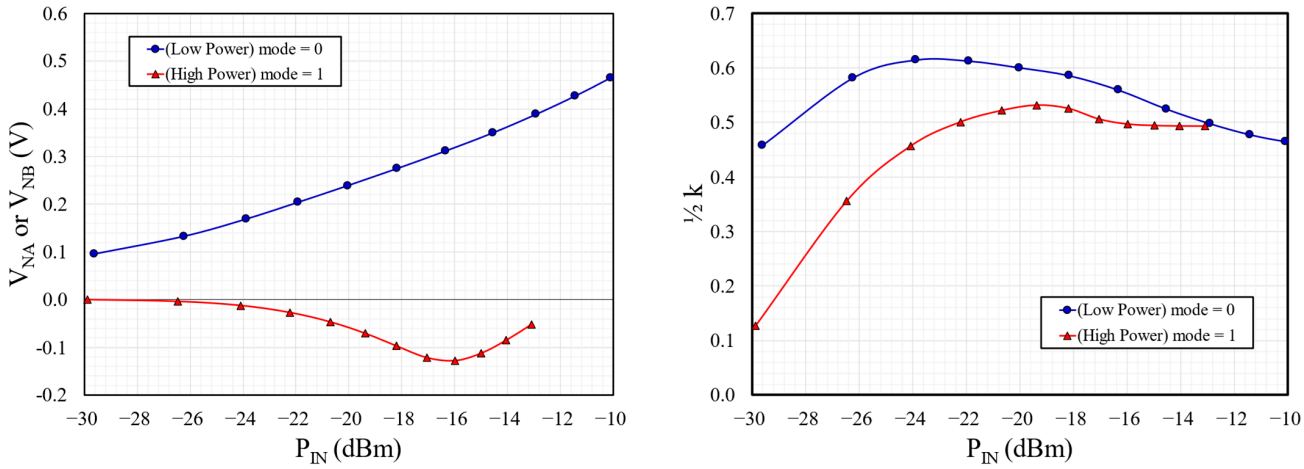


Figure 7. Simulation of (**a**) generated bias of V_{NA} or V_{NB} (V_{C6} or V_{C5}) and (**b**) ½ k = V_{C1}/V_{OUT}.

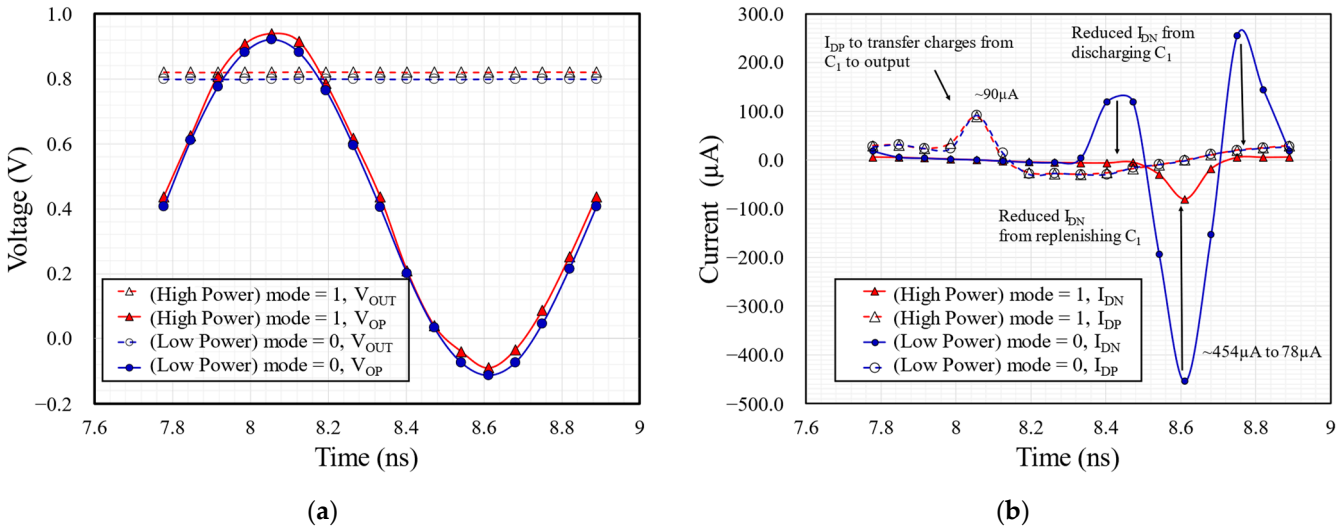


Figure 8. Transient simulation of (**a**) V_{OUT} and V_{OP} (**b**) I_{DS} of p-MOS I_P and n-MOS I_N.

2.4. Description of the Common-Gate Comparator

The common-gate comparator in Figure 9 is used to switch between the low and high P_{IN} and has a similar implementation as [9] using HVT devices. It operates at the subthreshold region to minimize the power consumption of the comparator. A hysteresis is provided by M_{15} and M_{16} in positive feedback when V_{MODE} = 0 V. It ensures the comparator initializes with V_{MODE} = 0 V and requires V_{OUT} to be sufficiently high to overcome the hysteresis to trigger a change in V_{MODE}. The comparator must configure the rectifier in the low-power mode (mode = 0) during the power-up sequence. The high-power mode (mode = 1) reduces the rectifier sensitivity due to a reduced n-MOS overdrive voltage and potentially prevents sufficient V_{OUT} from being generated in a low P_{IN} condition. During system initialization, the equivalent R_{LOAD} at the rectifier is high, with most of the system in either the standby or sleep mode. In the low-power mode, the rate of V_{OUT} versus P_{IN} profile is gentler than in the high-power mode, which prevents a rapid V_{OUT} build-up at high P_{IN}. The functional comparison is performed by Kirchoff's voltage loop between M_{11} and M_{12} as follows:

$$V_{REF} - V_{OUT} = (\Delta V_{M11} + V_{THP,M11}) - (\Delta V_{M12} + V_{THP,M12}) \tag{4}$$

$$\Delta V_{MX} = nV_T \ln \frac{I_{D,MX}}{I_{D0}\frac{W}{L}_{MX}\left(1 - e^{-\frac{V_{SD,MX}}{V_T}}\right)} \tag{5}$$

where I_{D0} is the characteristic current of the transistor, W/L is the aspect ratio of the transistor, V_T is the thermal voltage, n is the subthreshold slope factor, λ is the channel length modulation coefficient, and ΔV can be determined from Equation (5) for the overdrive voltage. ΔV_{M11} contributes to the offset voltage (V_{OS}) as $I_{D,M11} \neq 0$, while ΔV_{M12} is negligible due to $I_{D,M12} \approx 0$ when $V_{REF} > V_{OUT}$. Assuming that V_{OS} is compensated with V_{REF}, the effect of V_{OS} can be neglected for simplicity. The output of the comparator (V_{MODE}) tracks V_{OUT} when $V_{OUT} > V_{REF}$, as shown in Figure 10.

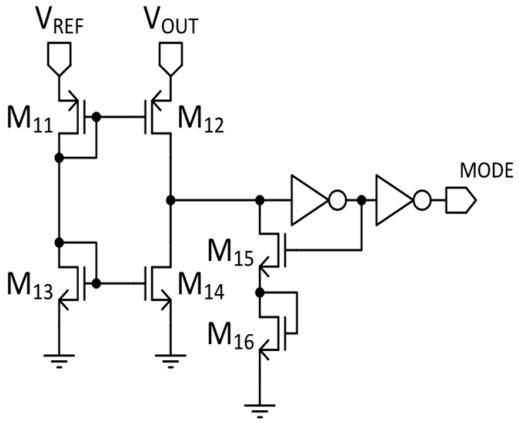


Figure 9. Schematic of the low-power common-gate comparator.

Figure 11a shows the total current (I_{TOTAL}) consumption from both V_{REF} and V_{OUT} of the comparator by varying V_{REF} at the typical process corner. The various process corners are simulated, and the upper and lower bound of the total current consumption having I_{TOTAL} < 6 nA with the worst corner at the ff corner due to a lowering of both p-MOS and n-MOS V_{TH}. Figure 11b shows the impact of the comparator on the *PCE* of the proposed rectifier by examining the current ratio between the comparator and the I_{OUT}. The comparator contributes less than 0.1% of I_{OUT}, making it suitable for the rectifier operating at low P_{IN} in a harvesting application.

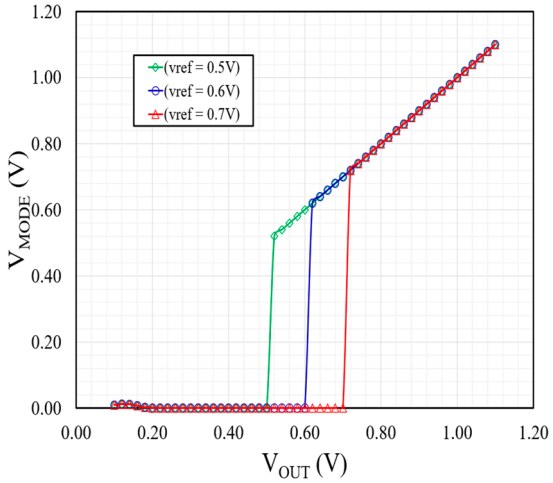


Figure 10. Simulated comparator output V_{MODE} versus V_{OUT} at different V_{REF}.

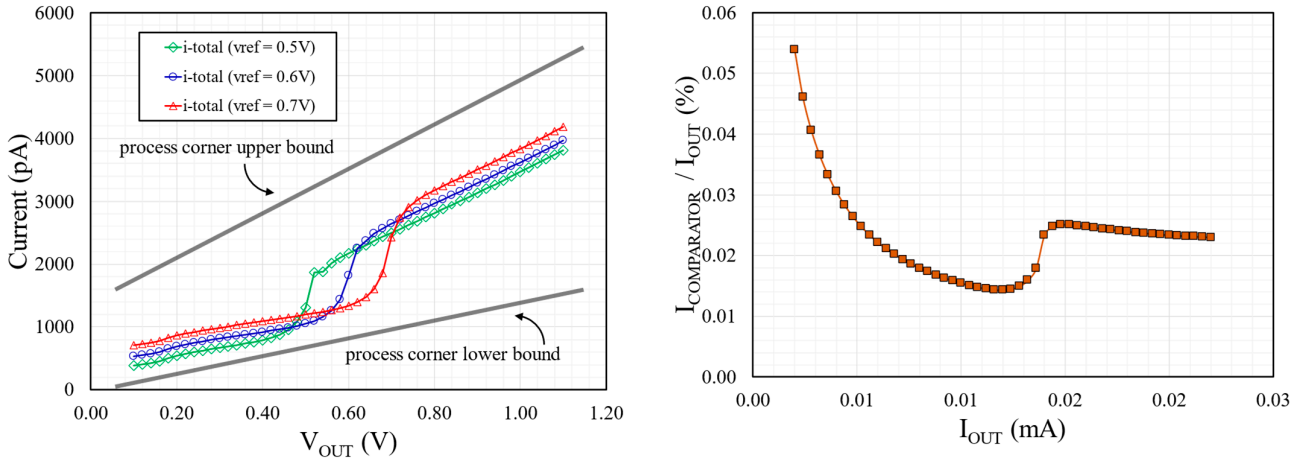


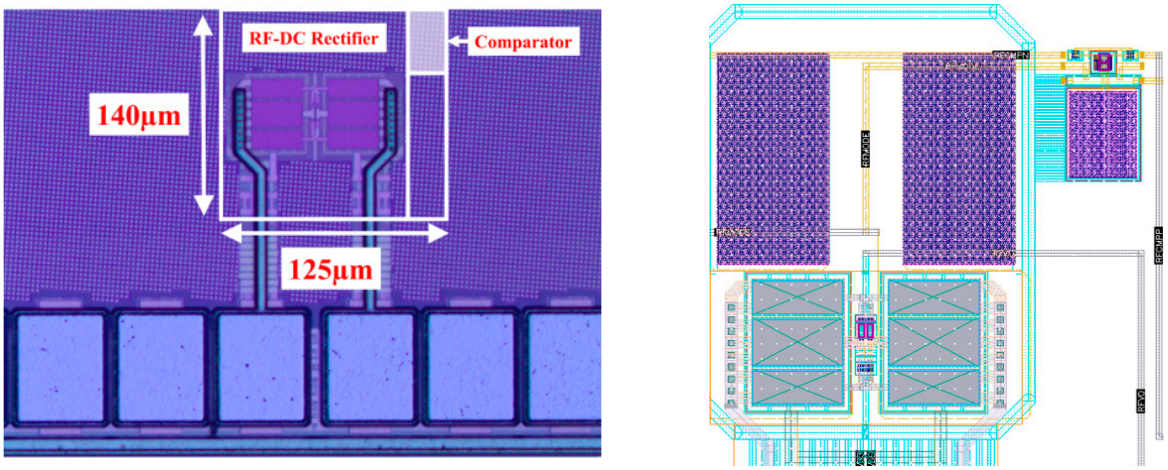
Figure 11. Simulated (**a**) total current consumption of comparator at different V_{REF} and (**b**) comparator-to-rectifier current ratio at R_{LOAD} = 50 kΩ and V_{REF} = 0.6 V.

3. Measurement Results

The proposed rectifier is implemented in a 40 nm low-power CMOS node. It occupies an area of 125 µm × 140 µm, as shown in Figure 12. The rectifier is optimized at P_{IN} = −16 dBm, and the device parameters are tabulated in Table 1. The measurement setup in Figure 13a consists of a vector network analyzer (VNA) (Agilent E5061B), a digital multimeter (Agilent 34461A) and a test fixture with the rectifier in QFN40. V_{OUT} and S_{11} are recorded while sweeping the VNA output port power. S_{11} is determined by de-embedding the test fixture and setting the reference plane at the pads of the package. The rectifier's effective P_{IN} is determined as follows:

$$\underset{[\text{dBm}]}{P_{IN}} = \underset{[\text{dBm}]}{P_{SOURCE}} - \underset{[\text{dB}]}{L_{INSERT}} + \underset{[\text{dB}]}{10\log\left(1-|S_{11}|^2\right)} \quad (6)$$

where P_{SOURCE} is the output power of the VNA port, and L_{INSERT} is the insertion loss due to the test fixture.



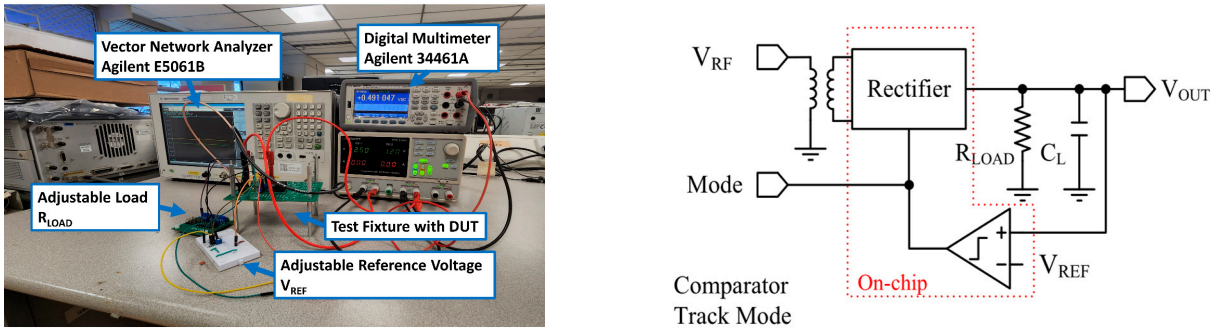
(**a**) (**b**)

Figure 12. Chip (**a**) micrograph and (**b**) layout of the proposed rectifier.

Table 1. Device parameters of the switchable polarity bias rectifier.

Device	Type	Width/Length
M_1–M_2	LVT	24 µm/40 nm
M_3–M_4	LVT	4 µm/40 nm
M_5–M_6	HVT	0.2 µm/2 µm
M_7–M_8	LVT	0.2 µm/2 µm
M_9–M_{10}	LVT	2 µm/100 nm
R_1–R_2	Poly	4 MΩ
C_1–C_6	MIM	630 fF
M_{11}–M_{12}	LVT	600 nm/2 µm
M_{13}–M_{14}	2.5V GP [1]	500 nm/4 µm
M_{15}–M_{16}	2.5V GP [1]	3 µm/2 µm
Inverter p-MOS	2.5V GP [1]	600 nm/2 µm
Inverter n-MOS	2.5V GP [1]	3 µm/2 µm

[1] GP is the general-purpose device with higher V_{TH} than HVT.



(**a**) (**b**)

Figure 13. Measurement (**a**) setup and (**b**) configuration for the rectifier in comparator-track (CT).

The rectifier is measured with different configurations to determine its performance through the MODE pin, as shown in Figure 13b. The low-power (LP) mode with $V_{MODE} = V_{SS}$ and the high-power (HP) mode with V_{MODE} = 1.1 V are characterized to determine the two PCE_{PEAK}. The comparator-track (CT) mode switches between the two PCE_{PEAK} with an external V_{REF} for the measurement; V_{REF} is available from the PMU. The measured PCE versus P_{IN} is shown in Figures 14a, 15a and 16a for different R_{LOAD}. Figures 14b, 15b and 16b show V_{OUT} versus P_{IN} for different R_{LOAD}. The measurement is performed at 900 MHz

with a R_{LOAD} of 50 kΩ and a C_L of 10 pF. The proposed rectifier in the LP mode has a PCE_{PEAK} = 69% at a P_{IN} = −21 dBm; while operating in the HP mode, it has a PCE_{PEAK} = 75% at a P_{IN} = −17.5 dBm. During the CT mode, it exhibited an improved P_{IN} dynamic range performance of 11.5 dB across a 0.8 × PCE_{PEAK} with an externally provided reference voltage (V_{REF}) of 0.6 V. The CT has a sensitivity of −20.8 dBm to achieve a V_{OUT} of 1 V for an R_{LOAD} of 1 MΩ.

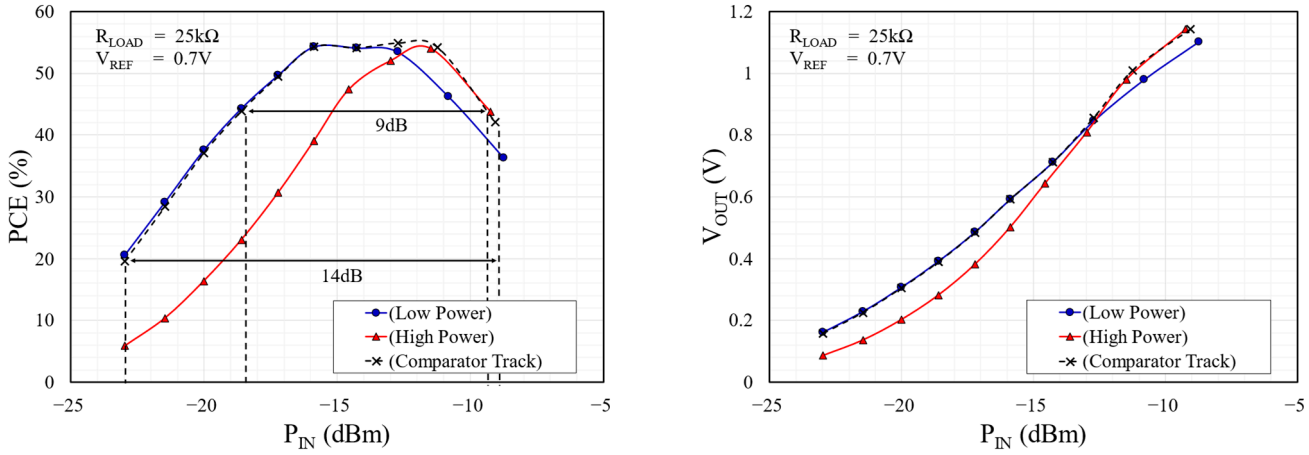


Figure 14. Measured results for R_{LOAD} = 25 kΩ and V_{REF} = 0.7 V: (**a**) *PCE* versus P_{IN} and (**b**) V_{OUT} versus P_{IN}.

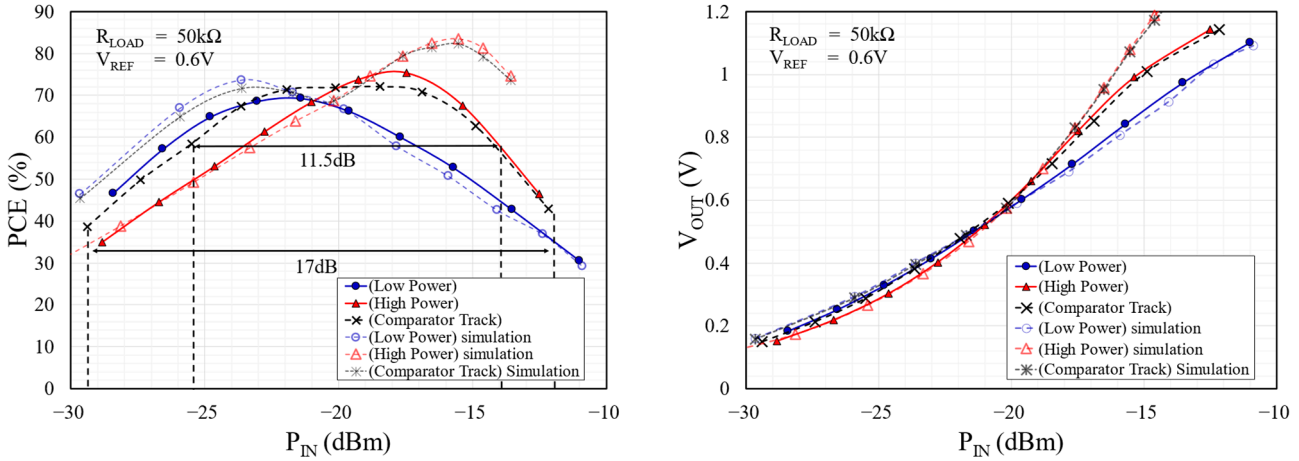


Figure 15. Measured results for R_{LOAD} = 50 kΩ and V_{REF} = 0.6 V: (**a**) *PCE* versus P_{IN} and (**b**) V_{OUT} versus P_{IN}.

Figure 17 shows the PCE_{PEAK} versus R_{LOAD}. The proposed rectifier has the optimal performance at R_{LOAD} = 50 kΩ. However, with an increasing R_{LOAD}, the internal losses in the rectifier dominate over P_{OUT}, resulting in *PCE* degradation. Furthermore, a higher V_{OUT} is generated at a much lower P_{IN}, which prematurely switches the polarity of the n-MOS bias and shifts the operating conditions between the p-MOS and n-MOS, resulting in a degraded *½k* when the proposed rectifier is operating in the CT mode. On the other hand, *PCE* also degrades with further reducing R_{LOAD} as R_{IN}/R_{LOAD} reduces the $V_{OUT}/2 \mid V_{RFP} \mid$ despite an increase to $I_{OUT}/I_{INTERNAL}$; R_{IN} is the inverse of the real admittance of the rectifier and $I_{INTERNAL}$ is the internal current of the rectifier [26]. This trend was also reported in the analytical studies by [25]. The *PCE* profile can be tuned by varying V_{REF}, as shown in Figure 18.

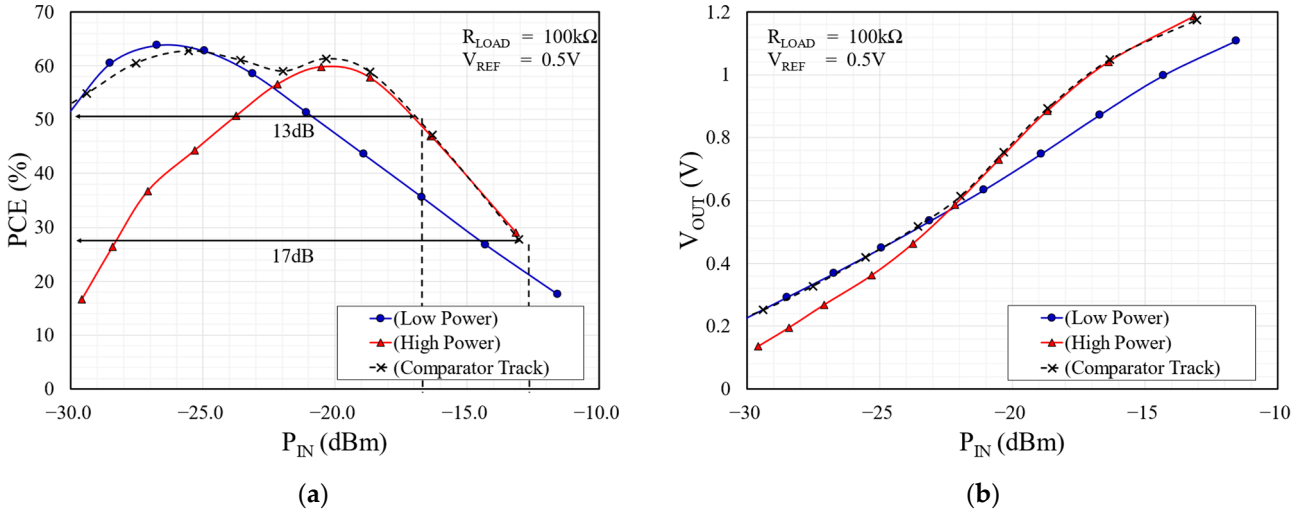


Figure 16. Measured results for R_{LOAD} = 100 kΩ and V_{REF} = 0.5 V: (**a**) *PCE* versus P_{IN} and (**b**) V_{OUT} versus P_{IN}.

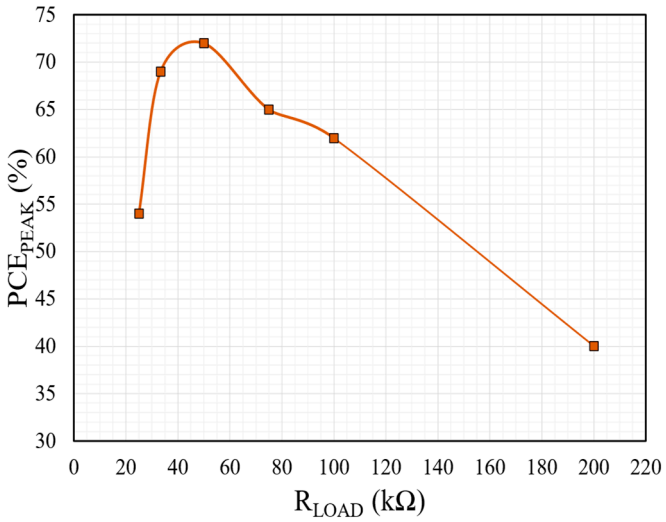


Figure 17. Measured PCE_{PEAK} versus R_{LOAD}.

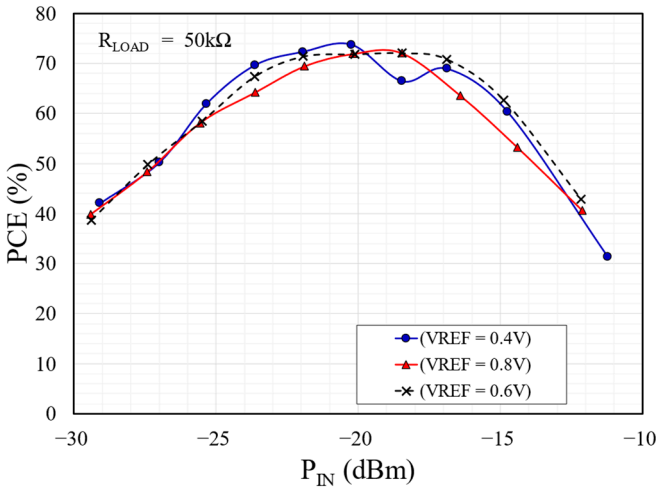


Figure 18. Measured *PCE* versus P_{IN} with R_{LOAD} = 50 kΩ for V_{REF}.

Table 2 compares the proposed rectifier with that of other rectifiers employing similar strategies to achieve P_{IN} dynamic range improvement. The proposed switchable polarity bias can provide a P_{IN} dynamic range of 11.5 dB and 17 dB to maintain a $PCE > 0.8xPCE_{PEAK}$ (PR1) and $PCE > 20\%$ (PR2) at a R_{LOAD} of 50 kΩ, respectively. The sensitivity of the proposed rectifier characterized at 100 kΩ is comparable to other work, but it fares 2 dB higher than [19,27] due to an increase in the parasitic loading on the n-MOS. Under the V_{OUT} = 1 V condition for sensitivity characterization, the proposed rectifier is operating in high P_{IN} with negative polarity bias at the gate terminal of the n-MOS which degrades the sensitivity. Despite this trade-off, the proposed rectifier achieved a better PR1 and PR2 than [19,27]. Wider PR2 was achieved by improving the low P_{IN} performance with the use of native devices with three configuration modes for [15], while dynamic body bias was implemented on top of self-biasing for [20]. On the other hand, the study in [12] uses a Dickson rectifier in the last stage of a 3-stage rectifier to minimize I_{REV} at high P_{IN}, thereby changing the *PCE* degradation characteristic and achieving an additional P_{IN} dynamic range.

Table 2. Performance comparison of proposed rectifier with reported state-of-the-art rectifier.

	This Work	**TVLSI 2023 [15]**	**TCAS II 2023 [12]**	**T-MTT 2020 [20] # ***	**T-MTT 2018 [19]**	**MWCL 2016 [27]**
Technology	40 nm	0.13 µm	65 nm	65 nm	0.18 µm	0.18 µm
Frequency	900 MHz	900 MHz	900 MHz	900 MHz	900 MHz	1 GHz
Technique	Switchable bias	Reconfigurable stack	Topology amalgamation	Dual-mode nested	Double-sided bias	Self-adapting feedback bias
Matching Network	No	No	No	No	No	No
No. of Stages, N	1	3	2+1	1	1	1
Load, R_{LOAD}	50 kΩ	100 kΩ	100 kΩ	100 kΩ	100 kΩ	100 kΩ
PCE_{PEAK} (%) @ P_{IN} (dBm)	72.1% @ −18 dBm	47.91% @ −14 dBm	79.8% @ −17.5 dBm	80% @ −25 dBm [a]	66% @ −18.8 dBm [a]	65% @ −20.9 dBm [a]
Sensitivity (dBm) @ R_{LOAD} (kΩ) for V_{OUT} = 1 V	−14.9 @ 50 kΩ −16.3 @100 kΩ −20.8 @ 1 MΩ	−14 @ 50 kΩ −16 @ 100 kΩ −21 @ 1 MΩ	−15.5 @ 100 kΩ	−14.9 @ 100 kΩ	−16.2 @ 50 kΩ [a] −18.2 @ 100 kΩ	−18 @ 100 kΩ
P_{IN} Range (dB), PR1 @ $PCE >$ $0.8xPCE_{PEAK}$	11.5	12 [a]	7 [a]	6.5	7 [a]	9.5 [a]
P_{IN} Range (dB), PR2 @ $PCE > 20\%$	17	22.8	21	Not reported	14.5 [a]	17 [a]
Area (mm^2)	0.0175	0.18	0.023	0.00648	0.0088	0.105

[a] Estimated from publication's figures. # Simulation results. * Measurement was performed at 433 MHz.

4. Conclusions

This paper presents a switchable polarity bias scheme that enhanced the P_{IN} dynamic range of a differential CMOS rectifier. It achieves a PCE_{PEAK} of 72.1% and a P_{IN} dynamic range of 11.5 dB for $PCE > 0.8xPCE_{PEAK}$ for R_{LOAD} = 50 kΩ. The P_{IN} dynamic range enhancement is achieved by producing different polarity biasing to adapt the overdrive voltage at the n-MOS: positive during low P_{IN} and negative during high P_{IN}. The switching of the polarity changes the optimal operating condition of the rectifier, thereby resulting in two distinct *PCE* peaks. Having two *PCE* peaks from a single rectifier is desirable as multiple rectifiers are commonly used in literature to address the different P_{IN} domains. The switchover is performed with an auxiliary low-power comparator to monitor the V_{OUT} and compare it with a V_{REF} to trigger a V_{MODE} signal. The control signal V_{MODE} is simple compared to other similar adaptive bias which requires extensive control circuits to generate a continuous analog bias on the gate terminal of the n-MOS. The mode pin allows trimming to be performed externally or adjusted by the control of the cascading DC–DC boost converter in an IoT application. The p-MOS is also biased positively during high P_{IN} to reduce the reverse conduction loss. The proposed rectifier is implemented in a 40 nm

process node operating at 900 MHz. The proposed rectifier has an improved dynamic range PR1 of 11.5 dB while maintaining a *PCE* above 80% of its PCE_{PEAK} despite having a simpler implementation compared with other state-of-the-art rectifiers.

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