

Article

LC Tank Oscillator Based on New Negative Resistor in FDSOI Technology

Yuqing Mao, Yoann Charlon, Yves Leduc and Gilles Jacquemod *

Polytech'Lab, Université Côte d'Azur, UPR UniCA 7498, 06903 Sophia Antipolis, France;
yuqing.mao@etu.unice.fr (Y.M.); yoann.charlon@unice.fr (Y.C.); yves.leduc.be@gmail.com (Y.L.)

* Correspondence: gilles.jacquemod@unice.fr

Abstract: Although Moore's Law reaches its limits, it has never applied to analog and RF circuits. For example, due to the short channel effect (SCE), drain-induced barrier lowering (DIBL), and sub-threshold slope (SS). . . , longer transistors are required to implement analog cells. From 22 nm CMOS technology and beyond, for reasons of variability, the channel of the transistors has no longer been doped. Two technologies then emerged: FinFET transistors for digital applications and UTBB FDSOI transistors, suitable for analog and mixed applications. In a previous paper, a new topology was proposed utilizing some advantages of the FDSOI technology. Thanks to this technology, a novel cross-coupled back-gate (BG) technique was implemented to improve analog and mixed signal cells in order to reduce the surface of the integrated circuit. This technique was applied to a current mirror to reduce the small channel effect and to provide high-output impedance. It was demonstrated that it is possible to overcompensate the SCE and DIBL effects and to create a negative output resistor. This paper presents a new LC tank oscillator based on this current mirror functioning as a negative resistor.

Keywords: LC tank oscillator; SCE and DIBL; current mirror; negative resistor; FDSOI technology



Citation: Mao, Y.; Charlon, Y.; Leduc, Y.; Jacquemod, G. LC Tank Oscillator Based on New Negative Resistor in FDSOI Technology. *J. Low Power Electron. Appl.* **2024**, *14*, 8. <https://doi.org/10.3390/jlpea14010008>

Academic Editor: Alex Yakovlev

Received: 27 November 2023

Revised: 12 January 2024

Accepted: 22 January 2024

Published: 1 February 2024



Copyright: © 2024 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (<https://creativecommons.org/licenses/by/4.0/>).

1. Introduction

The demand for highly efficient and reliable radio frequency (RF) oscillators has grown rapidly with the proliferation of wireless communication systems. Among various oscillator topologies, LC tank oscillators have been widely used due to their simplicity, low cost, and high Q resonance [1]. However, the performance of conventional LC oscillators is limited by the parasitic resistance of inductors and capacitors, which reduces the quality factor (Q) and increases the power consumption.

To address these issues, negative resistance elements have been employed in LC tank oscillators to compensate for the parasitic losses and enhance the feedback loop gain [2]. Negative resistance is a type of impedance that decreases with increasing voltage or current. Negative resistance devices can increase gain and feed it back into the oscillator circuit, effectively increasing the gain and sustaining the oscillations. Phase noise (PN) and power consumption are the most important characteristics of oscillators. To achieve the specifications of telecommunication standards, particularly in terms of PN, the most popular LC tank VCO (voltage-controlled oscillator) is based on a differential cross-coupled structure to compensate the losses of the LC tank [3,4]. In this paper, we propose a new structure based on the advantages of the FDSOI technology.

Thanks to Moore's Law, the increase in performance in microelectronics technology, continuous for more than 50 years, is made possible by the miniaturization of the MOS transistors [5]. However, this law has never applied to analog and RF circuits. For example, due to the short channel effect (SCE), drain-induced barrier lowering (DIBL), and sub-threshold slope (SS). . . , longer transistors are required, especially for analog cells, as shown in Figure 1 [6].

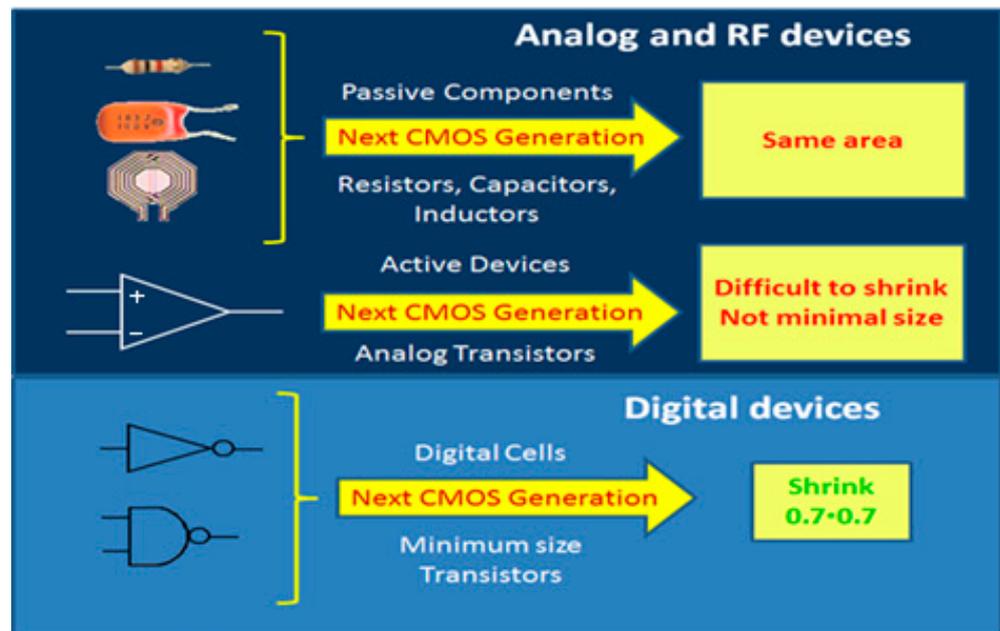


Figure 1. Limitations of the Moore Law for analog circuits.

To address these limitations while reducing the size of the transistors, several mainstream advanced technologies have emerged. For example, junctionless dual-gate MOSFETs have good noise performance in small sizes [7,8], and short channel effects can be suppressed by the formation of ultra-thin fin in FinFET devices [9], etc.

In addition, the efficient back-gate biasing provided by the FDSOI MOS transistor is being proposed in this paper as a means to compensate for SCE and DIBL effects. However, the output current is very sensitive to the channel length using the new topology. Finally, it was demonstrated that it is possible to overcompensate the SCE and DIBL effects and to introduce a negative output resistor. The focus of this paper is the LC tank oscillator based on this current mirror functioning as a negative resistor.

In Section 2, a short summary of FDSOI technology is presented, with a focus on the transistor back-gate. Section 3 covers the principle of a basic current mirror and its limits for short-channel-length transistors. The section demonstrates how FDSOI technology can help reduce these limitations. Section 4 describes the implementation of a negative resistor to compensate for the losses of an LC resonator in order to achieve an oscillator. This paper concludes with a summary of the findings.

2. FDSOI Technology

FDSOI technology is based on a thin layer of silicon that is on a buried oxide (Box). Called Ultra-Thin Body and Box (UTBB), FDSOI transistors are embedded in the fully depleted thin silicon layer and therefore offer unique bulk advantages. FDSOI technology claims better power and performance than its bulk counterpart [10]. FDSOI transistors correspond to a simple evolution of the conventional MOS transistor, as shown in Figure 2.

This technology is perfectly adapted to analog, RF, and mixed circuits design. By gaining a comprehensive understanding of FDSOI technology, we can appreciate its benefits as shown in Figure 3 in low-voltage, analog, and RF applications [11]. Specifically, FDSOI offers a substantial reduction in the Pelgrom coefficient (AV_t) [12] mismatch factor when compared to other technologies such as 28 nm LP bulk technology. This in turn allows for excellent analog performance while minimizing power consumption.

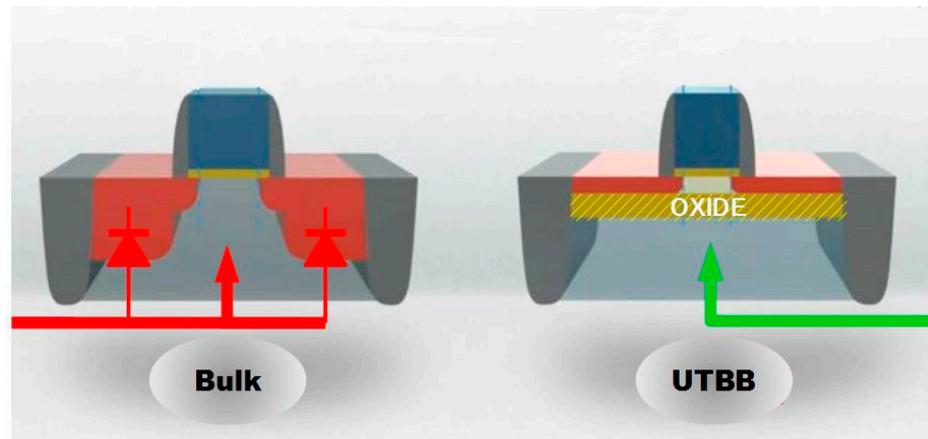
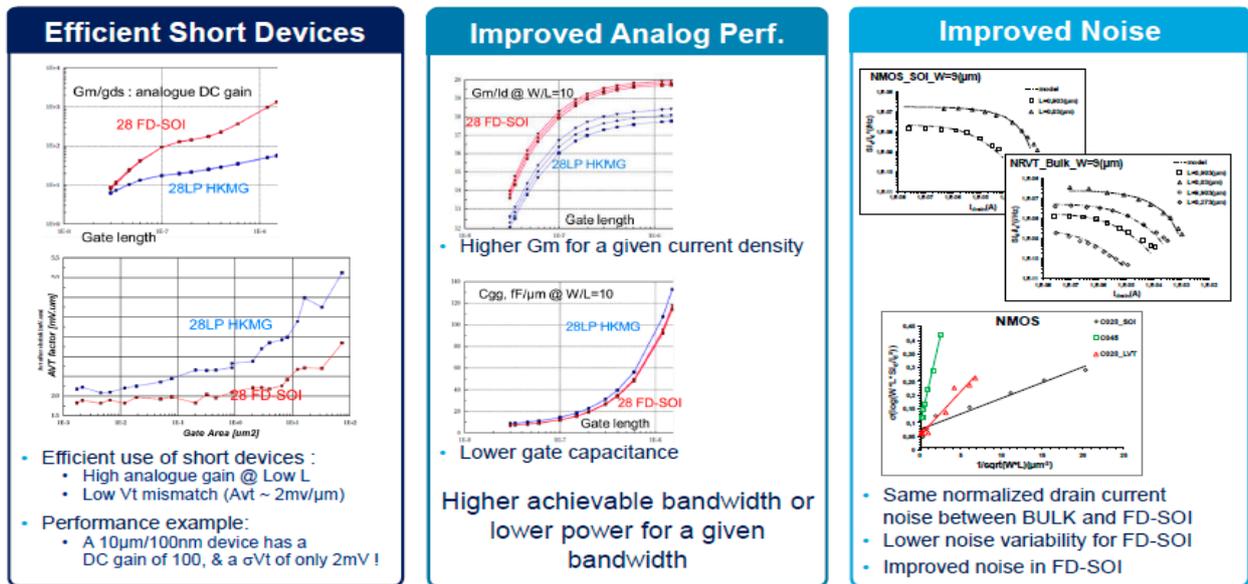


Figure 2. From bulk to UTBB MOS transistor.



Courtesy, L. Vogt, F. Paillardet, C. Charbuillet, P. Scheer, STMicroelectronics

Figure 3. Advantages of FDSOI technology for analog design [11].

One of the main features of this technology is the possibility to bias the back-gate electrode of the transistors in order to modify its threshold voltage, V_{Th} . Figure 4 presents the back-gate (BG) contact of such a transistor, and Figure 5 depicts the measured influence of the BG biasing on the V_{Th} variation [13]. Compared to conventional transistors, in FDSOI technology, the value of V_{Th} can be effectively reduced by BG biasing.

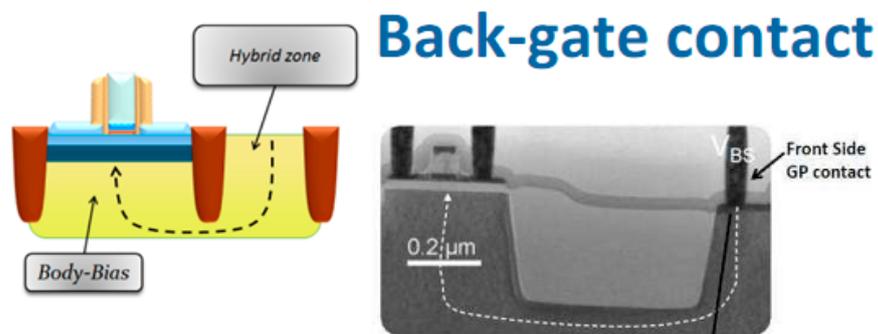


Figure 4. Illustration of the back-gate biasing.

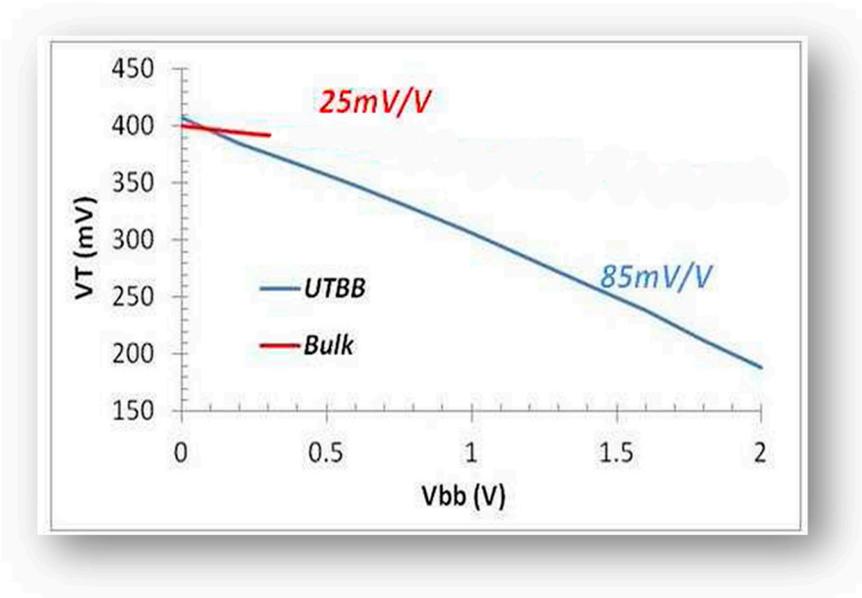


Figure 5. V_{Th} variation versus bulk or back-gate biasing [13].

In the following sections, all simulations are realized using Cadence framework and the PDK (process design kit) of the STMicroelectronics 28 nm FDSOI technology.

3. Current Mirror

3.1. Classical Design

A current mirror is a circuit that duplicates the current flowing through an active device by regulating the current in another active device, thus maintaining a stable output current regardless of the load [14]. Figure 6 depicts a basic current mirror employing bulk NMOS transistors.

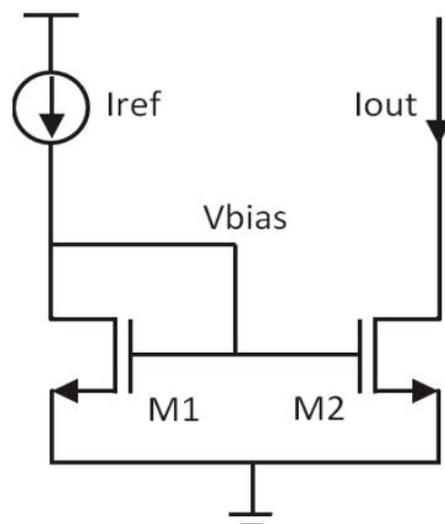


Figure 6. Basic current mirror.

Neglecting the channel length modulation, the I_{ref}/I_{out} ratio is equal to the size ratio of the two transistors, given by the well-known Equation (1).

$$\frac{I_{out}}{I_{ref}} = \frac{(W/L)_2}{(W/L)_1} \tag{1}$$

The existence of the ideal situation is precluded by channel length modulation [15], which is characterized by the channel length modulation coefficient λ that varies with the size of the length. As a result, the current is copied incorrectly, especially when the transistors are shortened. Then, the two currents, I_{ref} and I_{out} , are given by Equations (2) and (3).

$$I_{ref} = \frac{1}{2} \mu_n C_{OX} \left(\frac{W}{L} \right)_1 (V_{gs} - V_{thn})^2 (1 + \lambda V_{ds1}) \tag{2}$$

$$I_{out} = \frac{1}{2} \mu_n C_{OX} \left(\frac{W}{L} \right)_2 (V_{gs} - V_{thn})^2 (1 + \lambda V_{ds2}) \tag{3}$$

With the same V_{gs} , the ratio becomes:

$$\frac{I_{out}}{I_{ref}} = \frac{(W/L)_2 (1 + \lambda V_{ds2})}{(W/L)_1 (1 + \lambda V_{ds1})} \tag{4}$$

Accordingly, the current copy depends on both the ratio of transistor sizes and V_{ds1} and V_{ds2} , which may not be equal. This mismatch is worsened under short channel conditions with large λ . Several current mirror structures have been developed to reduce the short channel effect, such as the cascode current mirror and Wilson current mirror. These structures enforce equal V_{ds} for the two transistors to ensure uniform channel modulation. However, cascoded types of the basic current mirror (such as Wilson or Widlar topologies) are not feasible for low power supply voltages such as 1 V, as they reduce voltage margin or increase power consumption.

3.2. New Mirror Current Topology Using FDSOI Technology

Our proposed novel solution involves dynamically biasing the back-gate of FDSOI transistors to counteract the short channel effect, even when V_{ds} is not the same [6]. This approach can be applied to the basic current mirror depicted in Figure 6 by configuring the back-gates of FDSOI transistors, as shown in Figure 7.

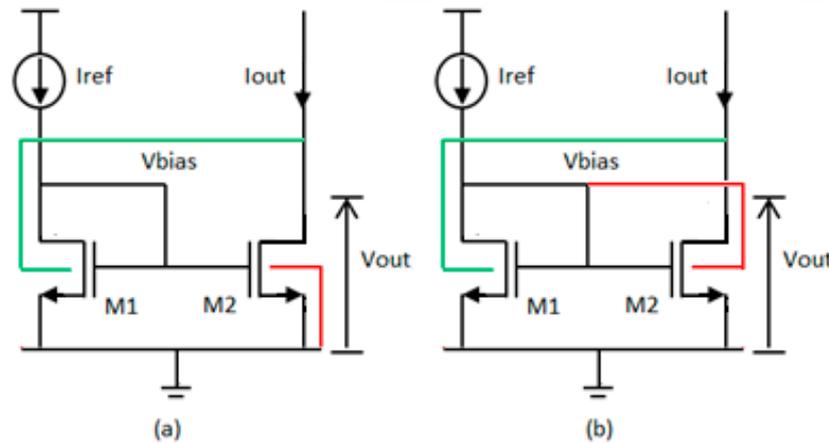


Figure 7. Basic current mirrors with two different back-gate configurations: (a) with one back-gate control and (b) two calibrated back-gate control.

In fact, reducing the slope of I_{ds} in the saturation region can be achieved by biasing the back-gate voltage. Figure 7a depicts the connection of V_{out} to the back-gate of M1. With this setup, the back-gate voltage of M1 tracks the drain voltage of M2, which varies from 0 to 1 V. As the back-gate voltage rises, the threshold voltage drops, leading to a reduction in the biasing voltage (V_{gs}) required to maintain the same source current (cf. Equation (2)). Consequently, the slope of the output current can be controlled, and it can become horizontal or negative based on the lengths of the transistors.

Additionally, the drain voltage of M1 can be leveraged to control the back-gate voltage of M2, as illustrated in Figure 7b. Here, instead of connecting the back-gate of transistor M2 to the ground, it is linked to the drain voltage of M1 to lower the threshold voltage for M2, resulting in an increase in the output current (cf. Equation (3)). The simulations presented below operate in the moderate region by setting a small reference current (such as 1 μA).

In this paper, the PDK used is CMOS28 FDSOI 1.5.a provided by STMicroelectronics. Additionally, the PMOS and NMOS used are lvtpfettw and nfettw from the cmos32lp library, respectively, which take advantage of having a triple-well structure. By setting the correct voltage in each well and substrate, one back-gate can be utilized to control the subtract voltage without any short circuit or leakage issues, thanks to the equivalent two-diode structure [15]. Figure 8 shows simulation results of a basic current mirror with different back-gate configurations, using small transistors ($W_N/L_N = 80\text{ nm}/33\text{ nm}$) to focus on the short channel effect. The output current (I_{out}) exhibits an exponential relationship within the moderate region (red curve) when the back-gate of each transistor is biased to the ground, similar to a classical bulk transistor. This reveals that the basic current mirror without back-gate control experiences a significant mismatch between the reference current and the output current.

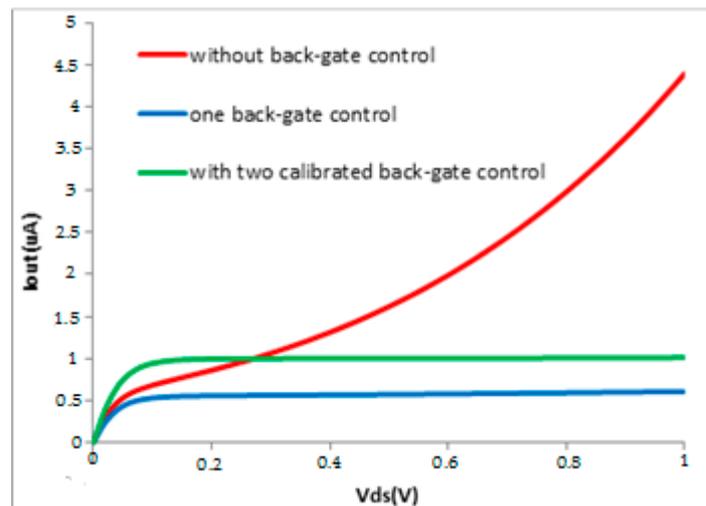


Figure 8. Comparison with different back-gate configurations.

By calculating an optimized size, the back-gate of M1 can be controlled with the drain voltage of M2 and compensate for the short channel effect by decreasing V_{bias} (blue curve, cf. configuration Figure 7a). Moreover, connecting both back-gates of the two transistors to the drain voltages can result in an output current that increases up to the reference current of 1 μA , as illustrated by the green curve (cf. configuration Figure 7b).

In simulations (cf. Figure 8), the NMOS transistor width and length were fixed at 80 nm and 33 nm, respectively, to reduce gaps between the reference and output currents. Varying the transistor lengths enables manipulation of g_{ds} and g_{mb} values. Finally, a transistor length of 35 nm, along with a fixed width of 100 μm , was found to be optimal for compensating g_{ds} by g_{mb} , with higher reference currents.

3.3. Implementation and Measurements

The construction of both types of current mirrors was carried out using UTBB-FDSOI PMOS transistors, as shown in Figure 9. The back-gate of each transistor was connected to V_{DD} in the absence of back-gate control.

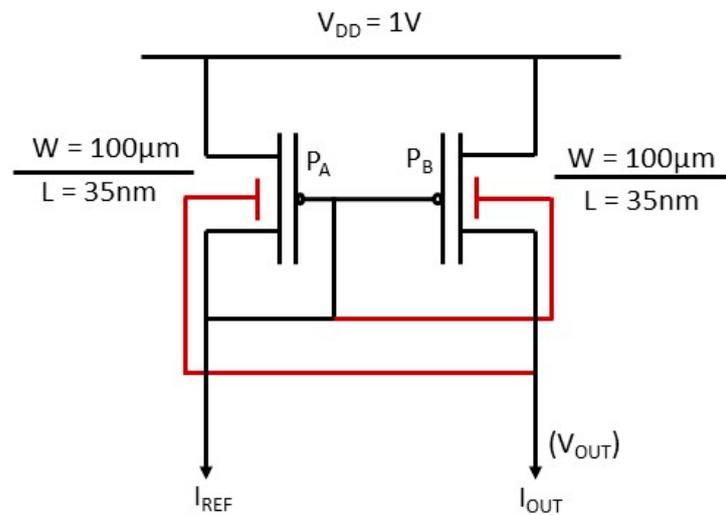


Figure 9. Implemented structure where the red wires correspond to the back-gate control.

First, the length of the output transistor (P_B) has to be optimized. In order to achieve this more efficient length value, a series of DC simulations was conducted. In Figure 10, only three simulation results were presented with three different values of L (34 nm, 35 nm, and 36 nm) while maintaining a constant width of $W = 100 \mu\text{m}$, where $I_{REF} = 45 \mu\text{A}$. The results indicate that the output current of the current mirror is highly dependent on the transistor length and is very sensitive. The optimal transistor length was found by the simulation to be 35 nm, as deviations from this length resulted in either undercompensation (for $L = 34 \text{ nm}$) or overcompensation (for $L = 36 \text{ nm}$).

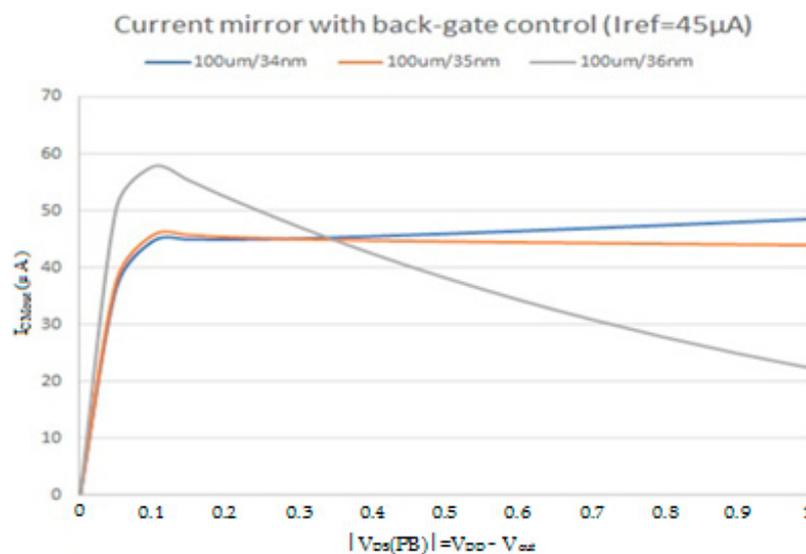


Figure 10. Simulations of a current mirror with BG control for different lengths of the output transistor.

The two configurations, with and without back-gate control (in the case of without, the back-gate of the two PMOS transistors is connected to $V_{DD} = 1 \text{ V}$), have been implemented in 28 nm FDSOI technology. The layout is depicted in Figure 11 and has a size of $30 \times 40 \mu\text{m}^2$ under the implementation of 28 nm FDSOI technology by STM. Finally, simulations and measurements are compared as shown in Figures 12 and 13.

The experiment involved testing the current mirror with three different current values ($I_{REF} = 45, 90, \text{ or } 180 \mu\text{A}$) and comparing the results with and without back-gate control. Both configurations with the optimal L value (35 nm) have the same size of transistors. In Figures 12 and 13, measurements and simulations (solid and dotted lines, respectively)

show good agreement in the saturation regions, despite slightly different saturation voltage values (0.1 V for simulation and a higher value for measurement). To our knowledge, we have not found an answer to explain this phenomenon to date. Therefore, it can be concluded that the cross-coupled back-gate auto-biasing technique effectively stabilizes the current in the saturation region at values of 45, 90, and 180 μA , respectively.

As demonstrated in simulation, Figure 12 shows that this topology is very sensitive to the length of the transistor. The overcompensation of the SCE effect is a little bit highlighted in measurement where a small negative resistance appears in the saturation region (especially for higher currents, i.e., $I_{\text{REF}} = 180 \mu\text{A}$). If this sensitivity can be a problem for the realization of a current mirror, it is not the case if we really want to realize a negative resistor, as described in Section 4.

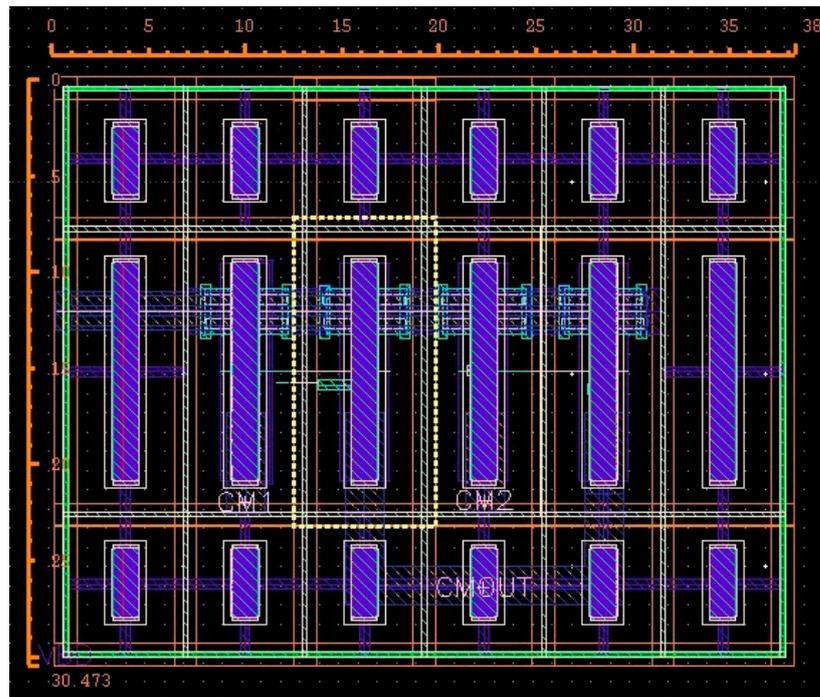


Figure 11. Layout of the two current mirrors.

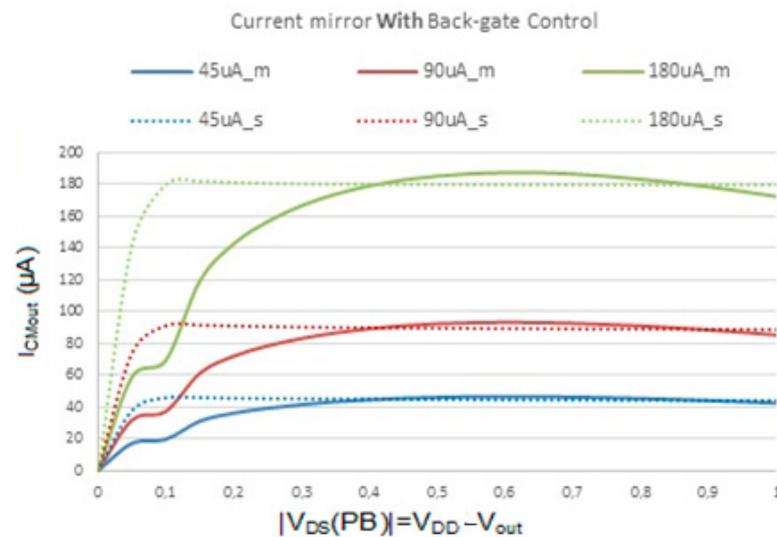


Figure 12. Comparison between measurements and simulations with back-gate control.

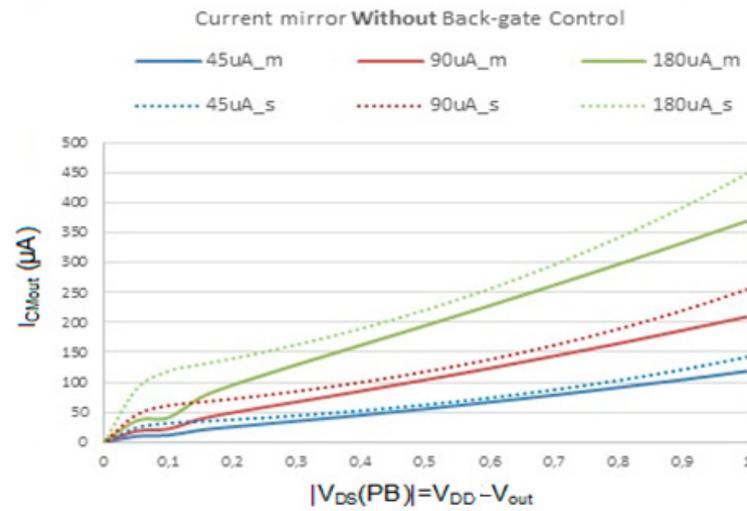


Figure 13. Comparison between measurements and simulations without back-gate control.

This auto-calibration back-gate technique has been also used to realize a low phase noise complementary ring oscillator [16]. The following section describes how to use this current mirror to realize a negative resistance through overcompensation of the SCE effects.

4. New LC Tank Oscillator

Thanks to the previous results, a negative resistance LC tank oscillator is proposed. The circuit is designed by transforming the current mirror circuit into a negative resistance circuit. The negative resistance is created by adjusting the length of the output transistor of the current mirror. To optimize the size of this output UTBB-PMOS transistor (P_B) and to achieve the desired negative resistance, several simulations were conducted. We performed DC simulations to explore the behavior of the negative resistance circuit across varying reference current magnitudes. Figure 14 showcases the simulation outcomes corresponding to a reference current of 1 mA. These simulations were conducted considering an incremental elongation of transistor length (L) from 30 nm to 100 nm (by step of 10 nm), displayed sequentially from top to bottom.

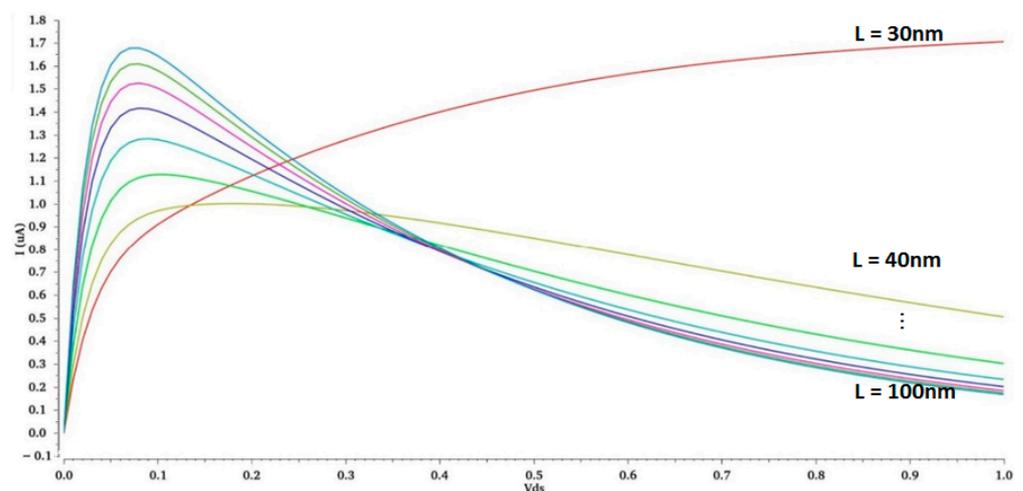


Figure 14. Simulation results for different lengths of the transistor with 1 mA.

As expected, for a value of L greater than 50 nm, the resistance value is not very sensitive to the variation of this length. Finally, a value of $L = 80$ nm was chosen for both transistors of the current mirror to realize a negative resistor.

To generate the input current, a UTBB-NMOS transistor was used, and the current was controlled by V_{BIAS} , as shown in Figure 15. The negative resistance circuit was connected in parallel with the oscillation circuit, enabling continuous oscillation. The oscillation frequency was determined by the values of the inductor and capacitor in the LC tank circuit.

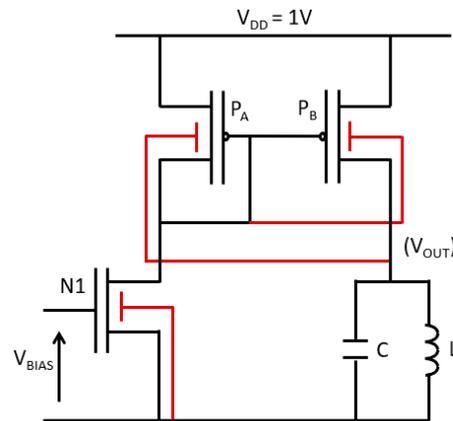


Figure 15. LC tank oscillator based on new negative resistor where the red wires correspond to the back-gate biasing for each transistor.

The circuit’s resonance frequency of 2.45 GHz was achieved by selecting the appropriate values for the inductor and capacitor. Specifically, an inductor value of 1 nH and a capacitor value of 4.2 pF were selected, considering the relationship between the inductance, capacitance, and resonance frequency given by:

$$f_0 = \frac{1}{2\pi\sqrt{LC}} = 2.45 \text{ GHz} \tag{5}$$

To evaluate the transient and phase noise performance of the circuit at different values of V_{BIAS} , several extensive simulations were performed. The impact of different V_{BIAS} values on the circuit’s performance was the main focus. To realize more accurate simulations, the series resistance of the inductor was taken into account, which is depicted in Figure 16.

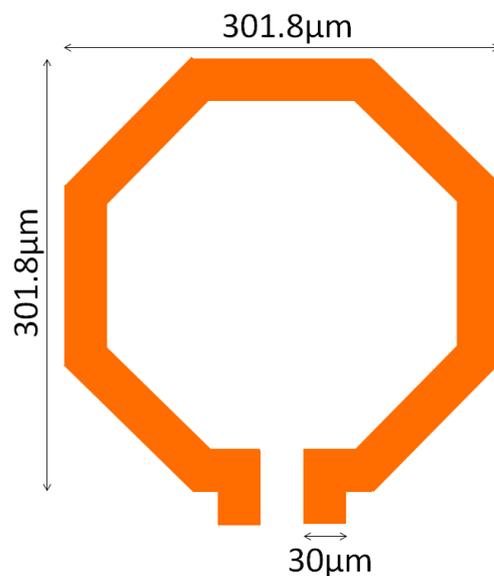


Figure 16. Layout of the 1 nH inductor.

Thanks to the geometry of the inductor, it is considered that its length equals $8 \times (125 + 102)/2 = 908 \mu\text{m}$. The resistivity of the chosen metal layer is $6.6 \text{ m}\Omega$, so the series resistance is equal to $r = 908/30 \times 6.6 = 200 \text{ m}\Omega$. The equivalent parallel resistor is given by Equation (6).

$$R_{//} = \frac{L}{rC} = 1.2 \text{ k}\Omega \tag{6}$$

Thanks to this value, the quality factor of the LC tank equals $Q = 2\pi RCf_0 = 77$. To verify these values, the impedance of the LC tank was simulated, including the series resistor $r = 200 \text{ m}\Omega$. The frequency response result is depicted in Figure 17. The impedance initially increases and then decreases as the frequency increases, reaching its maximum value at the resonant frequency.

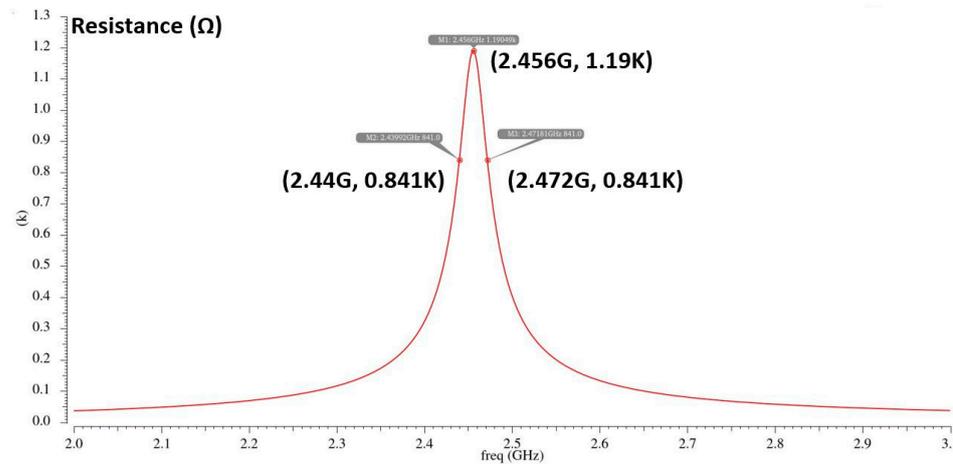


Figure 17. Impedance of the LC tank versus frequency.

At the resonance frequency ($f_0 = 2.45 \text{ GHz}$, cf. Figure 17), the simulated impedance equals $R_{//} = 1.2 \text{ k}\Omega$ as expected, and the bandwidth (for $Z = 850 \Omega$) is $2472 - 2440 = 32 \text{ MHz}$, so the quality factor is given by $Q = 2455/32 = 76$.

The goal is now to realize a negative resistor that has to compensate for $R_{//}$. The size W/L of P_A and P_B and the minimum value of I_{REF} (generated by N_1 through V_{BIAS}) need to be determined. First, $W = 100 \mu\text{m}$ was chosen to achieve some values of I_{REF} higher than a few mA. By adjusting in simulation the size of L from 30 nm to 120 nm to perform a negative resistor, the slope of the circuit, $|I_{OUT}/V_{DS}|$, exhibits a non-linear trend, initially increasing and then decreasing until reaching its peak at approximately $L = 80 \text{ nm}$. Notably, the output signal demonstrates its maximal amplitude and shortest response time when L is set to 80 nm . Finally, to determine the minimum value of I_{REF} for the oscillation's start, an ideal current generator was used to replace N_1 . The simulation results exhibit a value of $I_{REFmin} = 2.3 \text{ mA}$. To achieve this current with a low value of V_{BIAS} (0.5 V for example), the size of N_1 is $W/L = 30 \mu\text{m}/30 \text{ nm}$. Figure 18 gives the different sizes of the components.

The results of the different transient and phase noise simulations are summarized in Table 1. In fact, for these simulations, an ideal current generator was kept instead of transistor N_1 . These results show that the oscillation frequency is quite stable and the best compromise between settling time, power consumption (cf. I_{REF}), and phase noise is achieved for $I_{REF} = 5.0 \text{ mA}$ (i.e., $V_{BIAS} = 0.6 \text{ V}$). Depending on the application, it is possible to adjust the phase noise to power consumption ratio while maintaining the same frequency resonance.

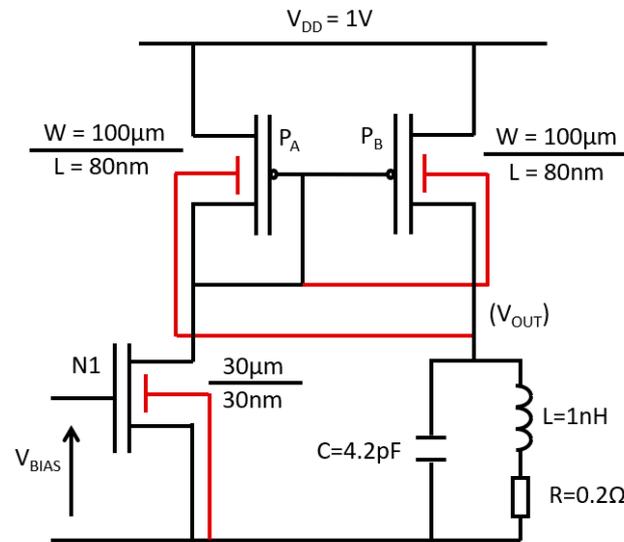
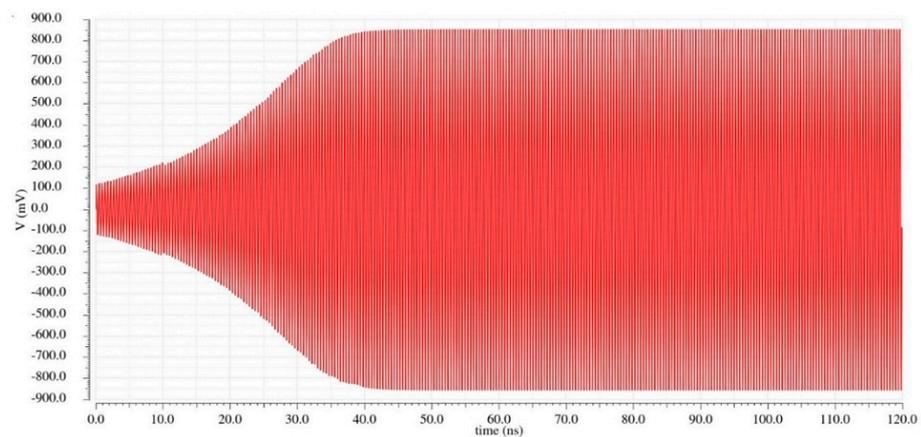


Figure 18. Sizing of the LC tank oscillator (The red wires correspond to the back-gate biasing of each transistor).

Table 1. Performances for different values of V_{BIAS} .

V_{BIAS} (V)	I_{REF} (mA)	Settling Time (ns)	f_{osc} (GHz)	PN (dBc/Hz @1 MHz)
0.1–0.4			No oscillation	
0.5	2.3	80	2.38	−113
0.6	5.0	45	2.37	−114
0.7	7.4	30	2.36	−112
0.8	8.8	26	2.36	−111
0.9	9.6	25	2.36	−111
1.0	10.1	25	2.36	−111

Figures 19 and 20 illustrate, respectively, the transient simulation and phase noise characteristics of the circuit when I_{REF} was set to 5.0 mA ($V_{BIAS} = 0.6$ V). In Figure 19a, the periodic output signal is displayed, with a settling time equal to 45 ns. In Figure 19b, the oscillation signal is scaled up to measure the oscillation frequency, which is found to be 2.37 GHz.



(a)

Figure 19. Cont.

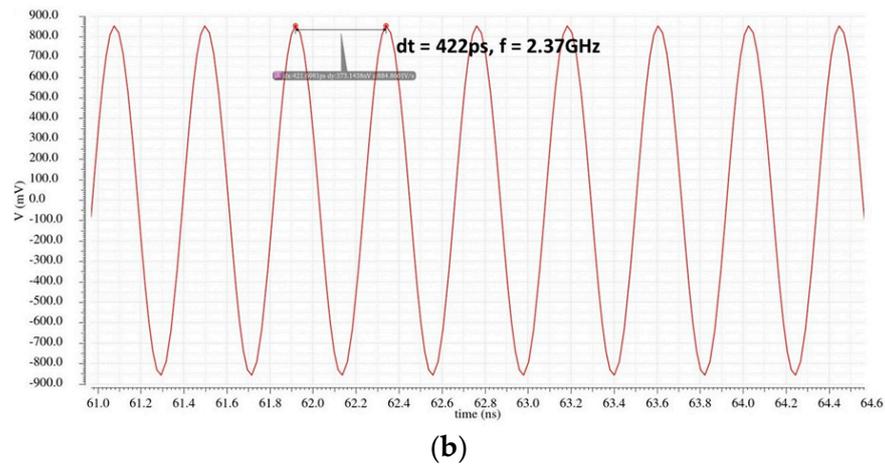


Figure 19. Transient simulations: (a) settling time and (b) steady state.

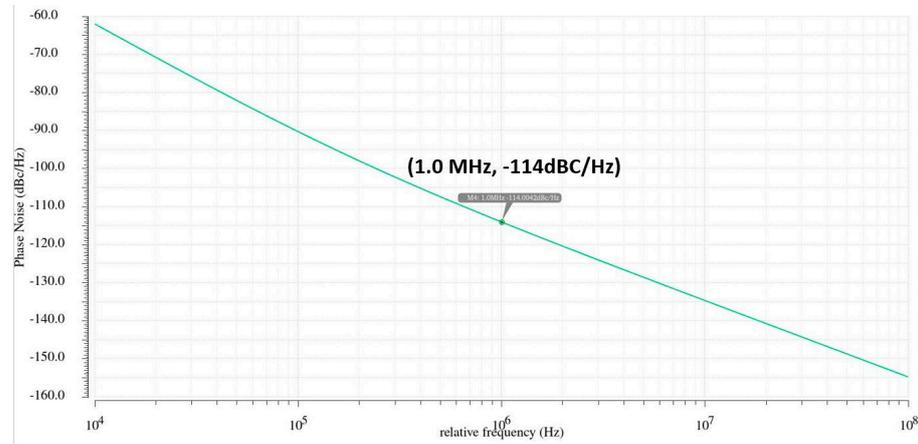


Figure 20. Phase noise simulation with $V_{BIAS} = 0.6$ V.

The power-delay product (PDP) of this oscillator was calculated using Equation (7) [17], which is 3.86 fJ. The phase noise is -114 dBc/Hz @1 MHz, as shown in Figure 20.

$$PDP (fJ) = \frac{\text{power (mW)}}{\text{maximum frequency (GHz)}} \tag{7}$$

Then, the total output capacitance of the current mirror was extracted, which is very close to $C_{DS}(P_B)$. This value equals $C_{out} = 0.3$ pF. The total capacitance of the LC tank is $C_T = 4.2 + 0.3 = 4.5$ pF, giving a resonance frequency $f_0 = 2.37$ GHz, as found in the simulation.

5. Comparison with Classical LC Tank VCO

Due to its performance in terms of phase noise, the most popular LC tank VCO is based on a differential cross-coupled structure to realize the negative resistor, as depicted in Figure 21 [18]. However, the tail current transistor, M_T in Figure 21, is one of the biggest noise contributors of this structure [19]. Different techniques to reduce this noise have been proposed, such as sinusoidal tail current shaping [20], tail current flicker noise reduction by complementary switched biasing [21], sinusoidal shaping of the ISF [22], novel tail current noise second harmonic filtering [23], . . . A significant and interesting contribution was proposed in 2007 [24] using SOI technology. In fact, the technology was PD (partially depleted) SOI, which allows to suppress the tail current transistor. The biasing current is directly modulated by the body voltage of the differential cross-coupled transistor pair, as depicted in Figure 22. More recent results have been published using FinFET or FDSOI

technology [25–27]. Table 2 provides a comparison of LC tank performance with these latest works. The FOMs of the different circuits are quite similar, but this work exhibits a better phase noise with higher power consumption. The FOM is given by relation (8).

$$FOM = -L(f_m) + 20 \log\left(\frac{f_0}{f_m}\right) - 10 \log\left(\frac{P_{DC}}{1mW}\right) \quad (8)$$

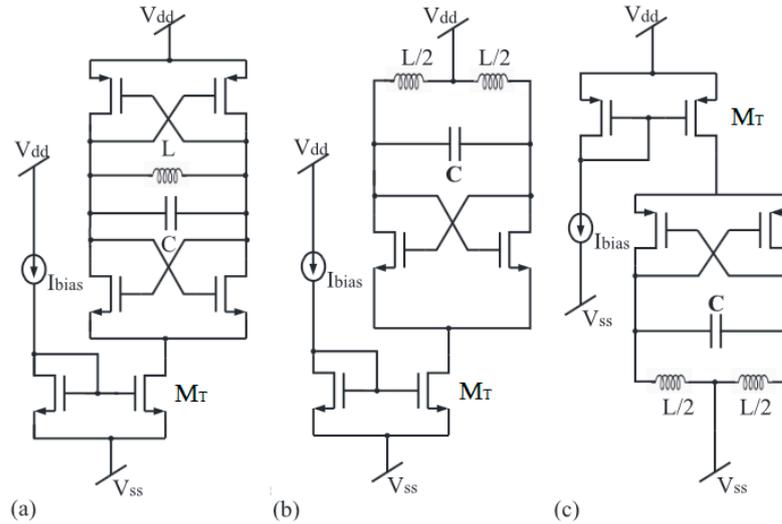


Figure 21. Differential cross-coupled LC oscillator: (a) CMOS, (b) NMOS, (c) PMOS [13].

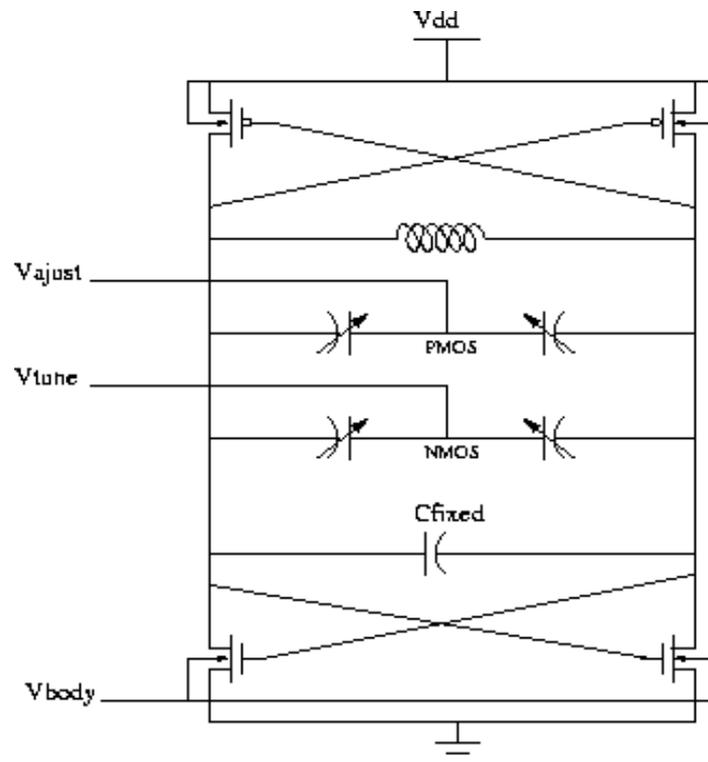


Figure 22. LC oscillator in PDSOI technology with body voltage control.

Table 2. LC tank performance summary and comparison.

Reference	[25]	[26]	[27]	This Work
Technology (nm)	22 FinFET	28 BULK	22 FDSOI	28 FDSOI
Supply Voltage (V)	0.85	0.35	0.8	1
f_{osc} (GHz)	16	2.4	24	2.4
PN@1 MHz (dBc/Hz)	−98	−110	−93	−114
Power Dissipation (mW)	5.94	1.3	20	9.26
FOM (dB)	174	176	168	172
Simulation or measurement results	Measurement	Measurement	Simulation	Simulation

These results show that our structure is more or less at the state of the art with a better phase noise and a simpler design, so with a very low-silicon area. Other comparisons between LC tank and RTW VCOs or LC tank and Ring VCOs can be found, respectively, in [28,29]. Moreover, another LC tank design in 22 nm technology is depicted in [30]. This paper, dedicated to SEU mitigation, also gives a comparison with two other published results.

6. Conclusions

In this paper, a novel back-gate control technique using UTBB-FDSOI transistors was presented that effectively reduces the SCE and DIBL effects in analog cells. By reducing these effects, it is able to decrease the size of the analog cells while maintaining their performance and reliability. Furthermore, it has been demonstrated that overcompensating the SCE and DIBL effects can create a negative resistor circuit, which was utilized to design and implement a negative resistance for the LC tank oscillator. According to our simulations, the LC tank oscillator exhibits stable oscillations at a frequency of 2.4 GHz with an optimal length of 80 nm (for $W = 100 \mu\text{m}$), while maintaining a low phase noise of $-114 \text{ dBc/Hz @1 MHz}$ at a V_{BIAS} of 0.6 V.

These first results mainly served as proof of concept of this new topology; however, it is possible to improve the performance of this circuit. It is thus possible to reduce the total consumption of this circuit by a factor of 2 by modifying the size of transistors N1 and P_A (cf. Figure 18). Therefore, if we divide the width of these two transistors by a factor of 10 (i.e., $W_{N1} = 3 \mu\text{m}$ instead of $30 \mu\text{m}$ and $W_{PA} = 10 \mu\text{m}$ instead of $100 \mu\text{m}$), the current I_{REF} is only 0.5 mA while the current in the output transistor (P_B) remains at 5 mA for $V_{BIAS} = 0.6 \text{ V}$. This modification does not change the output current or the negative value of the equivalent resistance but allows the total consumption to be reduced to 5.1 mW instead of 9.26 mW. This modification also allows the size of the final integrated circuit to be reduced.

Finally, we can replace the capacitance C of the LC tank by an NMOS varactor in order to produce a VCO, which can be integrated into a PLL, for example, to realize a transceiver. In this regard, we can note that the performance of the final circuit will not be sensitive to technological variations of the transistors used. The value of the negative resistor depends little on the size of the P_B transistor if this length remains between 50 and 100 nm. We will conduct further studies, including process, voltage, and temperature (PVT) and Monte Carlo simulations, to fully evaluate the stability of the negative resistance and the performance of the LC VCO. However, it should be noted that this is more engineering work than research.

Author Contributions: Circuit idea, G.J. and Y.M.; circuit design, Y.M. and Y.C.; software, Y.M. and Y.C.; writing—original draft preparation, Y.M. and G.J.; writing—review and editing, Y.M., Y.C., Y.L. and G.J. All authors have read and agreed to the published version of the manuscript.

Funding: This research received no external funding with the exception of Mao’s thesis grant (supported by the China Scholarship Council for 3 years of study at the Université Côte d’Azur under Grant No. 202008070128).

Data Availability Statement: All data are available from the authors upon request.

Conflicts of Interest: The authors declare no conflicts of interest.

References

1. Samori, C.; Levantino, S.; Lacaita, A.L. Integrated LC oscillators for frequency synthesis in wireless applications. *IEEE Commun. Mag.* **2002**, *40*, 166–171. [[CrossRef](#)]
2. Ham, D.; Hajimiri, A. Concepts and methods in optimization of integrated LC VCOs. *IEEE J. Solid-State Circuits* **2001**, *36*, 896–909. [[CrossRef](#)]
3. Gurjar, R.; Mishra, D.K. Design and performance analysis of low phase noise LC-voltage controlled oscillator. *TELKOMNIKA Telecommun. Comput. Electron. Control* **2023**, *21*, 872–880. [[CrossRef](#)]
4. Vosta, P.K.; Miar-Naimi, H.; Javadi, M. Comprehensive analysis of LC cross-coupled oscillator with active and passive transconductance amplification structure. *Analog Integr. Circuits Signal Process.* **2023**, *115*, 21–31. [[CrossRef](#)]
5. Moore, G. Cramming more components onto integrated circuits. *Electron. Mag.* **1965**, *38*, 114. [[CrossRef](#)]
6. Wei, Z.; Jacquemod, G.; Leduc, Y.; de Foucauld, E.; Prouvee, J.; Blampey, B. Reducing the short channel effect of transistors and reducing the size of analog circuits. *Act. Passiv. Electron. Compon.* **2019**, *2019*, 4578501. [[CrossRef](#)]
7. Kumar, K.; Raman, A.; Raj, B.; Singh, S.; Kumar, N. Design and optimization of junctionless-based devices with noise reduction for ultra-high frequency applications. *Appl. Phys. A* **2020**, *126*, 913. [[CrossRef](#)]
8. Mendiratta, N.; Tripathi, S.L. A review on performance comparison of advanced MOSFET structures below 45 nm technology node. *J. Semicond.* **2020**, *41*, 061401. [[CrossRef](#)]
9. Verma, S.; Tripathi, S.L.; Bassi, M. Performance Analysis of FinFET device Using Qualitative Approach for Low-Power applications. In *Devices for Integrated Circuit (DevIC), Kalyani, India*; IEEE: Piscataway, NJ, USA, 2019; pp. 84–88. [[CrossRef](#)]
10. Cathelin, A. Fully depleted silicon on insulator devices CMOS: The 28-nm node is the perfect technology for analog, RF, mmW, and mixed-signal system-on-chip integration. *IEEE Solid-State Circuits Mag.* **2017**, *9*, 18–26. [[CrossRef](#)]
11. Cathelin, A. *Advantages for Analog/RF & Mixed-Signal Designs*; SOI Consortium Forum: Tokyo, Japan, 2016; Available online: <https://www.semi.org/en/connect/events/fd-soi-and-rf-soi-forum-tokyo-japan-2016> (accessed on 26 November 2023).
12. Pelgrom, M.J.M.; Duinmaijer, A.C.J.; Welbers, A.P.G. Matching properties of MOS transistors. *IEEE J. Solid-State Circuits* **1989**, *24*, 1433–1439. [[CrossRef](#)]
13. Flatresse, P.; Wilson, R. *SOC Variability Reduction: The UTBB FD-SOI Way*; VARI: Darmstadt, Germany, 2013.
14. Toumazou, C.; Lidgley, F.; Haigh, D. *Analogue IC Design: The Current-Mode Approach*; The Institution of Engineering and Technology: London, UK, 1993; p. 666. ISBN 978-0863412974.
15. Wei, Z. Back-Gate Feedback for Auto-Calibration of Analog and Mixed Cells in UTBB-FDSOI Technology. Ph.D. Dissertation, Université Côte d’Azur, Côte d’Azur, France, 2019.
16. Jacquemod, G.; Wei, Z.; Leduc, Y.; de Foucauld, E.; Prouvee, J. New design of analog and mixed-signal cells using back-gate cross-coupled structure. In Proceedings of the 2019 IFIP/IEEE 27th International Conference on Very Large Scale Integration (VLSI-SoC), Cuzco, Peru, 6–9 October 2019.
17. Huq, S.M.I.; Baroi, O.L.; Shihab, S.A.; Biswas, S.N. Comparative Study and Design of Current Starved Ring Oscillators in 16 nm Technology. *IEEE Trans. Circuits Syst. II Express Briefs* **2021**, *68*, 1098–1102. [[CrossRef](#)]
18. Afacan, E.; Dundar, G. A comprehensive analysis on differential cross-coupled CMOS LC oscillators via multi-objective optimization. *Integration. VLSI J.* **2019**, *67*, 162–169. [[CrossRef](#)]
19. Hajimiri, A.; Lee, T.H. A general theory of Phase Noise in electrical oscillators. *IEEE J. Solid-State Circuits* **1998**, *33*, 174–194.
20. Jafari, B.; Sheikhaei, S. Phase noise reduction in LC cross coupled oscillators using sinusoidal tail current shaping technique. *Analog Integr. Circuits Signal Process.* **2018**, *96*, 125–132. [[CrossRef](#)]
21. Kassim, A.K.; Sharaf, K.; Ragaie, H. Tail current flicker noise reduction in LC VCOs by complementary switched biasing. In Proceedings of the IEEE 15th International Conference on Microelectronics, Cairo, Egypt, 11 December 2003; pp. 102–105.
22. Jannesari, A.; Kamarei, M. Sinusoidal shaping of the ISF in LC oscillators. *Int. J. Circuit Theory Appl.* **2008**, *36*, 757–768. [[CrossRef](#)]
23. Jafari, B.; Sheikhaei, S. Phase noise reduction in a CMOS LC cross coupled oscillator using a novel tail current noise second harmonic filtering technique. *Microelectron. J.* **2017**, *65*, 21–30. [[CrossRef](#)]
24. Geynet, L.; de Foucauld, E.; Vincent, P.; Jacquemod, G. Fully integrated dual-band VCOs with power controlled by body voltage in 130nm CMOS/SOI for multi-standard applications. *Analog Integr. Circuits Signal Process.* **2007**, *53*, 43–51. [[CrossRef](#)]
25. Dolt, D.; Livingston, Q.; Liu, T.; Kuma, A.; Palermo, S. SEE Sensitivity of a 16GHz LC-Tank VCO in a 22nm FinFET Technology. In Proceedings of the 2022 IEEE International Symposium on Circuits and Systems (ISCAS), Austin, TX, USA, 27 May 2022–1 June 2022; pp. 254–257. [[CrossRef](#)]
26. Chen, Y.; Babaie, M.; Staszewski, R.B. A 350-mV 2.4-GHz quadrature oscillator with nearly instantaneous start-up using series LC tanks. In Proceedings of the IEEE Asian Solid-State Circuits Conference (A-SSCC), Seoul, Republic of Korea, 6–8 November 2017; IEEE: Piscataway, NJ, USA, 2017; pp. 104–108. [[CrossRef](#)]
27. Hao, B.; Wang, Z.; Zhang, J.; Ma, M.; Wang, Y. A Low-Noise High-Robust LC-VCO Based on 22nm FD-SOI Process. In Proceedings of the 7th International Conference on Integrated Circuits and Microsystems (ICICM), Xi’an, China, 28–31 October 2022; IEEE: Piscataway, NJ, USA, 2022; pp. 166–170. [[CrossRef](#)]

28. Jacquemod, G.; Benabedjelil, F.; Tatinian, W.; Lucchi, P.; Borgarino, M.; Carpineto, L. Comparison between RTW VCO and LC QVCO 12GHz PLLs. *Analog Integr. Circuits Signal Process.* **2012**, *73*, 749–756. [[CrossRef](#)]
29. Monda, D.; Ciapri, G.; Mangraviti, G.; Berti, L.; Saporanara, S. Analysis and comparison of Ring and LC tank oscillators for 65nm integration of Rad-Hard VCO for SpaceFibre applications. In *Applications in Electronics Pervading Industry, Environment and Society*; Springer: Berlin/Heidelberg, Germany, 2019; pp. 25–32.
30. Dolt, D.; Kim, I.; Palermo, S. A comparison of 25-GHZ-LC-VCO circuit topologies for SEU mitigation in 22nm FinFET. In *Proceedings of the IEEE/MTT-S International Microwave Symposium, San Diego, CA, USA, 11–16 June 2023*; pp. 151–154.

Disclaimer/Publisher’s Note: The statements, opinions and data contained in all publications are solely those of the individual author(s) and contributor(s) and not of MDPI and/or the editor(s). MDPI and/or the editor(s) disclaim responsibility for any injury to people or property resulting from any ideas, methods, instructions or products referred to in the content.