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Editorial

Special Issue "Smart IC Design and Sensing Technologies"

George Floros * and Athanasios Tziouvaras

Department of Electrical and Computer Engineering, University of Thessaly, 38334 Volos, Greece
* Correspondence: gefloros@e-ce.uth.gr

Abstract: Smart sensing technologies and their inherent data-processing techniques have drawn considerable research and industrial attention in recent years. Recent developments in nanometer CMOS technologies have shown great potential to deal with the increasing demand of processing power that arises in these sensing technologies, from IoT applications to complicated medical devices. Moreover, circuit implementation, which could be based on a full analog or digital approach or, in most cases, on a mixed-signal approach, possesses a fundamental role in exploiting the full capabilities of sensing technologies. In addition, all circuit design methodologies include the optimization of several performance metrics, such as low power, low cost, small area, and high throughput, which impose critical challenges in the field of sensor design. This Special Issue aims to highlight advances in the development, modeling, simulation, and implementation of integrated circuits for sensing technologies, from the component level to complete sensing systems.

Keywords: VLSI design; integrated circuits; sensing technologies; circuit optimization methods; modeling and simulation; signal processing; CAD tools for smart IC design

Introduction

The latest advances in electronic circuits and sensing technologies indicate that there is a shift in interest to low power and energy efficient designs. On the electronic design side, several works focus on voltage regulation, timing speculation and near-data processing methodologies to achieve the envisioned energy-related goals. Authors in [1] propose a voltage regulation technique for IoT processors, under which the chip operates in near-threshold voltage values to decrease its energy consumption. In [2], the concept of an event-driven voltage regulator is introduced which manages the circuit power and trades power consumption with control latency by considering the slack and clock frequency. This approach is feasible since different instruction types depict distinct timing requirements, and thus the clock frequency of a circuit can be dynamically scaled accordingly to the instruction types occupying the pipeline [3]. Following this concept, the authors in [4] employ an architectural-oriented approach to combine near-data execution with a dynamic clock scaling mechanism. By employing a hybrid memory cube DRAM to execute instructions closer to the DRAM die and by leveraging the timing requirements of each instruction separately, the design manages to achieve significant efficiency levels. Recently, near-data instruction execution, also known as in-memory processing, is gaining ground since it achieves high performance and lower power consumption compared with the standard execution paradigm. On the other hand, near-data architectures require refined control logic in order to designate which instructions will execute on the DRAM side and which instructions will execute on the processor side [5]. Previous works in near-data processing depict significant improvements in the domains of IoT [6], big data applications [7] and machine learning [8].

Another popular approach is the adoption of application specific design which focus on the intricacies and requirements of specific application types. Contrary to the general-purpose approach, application specific designs are built to optimize their computation and functional characteristics with respect to application requirements. This design paradigm

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depicts significant gains on security [9], neural network [10], video processing [11] and signal processing [12] domains. The wide accessibility of the Field programmable gate arrays (FPGAs) to the research community is one of the key factors that led to the popularization of the application specific circuit designs. FPGAs are reconfigurable platforms which consist of programmable hardware cells that can adapt their circuit logic according to the application requirements. Today, FPGAs are used as prototypes and microcontroller for a wide range of applications such as radar systems [13], deep neural networks [14] and wireless communications [15].

As a result, digital signal processing algorithms are nowadays massively applied on IC designs for deep learning, computer vision, 5G/6G communications, automotive systems, health monitoring, and video processing applications. All of the above require an increased data rate [16] as well as low power consumption [17] techniques for an embedded environment. Frequently, computation-intensive signal processing algorithms need to be implemented in dedicated VLSI designs in order to be capable for real-time processing operations [18]. Therefore, due to strict power and performance requirements it is very challenging to realize different digital signal processing algorithms into efficient VLSI design [19]. Designers are required to meet several constraints on power consumption, clock rate, die area, cost, and reconfigurability while also achieving balanced trade-offs between the above characteristics [20,21].

In order to achieve this challenge designers, need to apply several CAD tool design methodologies [22]. IC optimization techniques and novel CAD tools are applied in parallel for the realization of efficient ICs and for reducing the resource consumption [23–25]. Another important issue is that dedicated CAD tool methodologies are required for a diverse range of applications, in which application specific designs are expected to be employed. For example, novel CAD tools need to be integrated into modern IC design flows for hardware security purposes [26], as well as, for long-term reliability and circuit aging factors [27,28], which are crucial for the automotive and the aeronautics industry. Finally, along with the different CAD tool methodologies, designers develop mathematical modeling and simulation techniques in order to gain insights for different IC and sensing designs [29,30], before these are applied in real world applications.

For the aforementioned reasons, a very strong effort is required by the IC design research community for proposing new efficient chips and CAD tools methodologies in order to deal with the increased demand of the industry. The final aim of this editorial and of the whole *Special Issue* is to stimulate and highlight the advancements in the development, modeling, simulation, and implementation of smart ICs for sensing technologies, from the component level to complete sensing systems, along with novel CAD tool design methodologies that will accompany the corresponding designs.

Conflicts of Interest: The authors declare no conflict of interest.

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