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Current Density-Voltage (J-V) Characterization of Monolithic Nanolaminate Capacitors †

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Abstract: In a world of miniaturized electronics, there is a rapidly increasing need for reliable, efficient, and compact energy storage systems with low-loss dielectrics. To address this need, this work proposes the development of compact, micro-capacitive energy storage devices compatible with IC processing so that they can be integrated monolithically on-chip. There are two main approaches to the fabrication of integrated on-chip micro-supercapacitor energy storage devices: interdigitated electrode (IDE) devices and parallel plate electrode (PPE) devices. As part of the design of such systems, this study aims to investigate the behavior of current density-voltage (J-V) in homogeneous and heterogeneous IDE and PPE devices to determine whether the anomalies between the interfaces of dielectric materials in such structures affect their leakage current. The ultimate goal is to design a solid-state capacitor energy storage module with low-loss dielectrics, high energy densities, and improved areal capacitance density that can offer a high number of charge/discharge cycles for portable power electronics. An understanding of J-V characteristics is crucial in achieving this objective. Specifically, this paper will explore and investigate nanolaminate, solid-state PPE, and IDE capacitive energy storage "modules" fabricated using nanolithographic techniques. The dielectric layers in these structures are composed of alternating nanolaminate layers of thin higher-k Al_2O_3 and lower-k SiO_2. Recent findings have shown that capacitive energy storage devices made from a large number of these on-chip multilayer nanolaminate energy storage PPE (MNES-PPE) structures that utilize the interfacial anomalies of thin high-k/SiO_2 nanolaminates could have the potential to overcome many of the limitations of current compact energy storage technologies. Preliminary projections indicate that these high-density nanolaminate capacitors with laminate thicknesses around 5 nm could produce devices with high volumetric energy densities (∼290 J/cm^3) that are significantly higher than conventional supercapacitors (∼20 J/cm^3).

Keywords: current density; energy storage; dielectrics; nanolaminates; monolithic; capacitors; solid-state

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1. Introduction

Currently available electrochemical batteries have the disadvantage of low power density, which restricts their use in applications that require high pulse power. Supercapacitors, on the other hand, have electrodes and electrolytes that can deteriorate after heavy use [1], despite having energy density about an order of magnitude smaller than lead-acid batteries [2]. These devices also suffer from low breakdown voltages, limiting their energy density [1]. Despite research efforts in advanced solid-state dielectrics, such as ferroelectric polymers [3], superlattices [4], and doped ferroelectrics [5], which aim to match the energy density of supercapacitors, they are not currently viable alternatives due to their lack of high breakdown field strengths [6].

Multiple factors affect the breakdown field strength and leakage current in devices, such as bonding structure, interfacial properties, materials' bandgap, the mean-free path

of electrons, and possible electron tunneling mechanisms. In high-k materials, where narrow bandgaps can result in significant loss, inserting a higher bandgap insulator between electrodes and nanolaminate layers can substantially reduce leakage current and enhance breakdown strength [7–9]. For example, researchers in [7] found that a 5 nm Al_2O_3 interfacial layer optimizes the dielectric properties of Al_2O_3/TiO_x nanolaminates, reducing leakage current density while maintaining high dielectric constant. However, refs. [7,9] demonstrated that using an ultra-thin interfacial Al_2O_3 layer (less than 2 nm) can cause direct tunneling, leading to a decrease in breakdown field strength.

One of the possible ways to develop solid-state capacitive energy storage devices with high permittivity, significant energy and power density, low leakage, and an enormous number of recharge cycles is to incorporate certain low loss, high-breakdown field strength materials such as Al_2O_3, HfO_2, ZrO_2, Si_3N_4, and SiO_2 into existing nanotechnologies [10] as multilayer nanolaminates. The interfacial permittivity of these dielectric nanolaminates and its impact on the current density-voltage (J-V) relationship are typically two of the most important electrical parameters to be understood and characterized.

The primary goal of this study is to enhance our comprehension of the current density-voltage (J-V) behavior in homogeneous and heterogeneous parallel plate electrode (PPE) and interdigitated electrode (IDE) devices by using experimental findings and 2-D finite element method (FEM) simulation models. The study aims to determine whether anomalies at the dielectric/dielectric material interface in such structures negatively impact the leakage current in a monolithic capacitor energy storage system. The insights gained from this investigation will be utilized to suggest the design of a high-density energy storage device with minimal loss and high breakdown voltage in Section 4 of this research.

2. Materials and Methods

2.1. Overview of Fabrication of PPE and IDE Devices

In this work, initially, the PPE devices with plate areas of 76 µm by 76 µm are fabricated on p-type silicon substrates with $< 100 >$ orientation and resistivity of 8–12 Ω·cm. The top and bottom metal electrodes are evaporated using a Denton Explorer e-beam evaporator tool. Next, 100 nm SiO_2 and Si_3N_4 dielectric layers are deposited using a Unaxis plasma enhanced chemical vapor deposition (PECVD) system on the first two PPE devices, and 100 nm of Al_2O_3 is e-beam evaporated for the third device as shown in Figure 1. The capacitance and conductance values of the PPEs are measured using HP4284A LCR four-point probe meter at f = 1 kHz with an AC amplitude of 1 V with zero offset bias. The measured capacitance values are used to extract the relative permittivities of SiO_2, Si_3N_4, and Al_2O_3 as k_{SiO_2} = 4.3, $k_{Si_3N_4}$ = 6.6 and $k_{Al_2O_3}$ = 9.9, respectively, by means of an analytical parallel plate model and the corresponding simulation models.

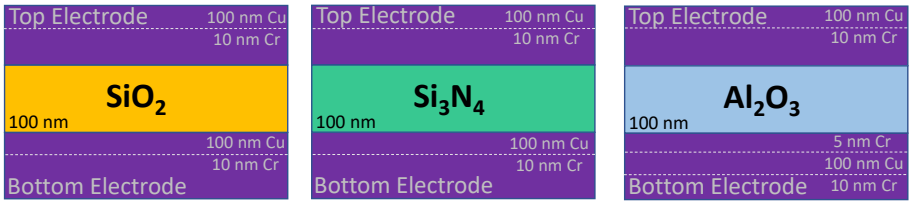

Figure 1. Parallel plate electrode (PPE) devices with (**a**) SiO_2, (**b**) Si_3N_4 and (**c**) Al_2O_3 dielectrics.

Using Si wafers with the aforementioned characteristics, three homogeneous and three heterogeneous IDE devices are fabricated with different combinations of SiO_2, Si_3N_4, and Al_2O_3 as shown in Figure 2. Initially, 900 nm of SiO_2 is deposited to provide an isolation layer. The wafer with the 900 nm SiO_2 layer is then cleaved using a diamond scribe into six samples. Next, the SiO_2 and Si_3N_4 layers are deposited on the samples using PECVD, and the Al_2O_3 is e-beam evaporated. The thickness of the first 900 nm SiO_2 layer is verified using a Nanospec Reflectometer, and for the 100 nm SiO_2, Si_3N_4 and Al_2O_3

layers, a Woollam M2000 Ellipsometer is used. All samples are then spin-coated using an A6 950-polymethylmethacrylate (PMMA) solution and are exposed using an Elionix ELS-G100 electron beam lithography (EBL) system at an exposure current of 3 nA. IDE capacitors with 1000 interleaved electrodes that have spacings of 200 nm are fabricated on each of the six samples using the EBL. The resulting patterns are developed in a mixture of one part methyl isobutyl ketone (MIBK) and one part isopropanol (IPA) and are inspected post-development using an Olympus MX61 Microscope. Next, the IDE electrodes and contact pads required for electrical measurements are formed by evaporating 10 nm of Cr and 100 nm of Cu using the e-beam tool. The PMMA residues on the samples are then lifted off by immersing the samples in a Microposit Remover 1165 and heating the solvent at 120 °C for 2 h. After the lift-off, the samples are triple-cleaned using IPA, acetone, and methanol and inspected using an Olympus MX61 Microscope. The widths of the IDE electrodes and the spacings between them are verified using a Hitachi S-4700 scanning electron microscope (SEM).

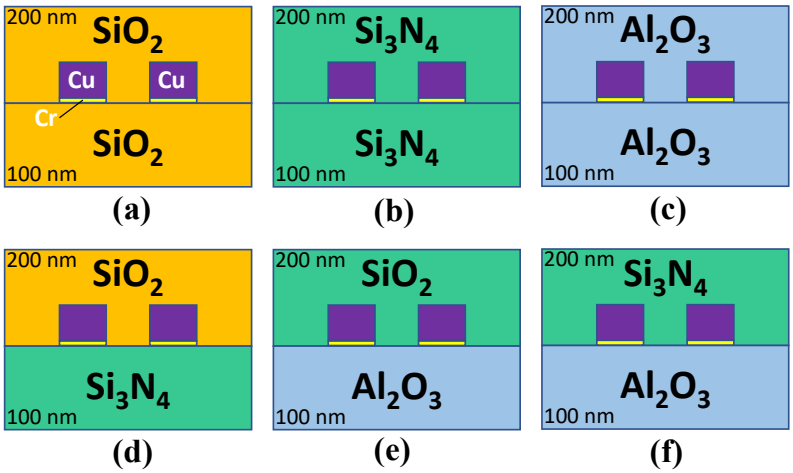

Figure 2. Interdigitated electrode (IDE) devices with (**a**) SiO_2/SiO_2, (**b**) Si_3N_4/Si_3N_4, (**c**) Al_2O_3/Al_2O_3, (**d**) Si_3N_4/SiO_2, (**e**) Al_2O_3/SiO_2 and (**f**) Al_2O_3/Si_3N_4 dielectrics.

Similar to the PPE devices, the capacitance and conductance values of the six IDE devices are measured using the HP4284A LCR 4-point probe meter under ambient conditions at f = 1 kHz with an AC amplitude of 1 V with zero offset bias at standard room temperature (25 °C). These measurements are explained in more detail in [11]. The devices are then encapsulated with 200 nm SiO_2, Si_3N_4, and Al_2O_3 layers as shown in Figure 2. As the last step of fabrication, the electrical contact pads of the devices are exposed using the EBL, developed, and thoroughly inspected.

2.2. Current-Voltage (I-V) Measurements

The I-V measurements on PPE and IDE devices are conducted using a Keithley 2450 Source Meter (SMU) instrument. These measurements aim to perform I-V testing that allows for the measurement of low current densities before dielectric breakdown occurs. The measurements are taken at low applied voltages to avoid damaging the PPE or IDE devices. A standard room temperature of 25 °C is maintained during the I-V measurements for both devices. Seven devices from each PPE and IDE structure are tested, resulting in 84 I-V measurements. The results of these electrical measurements are averaged and presented in Section 3 of this paper.

3. Results

3.1. Homogeneous PPE and IDE Devices

Figure 3a illustrates the current density-voltage (J-V) plot that compares the homogeneous IDE and PPE structures. It is evident from the plot that the IDE geometry exhibits a

higher leakage current than the PPE geometry. For instance, the SiO_2 device with homogeneous IDE has a leakage current that is orders of magnitude larger than that of the SiO_2 PPE device. Similarly, there is an approximate order of magnitude difference in leakage currents between the Si_3N_4 IDE and Si_3N_4 PPE and between the Al_2O_3 IDE and Al_2O_3 PPE structure, as depicted in Figure 3a. Notably, these differences in leakage are observed in homogeneous IDE and PPE devices that lack anomalous interfacial planes, which could cause additional low resistance current paths.

At V = 0.1 V, Figure 3b displays the electric field profile of both homogeneous IDE and PPE structures. In the homogeneous IDE SiO_2 device, the electric field varies between the adjacent electrode finger, with the highest fields situated at the edges of the electrodes (Figure 3c). Conversely, in the PPE SiO_2 structure, the electric field remains consistent between two parallel electrodes, as demonstrated in Figure 3d. The non-uniformity of electric fields in IDEs compared to PPEs can be attributed to the differences in the geometries of the electrodes. The fingers in the IDEs create a series of capacitors, which results in a non-uniform and complex distribution of electric fields along the electrodes [12,13]. The high fields around the IDE electrode could be a source of high carrier injection into the dielectric, while the PPE structure lacks these high fields entirely. Non-trivial carrier injection can occur when the electric field strength around the IDE electrodes exceeds a certain threshold, and the energy barrier of the dielectric material can be overcome, leading to the generation of charge carriers. After injection, these high fields could also initiate impact ionization, increasing the dielectric conductivity and leakage in the capacitor device. The aforementioned observations imply that a PPE electrode design would be more effective in significantly reducing leakage currents for a forthcoming energy storage device. However, due to their sensitivity to this electrical characteristic, IDE structures remain better suited for exploring tangential interfacial permittivity.

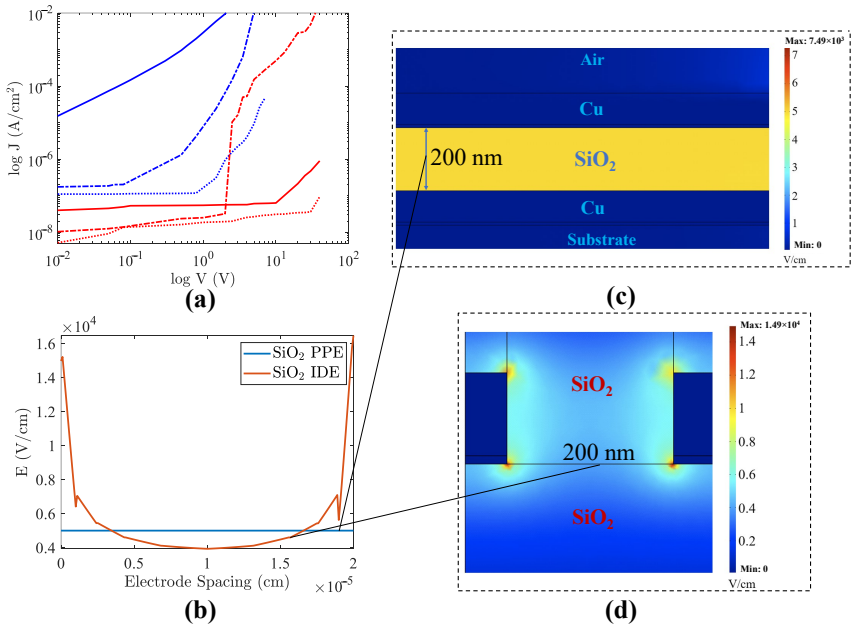

Figure 3. (**a**) J-V characteristic plots for the SiO_2, Si_3N_4, and Al_2O_3 homogeneous IDE and PPE devices. Solid blue line represents IDE SiO_2/SiO_2; blue dashed line represents IDE Si_3N_4/Si_3N_4; blue dotted line represents IDE Al_2O_3/Al_2O_3; solid red line represents PPE SiO_2; red dashed line represents PPE Si_3N_4; red dotted line represents PPE Al_2O_3. (**b**) Plot of electric field vs. electrode spacing characteristics between two electrodes for homogeneous (**c**) PPE SiO_2, and (**d**) IDE SiO_2 devices with 200 nm electrode spacing at 0.1 V.

3.2. Homogeneous vs. Heterogeneous Structure in IDE Devices

Figure 4 illustrates the current densities of both homogeneous and heterogeneous encapsulated IDE devices. In Figure 4a, the J-V characteristics of Si_3N_4/SiO_2 and SiO_2

IDE structures are quite similar. This suggests that leakage is primarily dominated by the bulk oxide between the electrodes, and consequently, the Si_3N_4/SiO_2 interface has minimal impact on device leakage. This experimental result holds significance since prior research in [14] identified the interfacial permittivity to be very high ($k_{Si_3N_4/SiO_2} \sim 1419$). Therefore, this finding strongly suggests that the Si_3N_4/SiO_2 material combination may be a feasible candidate for future device designs.

Furthermore, the J-V characteristic plots of the Al_2O_3/SiO_2, SiO_2, and Al_2O_3 IDE structures indicate that the inclusion of the interface has minimal impact on the overall leakage current. In Figure 4b, the Al_2O_3/SiO_2 device exhibits an order of magnitude lower leakage current than the homogeneous SiO_2 IDE device, but higher leakage compared to the homogeneous Al_2O_3 IDE structure. This suggests that the heterogeneous Al_2O_3/SiO_2 structure features a relatively low-leakage interface. Such low leakage, coupled with the high interfacial permittivity ($k_{Al_2O_3/SiO_2} \sim 2373$ [14]), provides strong encouragement for incorporating this Al_2O_3/SiO_2 interface into future energy storage devices. However, there is an interface that appears to exacerbate leakage current. Figure 4c demonstrates that the higher leakage current in the Al_2O_3/Si_3N_4 heterogeneous IDE structure compared to the other two homogeneous IDE devices indicates that the addition of the heterogeneous interface has degraded the quality of the Al_2O_3/Si_3N_4 heterogeneous device. This could be attributed to more complex interfacial trap states in this structure. Consequently, this outcome suggests that incorporating this interface into an energy storage device would not be suitable.

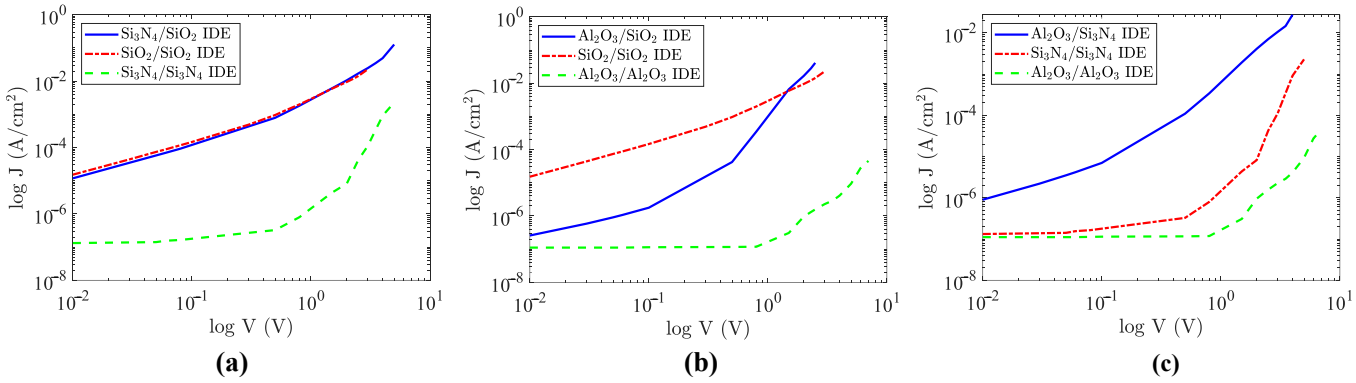

Figure 4. J-V characteristic plots for the heterogeneous and homogeneous IDE devices with (**a**) Si_3N_4/SiO_2, SiO_2, and Si_3N_4, (**b**) Al_2O_3/SiO_2, SiO_2, and Al_2O_3, and (**c**) Al_2O_3/Si_3N_4, Si_3N_4 dielectrics.

4. Discussion

Potential Application of Ideal High-Density PPE Devices

This section examines the potential of the previously fabricated homogeneous and heterogeneous IDE and PPE devices to be used as potential candidates for energy storage devices. A new device architecture that utilizes on-chip PPE structures and the directional interfacial anomalies of very thin (5 nm) SiO_2 and Al_2O_3 nanolaminates is proposed as a possible solution to overcome the shortcomings of current energy storage technologies.

The PPE and IDE structures, both homogeneous and heterogeneous, depicted in Figures 1 and 2 have been evaluated for their breakdown voltage. The J-V characteristics of these structures in Section 3 and the estimated breakdown voltage values for all the fabricated PPE and IDE structures were considered to identify the optimal energy storage device. The recommended device comprises thin nanolaminate dielectric layers of Al_2O_3/SiO_2 that are deposited so that the interface layers are perpendicular to the metallic electrodes, enabling the highly polarizable interfaces of these layers to be activated more efficiently, as illustrated in Figure 5.

The PPE structure of a theoretical multilayer nanolaminate energy storage system (MNES) is presented in Figure 5. This model, which was simulated using COMSOL

Multiphysics® (COMSOL, Inc., Stockholm, Sweden), consists of 18 alternating layers of 5 nm SiO_2 (k_{SiO_2} = 4.3) and Al_2O_3 ($k_{Al_2O_3}$ = 9.9), with a 1 nm high-k interfacial layer ($k_{Al_2O_3/SiO_2}$ = 2373), placed between capacitor electrodes with a spacing of 200 nm. The value of the interfacial high-k and the model itself have been extracted from experimental data described in [14,15]. The maximum storage voltage V_{max} for the MNES PPE configuration shown in Figure 5 can be calculated using:

$$V_{max} = \beta V_{bd} = \beta E_{bd} d, \quad (1)$$

where β is the maximum charging factor, V_{bd} is the breakdown voltage, E_{bd} is the breakdown field strength of the dielectric material, and d is the distance between the electrodes. SiO_2 has a breakdown field strength of ~15 MV/cm, and Al_2O_3 has a breakdown field strength of ~10 MV/cm, according to [16] and [17], respectively. Thus, assuming a maximum breakdown factor of β = 0.5, the breakdown voltages of SiO_2 and Al_2O_3 are calculated to be ~300 V and ~200 V, respectively. Assuming that the breakdown of these materials is roughly half the strength of the weakest dielectric material in the laminate structure, i.e., β = 0.5, the structure depicted in Figure 5 is then simulated at a maximum voltage of V_{bd} = 100 V. The resulting simulated capacitance C, which accounts for overhead capacitances, is calculated to be 0.1 pF. The maximum volumetric energy density for the multilayer nanolaminate U_{vol} can be calculated using:

$$U_{vol} = \frac{Energy}{Volume} = \frac{CV_{max}^2}{2} \cdot \frac{1}{device\ volume} \quad (2)$$

The MNES PPE energy storage device depicted in Figure 5 with 5 nm Al_2O_3/SiO_2 multilayers, assuming β = 0.5, has a maximum obtainable volumetric energy density U_{vol} of approximately 293 J/cm^3 when operated at a maximum voltage of V_{max} = 100 V. The corresponding current density is estimated to be around ~10 nA/cm^2. Notably, this volumetric energy storage value is 36 × greater than that of an energy storage device of the same dimension with only Al_2O_3 deposited between the electrodes.

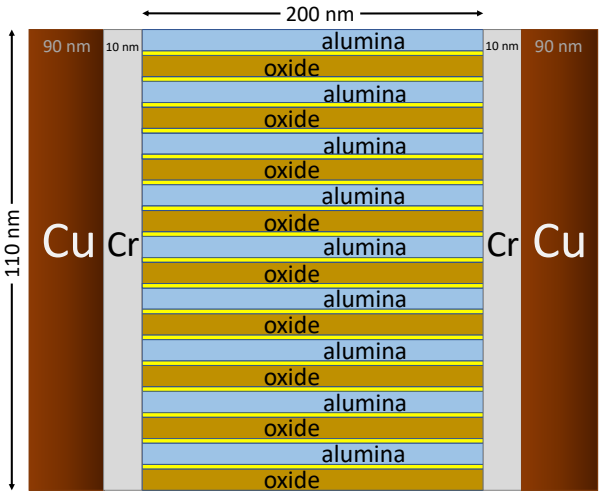

Figure 5. A zoomed FEM model of an multilayer nanolaminate energy storage (MNES) PPE structure composed of 18 alternating layers of Al_2O_3/SiO_2 with 1 nm high-k interface.

5. Conclusions

In this work, the current density-voltage characteristics of homogeneous and heterogenous IDE and PPE structures with SiO_2, Si_3N_4, and Al_2O_3 nanolaminates are investigated using experimental data and FEM simulations. The high breakdown field strengths of the materials examined in this work suggest that there may be potential for energy storage in capacitive devices that leverage the experimental findings and simulation results. In particular, preliminary J-V measurements and simulation projections showed that PPE

capacitive devices with a high density of Al_2O_3/SiO_2 nanolaminates with a laminate thickness of approximately 5 nm could produce devices with volumetric energy densities that are around 15× greater (i.e., ∼290 J/cm^3) compared to conventional electrochemical double layer supercapacitors (i.e., ∼20 J/cm^3).

Author Contributions: Z.M.K. and J.A.D. carried out the conceptualization, methodology, software, validation, formal analysis, investigation, and resources. Z.M.K. curated the data, prepared the original draft and did the writing. Z.M.K. and J.A.D. carried out the review and editing. J.A.D. supervised. Z.M.K. and J.A.D. administered the project. J.A.D. took care of the funding acquisition. All authors have read and agreed to the published version of the manuscript.

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Conflicts of Interest: The authors declare no conflict of interest.

Abbreviations

The following abbreviations are used in this manuscript:

IDE	Interdigitated Electrode
PPE	Parallel Plate Electrode
MNES	Multilayer Nanolaminate Energy Storage
FEM	Finite Element Method
PECVD	Plasma Enhanced Chemical Vapor Deposition
PMMA	Polymethylmethacrylate
EBL	Electron Beam Lithography
MIBK	Methyl Isobutyl Ketone
SEM	Scanning Electron Microscope

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