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Quad-Band Multi-Constellation Global Navigation Satellite System Receiver Development Platform with System-on-Chip Architecture †

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Abstract: GNSS receivers with multi-system and multi-frequency capabilities allow more reliable positioning, especially in challenging environments. However, increased available systems and signals lead to hardware resource allocation problems. This issue escalates when ten correlators per tracked GNSS signal are used. Moreover, the communication interface between the PL and the PS affects the time complexity and challenges the capability of the maximum number of tracking channels. This paper presents the GOOSE v2, a MPSoC-based GNSS receiver, which is composed of a quad-band (L1, L2, L5/E5 and S band) RFFE and baseband digital signal processing. The SoC includes a quad-core 64-bit processor and an FPGA. The on-chip communication between the processors and the FPGA offers high bandwidth, significantly reducing the time complexity. The preliminary evaluation of this new receiver platform shows that, in addition to the legacy signals, it supports NavIC L5 and S-band signals. Furthermore, this receiver closes the tracking loops faster than its legacy version (GOOSE v1), opening the door to implementing more complex algorithms requiring higher time complexity.

Keywords: global navigation satellite system (GNSS); navigation with Indian constellation (NavIC); system-on-chip (SoC); field programmable gate array (FPGA)

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1. Introduction

Global Navigation Satellite System (GNSS)-based positioning is growing at a rapid pace, and more devices (smartphones and upcoming application fields like autonomous driving or Internet of Things (IoT)) are equipped with GNSS receivers, enabling precise and reliable Position, Velocity and Time (PVT) solutions. According to the European Union Agency for the Space Programme (EUSPA) Earth Observation (EO) and GNSS market report for 2022 [1], it is forecasted that the annual shipments of GNSS receivers are to grow from 1.8 billion units to 2.5 billion units between 2021 and 2031. As a result, the global installed base of GNSS devices in use is expected to reach over 10 billion units by 2031. Consequently, the underlying satellite infrastructure system is also growing, and more countries tend to have independent satellite constellation systems. The same is true for Asia-Pacific and India. Instead of relying on other global systems (e.g., Global Positioning System (GPS), Galileo, BeiDou, or GLONASS), regional systems, such as Navigation with Indian Constellation (NavIC), were established to provide independent and tailored services to the users of a specific region.

More satellite systems mean more Satellite Vehicle (SV) availability, lower Dilution Of Precision (DOP) and an improved PVT solution. However, the increased availability of systems offers more challenges to the receiver manufacturers in terms of hardware and software resources, along with increased power consumption. Furthermore, GNSS receivers should maintain the synchronization of a higher number of SVs. GNSS receivers like the GNSS-Receiver with Open Software Interface (GOOSE)© platform [2] implement the tracking stage partly in hardware (correlators and Numerically Controlled Oscillator (NCO)) and partly in software (discriminators and loop filters). These receivers try to close the loop of all the tracking channels before a new correlation is performed. A low time complexity of the communication interface between the processor and the dedicated digital Hardware (HW) results in faster response and is essential to close the loop in time, avoiding synchronization failures. Also, the faster the response, the more tracking channels the GNSS receiver can manage. Moreover, a low time complexity in the communication interface enables the implementation of more complex and robust tracking architectures, such as Loop-Bandwidth Control Algorithm (LBCA)-based tracking architectures [3–5].

This work presents the GOOSE© v2 GNSS receiver, an enhanced version of the legacy GOOSE© [2], capable of receiving and processing four GNSS bands: L1, L2, L5/E5 and S-band. The latter could also be optionally replaced by E6. In addition to the existing legacy systems, the GOOSE© v2 also supports NavIC L5 and S-band signals. Figure 1 presents the GOOSE© v2 receiver platform.

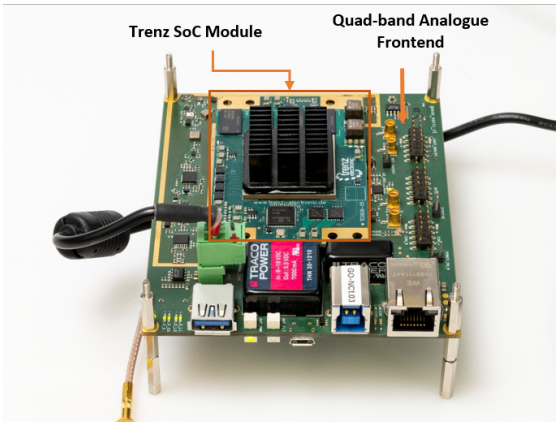


Figure 1. GOOSE© v2 receiver platform.

The receiver architecture is based on the Commercial-Off-The-Shelf (COTS) Multi-Processor System-on-Chip (MPSoC) module designed by Trenz Electronic [6]. The Programmable Logic (PL) part of this device contains a Fast Fourier Transform (FFT) core, a pseudo-random noise (PRN) generator module and 60 tracking channels. The Processing System (PS) includes a quad-core 64-bit processor and implements the code/carrier tracking loops, navigation message decoding and PVT algorithm. The System-on-Chip (SoC) feature allows the exchange between HW and Software (SW) with a very high bandwidth—thanks to the on-chip communication infrastructure.

This research performs a preliminary evaluation of the GOOSE© v2 by comparing it with its legacy version, evaluating the tracking of the NavIC signals and testing the capability of managed tracking channels.

The rest of the paper is organized as follows. Section 2 describes the proposed GNSS receiver named GOOSE© v2 and addresses the main updates compared to the legacy GOOSE© v1 receiver [7,8]. Section 3 presents the preliminary evaluation of the GOOSE© v2. Finally, Section 4 concludes and indicates future work.

2. Receiver Design

The GOOSE© v2 GNSS receiver is composed of an analog and a digital part. The digital part is characterized by the Xilinx MPSoC composed by the PS for the processing

implemented in SW and the PL, a kind of integrated Field-Programmable Gate Array (FPGA), to accelerate digital processing functions. Figure 2 shows the main architecture of the proposed platform.

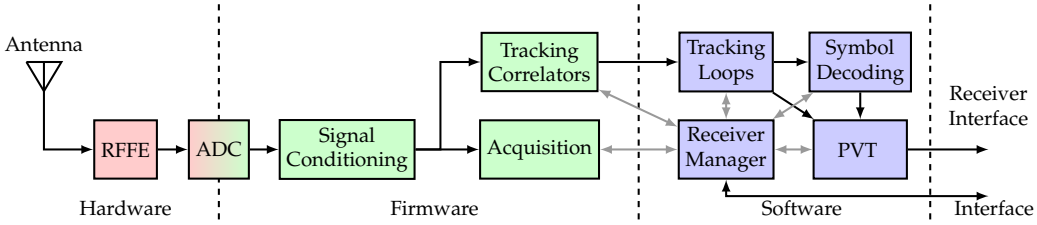


Figure 2. GOOSE© v2 architecture diagram.

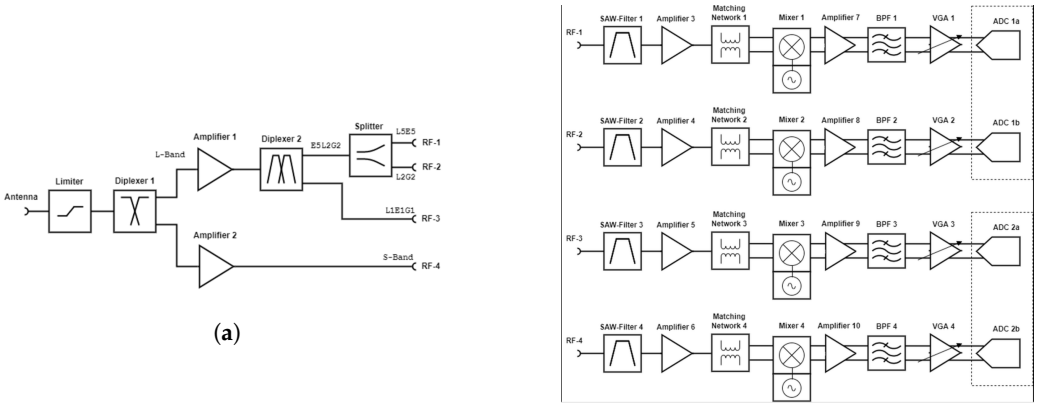
2.1. Radio-Frequency Front-End

According to the targeted frequency bands, the frequency plan in Table 1 is proposed. The E5-band (including the NavIC L5) determines the maximum bandwidth of 54 MHz to enable the reception of the full Galileo E5 Alternative Binary Offset Carrier (AltBOC) signal.

Table 1. Proposed frequency plan.

Channel	Band	Center Frequency (MHz)	Bandwidth (MHz)	LO Frequency (MHz)	IF-Band (MHz)	Sampling Rate (MHz)
1	L5, E5	1192	54	1254	35–89	250
2	L2, G2	1235	30	1298	48–78	250
3	L1, E1, G1	1582	50	1520	37–87	250
4	S	2492	20	2430	52–72	250

Figure 3 depicts the four-channel analog front-end of the GOOSE© v2. The input stage separates the antenna signal into four channels (see Figure 3a). After the limiter, the signal is divided into the L-band and S-band. A second diplexer is included in the L-band to split it into an upper and lower band. The lower band is connected to a splitter that creates two identical GNSS signals, which are processed separately (RF-1 and RF-2).



(**a**) (**b**)

Figure 3. Quad-band analog front-end: (**a**) radio frequency (RF) input stage and (**b**) RF signal chains.

The subsequent RF chains are processed individually (see Figure 3b). As the receiver architecture consists of one mixer stage that provides an Intermediate Frequency (IF) signal with only the real part, the pre-selection of the RF signal is important. A second measure to reduce the non-desired side bands is that the LO frequency of the mixer is higher compared to a low IF architecture with a complex IF signal. The following analog

processing is performed in four different paths. After band selection and amplification, the matching network converts the signal from single-ended to differential and is optimized for each band. The mixer stage shifts the signal according to the integrated local oscillator (see Table 1). The IF bandpass filter suppresses the out-of-band signals. The voltage gain amplifier (VGA) sets the appropriate level for the Analog-to-Digital Converter (ADC). Two dual 12-bit ADCs are selected to provide good performance in the digital domain. The sampling rate of the ADC is 250 MHz and enables the digital signal conditioning to use a simple $f_s/4$-mixer when shifting the signal to the baseband.

The schematic and the Printed Circuit Board (PCB) layout is optimized as follows:

- Same active components for all channels;
- Same footprint for all Surface Acoustic Wave (SAW) filters;
- Same structure for the matching network and the band pass filter, only the values of the components are changed.

The most significant benefit of this approach is that there is only one PCB layout design for all the channels, and the number of different active components is reduced to a minimum. This also guarantees fewer issues on the current component provisioning.

2.2. Digital Hardware Design

The digital HW board is based on a TE-0808 MPSoC module designed by Trenz Electronic [6]. This includes a Xilinx Zynq^{TM} UltraScale+^{TM}, 2 gigabyte (GB) 64-Bit Double Data Rate fourth generation (DDR4) memory, 2× Serial Peripheral Interface (SPI) Boot Flash (dual parallel) and altogether 4 × 160 pins used for the connectivity to the analog front-end board.

The benefits of employing a system on module (SoM) are the easy development, maintenance efforts and migration. On the one hand, the functionality is guaranteed by the manufacturer and it is typically possible to upgrade to an MPSoC device with a larger PL. On the other hand, they avoid the risks associated with the development of a customized FPGA board, because some special components like Random Access Memorys (RAMs) or FLASH memories cannot be bought in low volumes. The integrated SoC device is the Zynq^{TM} UltraScale+^{TM} XCZU15EG-1FFVC900E manufactured by Xilinx. The PS is characterized by a quad-core advanced Reduced Instruction Set Computer (RISC) machine (ARM) Cortex–A53 processor and a PL with approx. 750 K logic cells. The PL allows the implementation of real-time digital signal processing tasks at higher throughput. The firmware (FW) design mapped on the PL is described in Section 2.3.

2.3. Firmware Design

The firmware has two main purposes, i.e., to provide a signal conditioning of the received samples and to implement the different correlation methods needed by the GNSS acquisition and tracking stage. The PS of the Zynq^{TM} controls the digital HW modules implemented in the PL by reading and writing to the control and status registers. The communication interface integrated into the Zynq^{TM} MPSoC between PS and PL is Advanced Extensible Interface (AXI).

Baseband Design

The baseband core performs the standard GNSS operations. It contains a time management module, FFT acquisition and correlation channels for tracking. The time management module is based on a 32-bit HW counter, which runs at the frequency of the digital samples, and provides a unique time reference to all the GNSS modules.

The FFT acquisition unit is composed of a fixed size FFT core and its control logic. The acquisition supports a fast, a medium and a sensitive mode, and its algorithm is based on a parallel code-phase search method. The FFT core consists of a Xilinx XFFT Intellectual Property (IP). The size is 16 K according to the resource available on FPGA used in the platform. The acquisition module is controlled by the processor which specifies which signal should be searched for according to its acquisition strategy. Once the acquisition

performs a rough estimate of the main GNSS synchronization parameters, the tracking starts and refines the estimates. In total, there are 60 correlation channels in the presented GNSS platform.

Each correlation channel supports the correlation of two components (data and pilot) of a complex input signal. For each component, up to five delayed correlation points can be produced, which means that each channel is characterized in practice by ten complex correlators. The feedback control loops (Delay Locked Loop (DLL)/Frequency Locked Loop (FLL)/Phase Locked Loop (PLL)) are implemented in SW. They read out the complex integrate-and-dump data from the HW channels through a dedicated AXI interface. The loop steering values for the carrier and code NCOs are sent back through the channel control interface.

In addition to the control part, the correlation channels are characterized by the measurement interface, which collects information about all the internal counters and is triggered by the measurement interrupt generated by the time-management module. The measurements of all the channels are performed synchronously and allow for the calculation of the time of transmission of all the signals which are currently in tracking in SW. This is needed together with the time of arrival for the PVT calculation.

2.4. Software Design

The ogre_console is the main receiver program which manages the GNSS acquisition, tracking and PVT calculation processes. According to the signals selected (frequency and constellation), the receiver SW performs the acquisition in a continuous loop. For each acquired signal, a correlation channel is started. Different tracking options for each signal can be specified. As soon as enough signals are in tracking, a PVT can be calculated. The PVT is based on code measurements from the channels and the decoded Ephemeris.

3. Preliminary Receiver Evaluation

3.1. Resource Utilization on PL FPGA

Table 2 shows the resource utilization of the GOOSE© v2 receiver compared to v1. Since the same FFT size and amount of tracking channels are instantiated (as shown in Table 3), there is no significant difference in slice Lookup Tables (LUTs) between the two implementations. The 20,000 more LUTs are associated with the additional frequency band added in the digital signal conditioning. Each ADC frequency channel is first down-converted using the $f_s/4$-mixer and then down-sampled with a factor of 4. Therefore, an additional static Low-Pass Filter (LPF) is needed for anti-aliasing. This significantly increases the amount of Digital Signal Processor (DSP) blocks used, which is still only 10% of the blocks available on the device.

Table 2. Resource utilization.

Receiver	Xilinx Device	Slice LUTs	%	DSP Blocks	%
GOOSE© v1	Kintex7 410	221,783	78.25	71	4.61
GOOSE© v2	ZynqUS+ 15EG	239,506	70.18	370	10.49

Table 3. Firmware design components and properties.

Receiver	ADC Samples (bits)	ADC f_s (MHz)	Baseband Samples (bits)	Baseband f_s (MHz)	Static LPF	FFT Size	Tracking Channels
GOOSE© v1	8	81	4	81	-	16 K	60
GOOSE© v2	12	250	5	62.5	4	16 K	60

3.2. Performance Comparison between GOOSE v1 and GOOSE v2

In order to test the communication aspect of HW and SW, a parallel test with GOOSE© v1 and GOOSE© v2 is conducted in our Galileo lab using the Spirent Radio-Frequency Constellation Simulator (RFCS). The aim is to find out the number of tracking channels that the GNSS receiver can handle. The test setup is presented in Figure 4. Here, the RF output of the Spirent is connected to both receivers through a splitter.

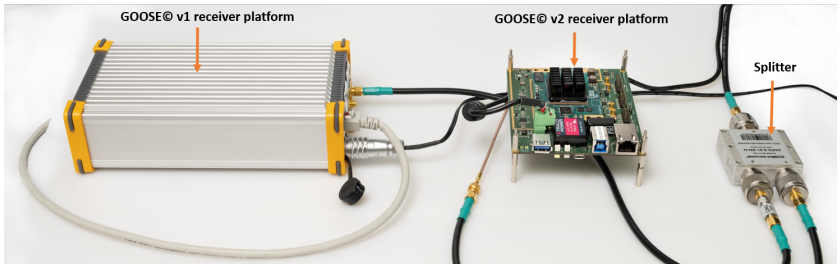


Figure 4. Test setup.

The selected test scenario includes GPS L1/L5 and Galileo E1/E5a signals. The HW integration time is set to 1 ms for both receiver platforms. Figure 5 shows the result of this test. At the start of the scenario, five SVs are enabled. Afterwards, one SV is added with at 1 min intervals. The number of tracked HW channels increases with respect to time. The trend is similar in both platforms, until E11 is added at the 480th second, where all of a sudden, the GOOSE© v1 stops while the other keeps tracking more SVs.

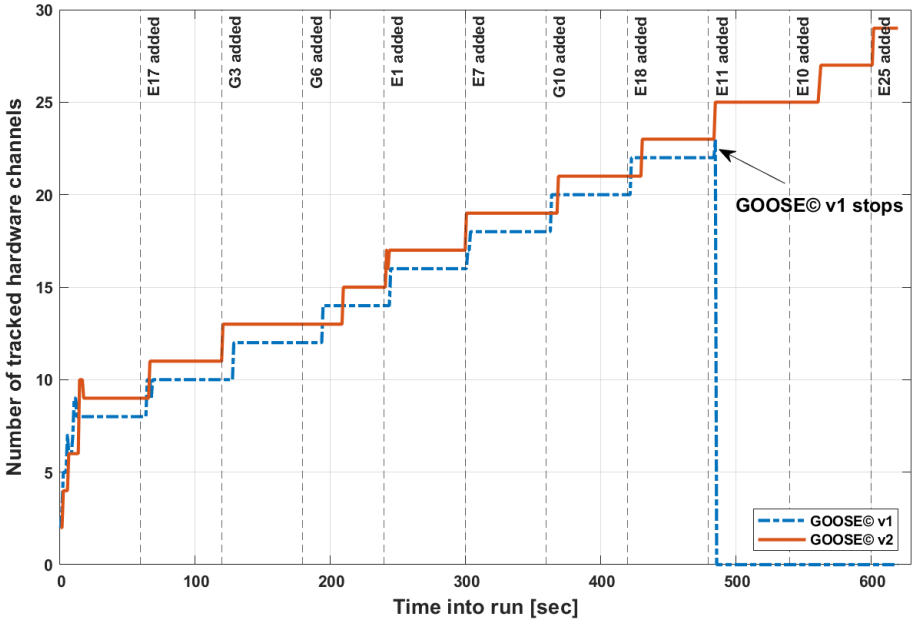


Figure 5. GOOSE© v1 and GOOSE© v2 performance result.

Figure 6 presents the computational load of both receivers at the break point of GOOSE© v1. Due to the high time complexity of the communication interface between PL and PS, the GOOSE© v1 cannot close the tracking channels in less than 1 ms. Consequently, the receiver SW application increases the computational load to a level until it terminates.

This result shows that GOOSE© v2 outperforms the GOOSE© v1 receiver when the HW integration time is reduced to 1 ms. This aspect plays a vital role for algorithms where the tracking loops need to be closed in the lowest possible time, such as in Vector Tracking (VT) [9], Deep Coupling (DC) and LBCA [5].

Figure 6. GOOSE© v1 and GOOSE© v2 processor load.

3.3. NavIC Tests Using GOOSE v2

The proposed platform was designed to support the NavIC processing. NavIC is a regional navigation satellite established by Indian Space Research Organization (ISRO). It is designed with a constellation of seven satellites and a network of ground stations. Currently, three satellites are placed in geostationary orbits and four satellites are placed in inclined geosynchronous orbits [10].

The first test demonstrates that the platform can acquire and track the L5 band of all the NavIC satellites visible from the test facility. The test setup is composed of GOOSE© v2 connected to the NavIC reference antenna. The NavIC reference antenna is mounted on the roof of the Fraunhofer IIS building in Nuremberg. Figure 7 shows that four L5 signals are acquired and are in stable tracking with a carrier-to-noise density ratio (C/N_0) of approx. 40 dBHz.

Table 4 shows a comparison of the C/N_0 between the proposed platform and a commercial receiver (Septentrio Mosaic-X5 [11]). The lower C/N_0 of the GOOSE© v2 might be due to the larger reception bandwidth, which also causes unwanted signals being processed. In order to improve the C/N_0, some additional filtering is needed in the S band channel or some interference mitigation capability.

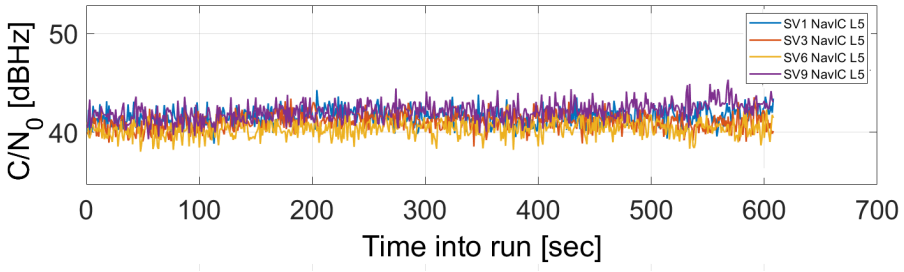


Figure 7. NavIC-L5 results using GOOSE© v2.

Table 4. NavIC-L5 C/N_0 mean values comparison between GOOSE© v2 and Mosaic-x5 receiver.

Receiver	SV1 (dBHz)	SV3 (dBHz)	SV6 (dBHz)	SV9 (dBHz)
GOOSE© v2	41.56	41.03	40.34	42.12
Septentrio Mosaic-X5	42.71	42.27	41.56	43.32

3.4. L1–L5 Tests Using GOOSE v2

To evaluate the more commonly used GPS and Galileo constellations, an additional test was performed. GPS L1CA and L5, Galileo E1BC and E5 AltBOC, and NavIC L5 and S were tracked using the NavIC reference antenna. In parallel, Septentrio PolaRx5 receivers also track signals of the same constellations. Figure 8a,b show the C/N_0 results of the GPS L1CA and Galileo E1BC using the GOOSE© v2. The C/N_0 results of the same signals using Septentrio PolaRx5 are provided in Figure 9. Here, we can see a slight difference in the amount of signals tracked due to the higher sensitivity of the commercial receiver.

Figure 8c,d show the C/N_0 results of the GPS L5 and Galileo E5 AltBOC on the GOOSE© v2. The C/N_0 results of the same signals using Septentrio PolaRx5 are provided in Figure 10. In this case, the C/N_0 of the two platforms is comparable and the same signals are tracked. No relevant difference can be observed for the L5-E5 band.

In addition, Figure 8e shows the C/N_0 for the NavIC L5- and S-band tracked satellites. The Septentrio receiver can track one low-C/N_0 signal more but cannot track signals in the S band.

In the test, we can see that both frequencies can be tracked for all the satellites except SVID1. The reason for this is not clear and should be further investigated. Additionally, L5 provides a higher C/N_0 of up to 3 to 5 dBHz. This could be due to the presence of interfering signals in the S band.

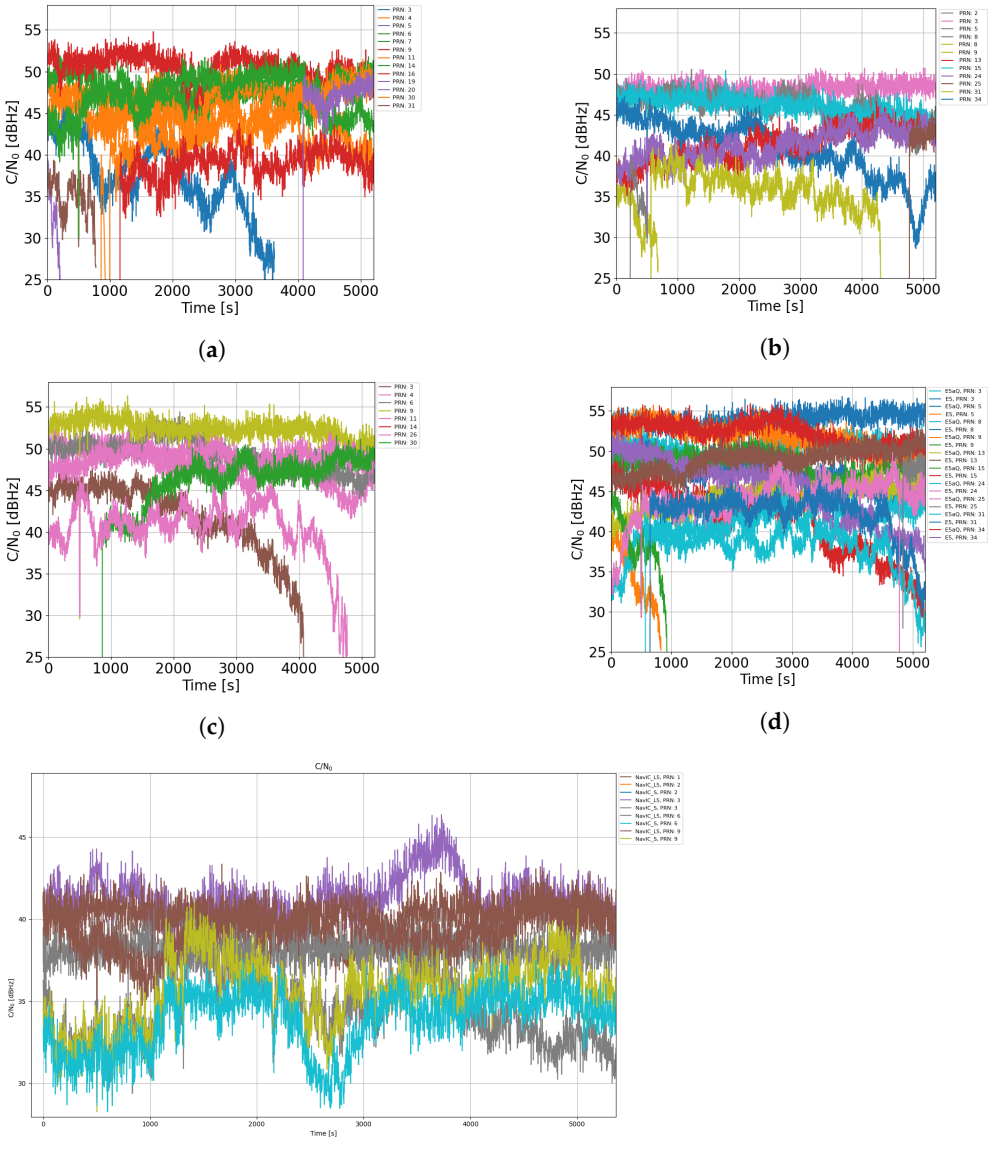


Figure 8. C/N_0 results with GOOSE© v2. (**a**) GPS L1, (**b**) Galileo E1, (**c**) GPS L5, (**d**) E5 AltBOC and E5A, and (**e**) NavIC L5 and S.

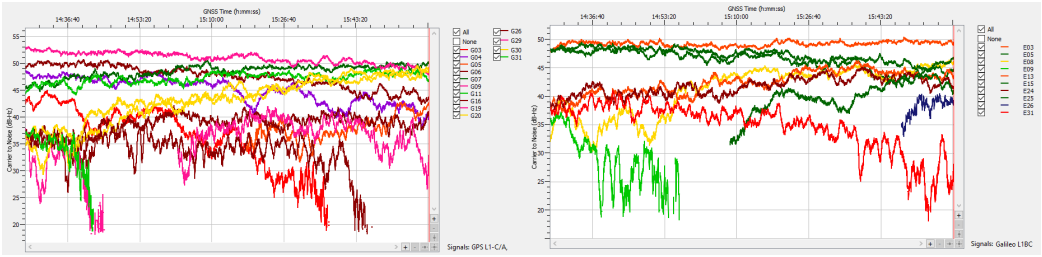


Figure 9. GPS L1 and Galileo E1 C/N_0 results using Septentrio PolaRx5.

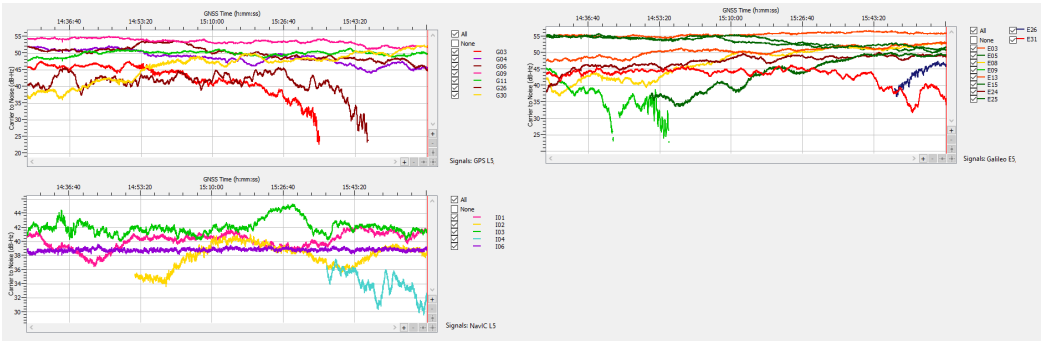


Figure 10. GPS L5 and Galileo E5 AltBOC C/N_0 results using Septentrio PolaRx5.

4. Conclusions

This paper presents an enhanced version of the legacy GOOSE©, the GOOSE© v2. This new platform is an MPSoC-based GNSS receiver that contains a quad-band (L1, L2, L5/E5 and S band) Radio-Frequency Front-End (RFFE) and baseband digital signal processing. The SoC feature allows at the same time the exchange between HW and SW with a very high bandwidth—thanks to the on-chip communication infrastructure. The results show that, in addition to the legacy signals, the new receiver platform supports the NavIC L5 and S-band signals along with the ability to close the tracking loops faster than its previous version. In addition, the proposed platform includes a Coral accelerator module suitable for exploiting potential GNSS Machine Learning (ML) algorithms [12].

As future work, the testing of the digital record and replay capability of the GOOSE© v2 using the four channels will be performed. In addition, the High-rate DFT-based Data Manipulator (HDDM) will be implemented in the PL of the platform [13]. Moreover, due to low time complexity of the PL-PS communication interface, more complex algorithms will be evaluated in SW, such as the VT and the LBCA.

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