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Comparative Analysis of Design Parameters for Modern Radio Frequency Complementary Metal Oxide Semiconductor Ultra-Low Power Amplifier Architecture Trends †

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Abstract: This research presents a comparative analysis of design parameters in modern power amplifier (PA) architecture trends in various CMOS nano-meter technologies. The design parameters include the signal gain, linearity, output power, and output power back-off. The resultant parameters are compared using a table, and various parameters of various designs are visually shown for comparison. These comparative findings will provide any designer with practical information to choose the best CMOS PA design for a specific application. The most important RF CMOS PA integrated implementations are addressed in the conclusion section.

Keywords: CMOS RF power amplifier; nano-meter technology trends; ultra-low power

1. Introduction

Currently, a faster, more effective, linear, and power-efficient communication system with a higher frequency is pursued due to the enormous demand for and rapid development of wireless transmission, as well as the needs for advanced short-range low-power Wireless Personal Area Network (WPAN) and long-range low-power Wireless Local Area Network (WLAN) systems [1]. Therefore, it is crucial to improve the PA's design in communication systems. In order to increase efficiency, modern power amplifiers should be built with a large output back-off (OBO) and enhanced efficiency. Because of the small chip size, CMOS technology enables operation at an ultra-low power supply, which reduces power dissipation and lowers manufacturing costs [2]. Figure 1 Represents the IEEE standards for ULP architectures.

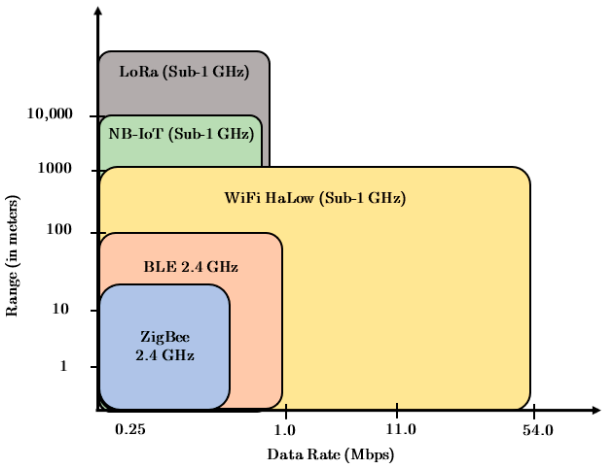

Figure 1. IEEE standards for low-power communications.

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2. Comparative Analysis of Modern RF CMOS PA Design Parameters

To assess the overall performance, a figure-of-merit (FoM) is used, which takes into account the most significant performances and characteristics in a methodology as follows:

$$\text{FoM} = \text{Saturated Output Power (dBm)} + \text{Power Gain (dB)} - \text{Insertion Loss (dB)} + 10\log[\text{PAE(\%)}] + 20\log(\text{freq(GHz)}] - 10\log[\text{dc Power Consumption (mW)}] \quad (1)$$

Equation (1) can be recognized by considering measurement representations as

$$\text{FoM} = P_{dBm} + S21_{dB} - S11_{dB} + 10\log(\text{PAE}) + 20\log(f_{GHz}) - 10\log(P_{dc}) \quad (2)$$

where P_{dBm} is the saturated output power in dBm, S21 is the power gain in dB, S11 is the insertion loss in dB, PAE is the power-added efficiency in percentage, f_{GHz} shows the channel frequency in GHz, and P_{dc} is the dc power consumption in mW. Figure 2 illustrates the PAE, output power, and FoM for recent PA architecture.

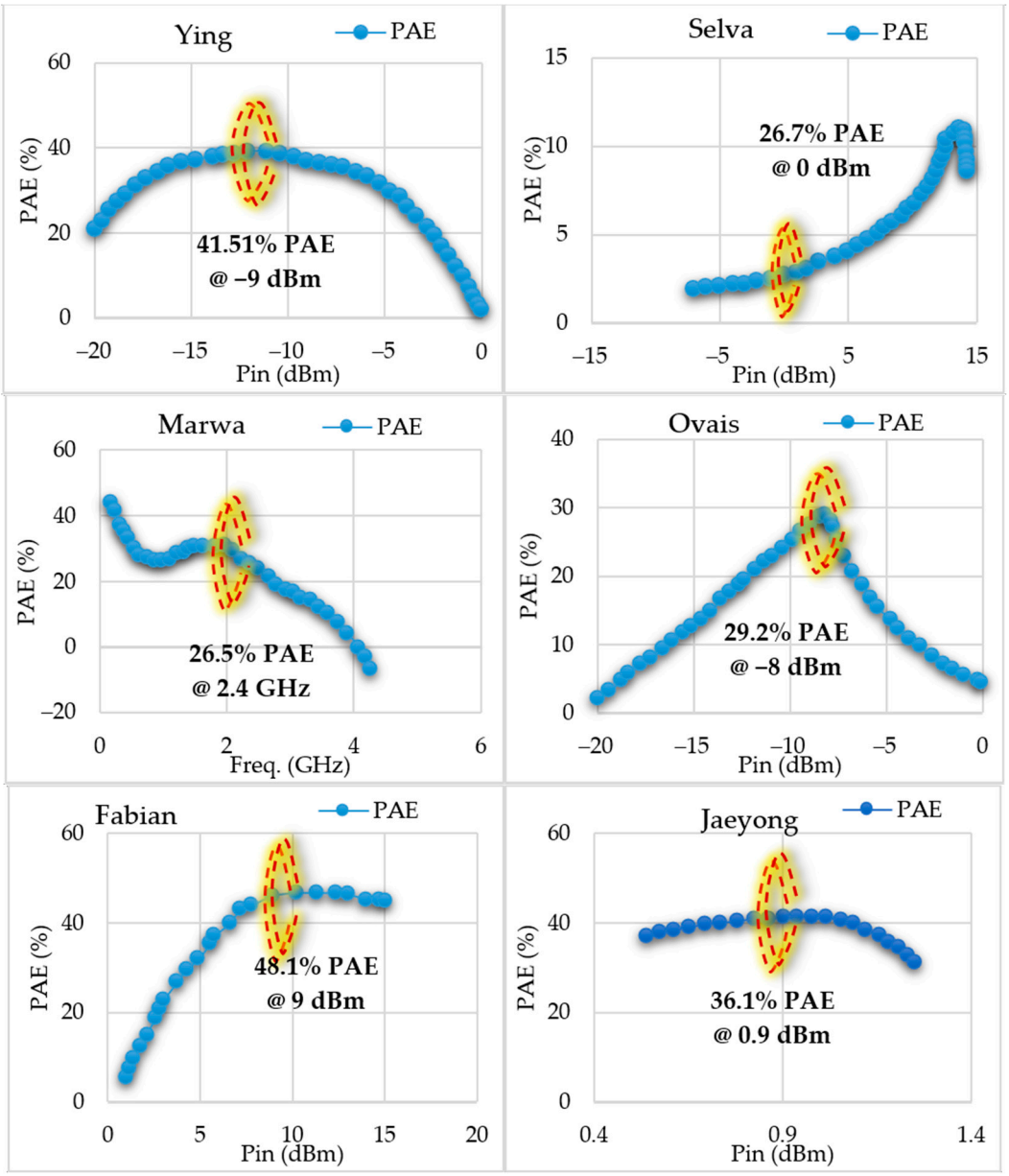
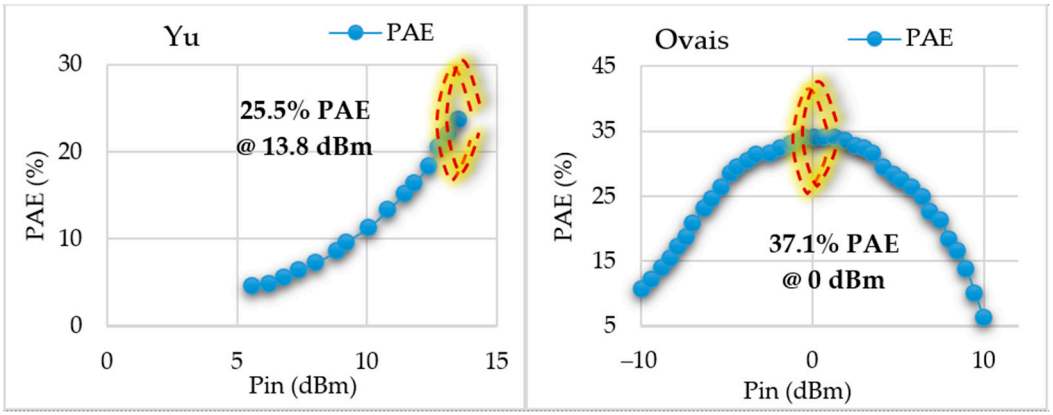
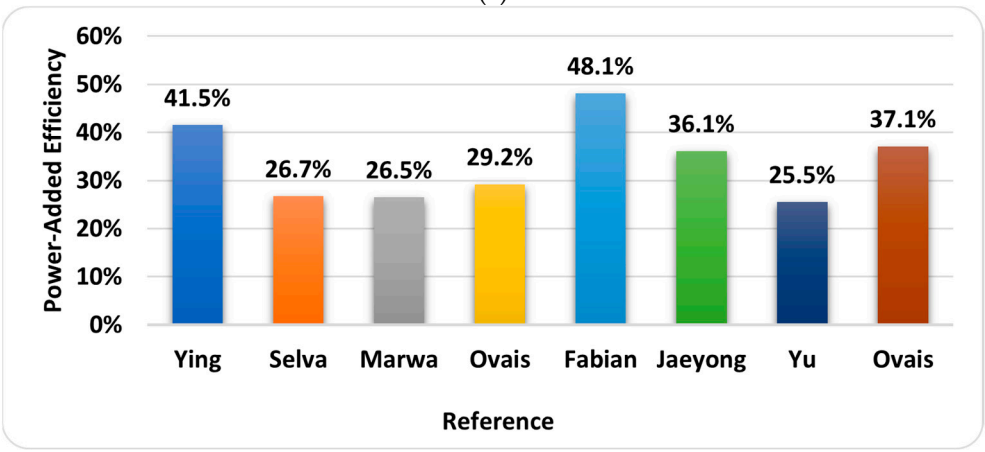


Figure 2. *Cont.*



(**a**)



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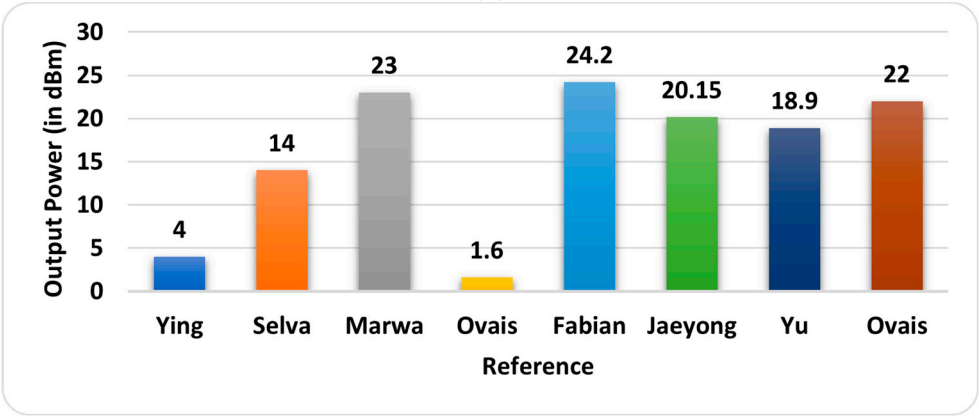
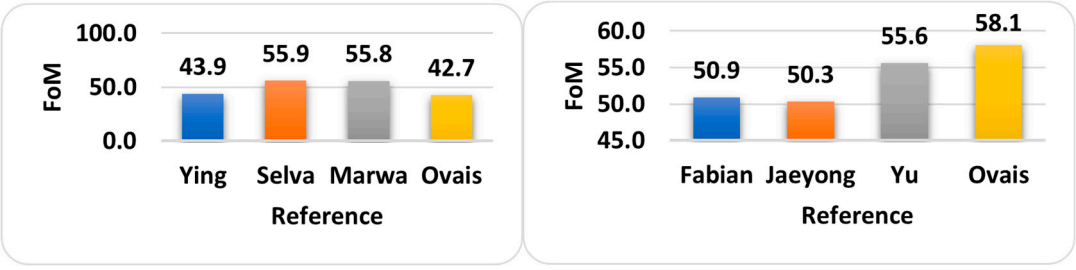


(**c**)



(**d**)

Figure 2. (**a**) PAE of individual design. (**b**) Discrete and statistical comparison of the PAE with the input power (dBm) and modern RF CMOS design architectures. (**c**) Comparison of saturated output power and (**d**) the analyzed figure-of-merit.

Table 1 shows the performance metrics for various state-of-the-art modern CMOS RF PAs at a glance. The depicted results were simulated to observe the discrete comparison of the PAE with the input power (dBm) and modern RF CMOS design architectures.

Table 1. Comparison of state-of-the-art CMOS RF PA ULP architecture in recent years.

Reference	Ying [3]	Selva [4]	Marwa [5]	Ovais [6]	Fabian [7]	Jaeyong [8]	Yu [9]	Ovais [10]
Technology	22 nm	180 nm	130 nm	65 nm	180 nm	180 nm	180 nm	65 nm
Year	2022	2019	2020	2021	2021	2019	2015	2022
IEEE Standard	BLE/802.15.4	BLE	BLE	BLE/802.15.4	802.11 ah LP-WLAN	802.11 ah LP-WLAN	802.11 ah LP-WLAN/LTE	802.11 ah LP-WLAN
Frequency	2.4 GHz	2.45 GHz	2.4 GHz	2.4 GHz	Sub-1 GHz	Sub-1 GHz	Sub-1 GHz	Sub-1 GHz
Supply Voltages	1.2 V	1.8 V	1.2 V	1.2 V	1.8 V	3 V	1.7 V	1.2 V
DC Power Consumption	LP (12 mW) (V_{DD} = 1.2 V and I_Q = 19.3 mA × 0.637)	LP (19 mW) (V_{DD} = 1.8 V and I_Q = 17 mA × 0.637)	LP16 mW	ULP 2.10 mW (V_{DD} = 1.2 V and I_Q = 2.75 mA × 0.637)	---	---	LP 18 mW	ULP 3.75 mW
Output Power	4 dBm	14 dBm	23 dBm	1.6 dBm	24.2 dBm	20.15 dBm	18.9 dBm	22 dBm
1 dB Compression	---	---	19.6 dBm	4.0 dBm	---	---	13.6 dBm	14.3 dBm
Input Return Loss (S11)	−11 dB	−19.7 dB	---	−11.9 dB	---	−14 dB	−23 dB	−15.05 dB
Power Gain	15.9 dB	12.9 dB	13 dB	10.14 dB	---	12 dB	13.6 dB	11.86 dB
Peak PAE	41.5%	26.7%	26.5%	29.2%	48.1%	36.1%	25.5%	37.1%

2.1. Power-Added Efficiency

The post-layout simulation results show that cascodes class-E [3] and class-D [7] have the highest PAEs for short-range WPAN and long-range WLAN networks, respectively. The analysis was performed with reference to the input power (in dBm). Concerning BLE RF PAs, Integrated Analogue Pre-Distorters (APDs) [4] and class-F designs with reconfigurable off-chip inter-stage matching networks [10] have a low PAE compared to class-E [3] and class-D [6] design architectures.

2.2. Saturated Power in dBm

Taking into account the WPAN BLE standards, Integrated Analogue Pre-Distorters (APDs) [4] and class-F designs with reconfigurable off-chip inter-stage matching network architectures [5] produce more output power because of the BLE class-1 ISM band. The least output power is produced by the CMOS power amplifier based on transformer coupling and synthetic dielectric differential transmission. Due to class-2 BLE ISM band designs, the remaining devices offer acceptable output powers between 1 and 4 dBm. Due to the sub-1 GHz band, the IEEE 802.11 ah WiFi HaLow offers a long range of up to 1 km, as observed in [7–10] PA design architectures.

2.3. ULP Consumption

The DPA with fixed inter-stage capacitances [6] and class-F designs with feedback using ET supply bias [10] are ultra-low power (ULP) designs compared to the rest of the proposed architectures. The MOS architectures in both designs are biased in the subthreshold region. The MOS biasing operation in moderate and weak inversion regions is a noticeable justification for ULP.

2.4. Figure-of-Merit

The BLE 4.0 and IEEE 802.11 ah standards exhibit the highest FoM due to ultra-low power consumption and PAE as major factors. Figure 2d compares the FoM for both low-power and long-range standards, respectively.

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Conflicts of Interest: The author declares no conflict of interest.

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