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Effects of Electrical Stress in Solution-Processed Spin-On Glass Dielectric Films: Frequency Dependence †

Ovier Obregon, Salvador Alcantara, Susana Soto and Miguel A. Dominguez *

Centro de Investigaciones en Dispositivos Semiconductores, Instituto de Ciencias, Benemérita Universidad Autónoma de Puebla (BUAP), Puebla 72570, Mexico; ovier.mectronica@gmail.com (O.O.); iniesta.salvador@gmail.com (S.A.); blanca.sotocruz@viep.com.mx (S.S.)

* Correspondence: miguel.dominguezj@correo.buap.mx; Tel.: +52-(222)-229-55-00 (ext. 1043)

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Abstract: In this work, the effects of the frequency dependence of transparent dielectric based on Spin-on Glass (SOG) under electrical stress is presented. The SOG thin films were cured at 200 °C in ambient air. The capacitance-voltage and capacitance-frequency characteristics were measured in Metal-Oxide-Semiconductor (MOS) capacitors using the SOG thin film. In addition, electrical stress is applied to the MOS capacitors at different voltage values and during a long period of time. The results show, depending on the bias stress applied, a reversible interface charge contribution and an irreversible charge induced by interface states probably generated by the degradation of the film.

Keywords: solution-processed; electrical stress; spin-on glass

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1. Introduction

Currently, the stability of field-effect devices based on emerging technologies is one of the most demanding research issues in terms of performance [1–5]. Since solution-processed electronic devices are attracting much attention to enable low-cost flexible electronics, the reported studies of stability seem to be conceived with arbitrary conditions. Frequently, they do not give explanation for the stress conditions used or the same values of electrical stress previously reported were considered, regardless the gate dielectric thickness and structure of the device [6–12]. Moreover, only few studies can be found in literature about this topic in solution-processed dielectric films [13].

Along with the material properties of each layer in the device, interface properties have a strong influence on the device performance. In this work, the effects of electrical stress in solution-processed dielectric film are presented. In particular, the frequency dependence of transparent dielectric based on Spin-on Glass (SOG) under electrical stress is presented. Electrical stress is applied to MOS capacitors at different voltage values and during a period of time. It is important to note that the SOG film was previously used as gate dielectric in planarized a-SiGe:H TFTs, flexible zinc nitride TFTs and flexible AZO diodes [14–16].

2. Materials and Methods

The SOG solution (SOG700B Filmtronics) was diluted 3:1 with Deionized Water (DI) and spin coated into the samples. The SOG/DI films were cured at 200 °C in air ambient. The complete fabrication process of the MOS capacitors is found elsewhere [17]. The capacitance-voltage and capacitance-frequency characteristics were measured using the Keithley-4200 Semiconductor Characterization System equipped with the 4200-CVU Integrated C-V, under dark conditions, ambient air and room temperature.

3. Results and Discussion

Figure 1 shows the capacitance-voltage characteristics for the n-type MOS capacitors. The characteristic shows a well-defined accumulation region when a positive voltage is applied at the top contact, as the positive voltage increases there is an accumulation of electrons at the dielectric-semiconductor interface (SOG-Si), increasing the capacitance. When a negative voltage is applied at the top contact, a depletion region is induced, then, the capacitance decreases [18].

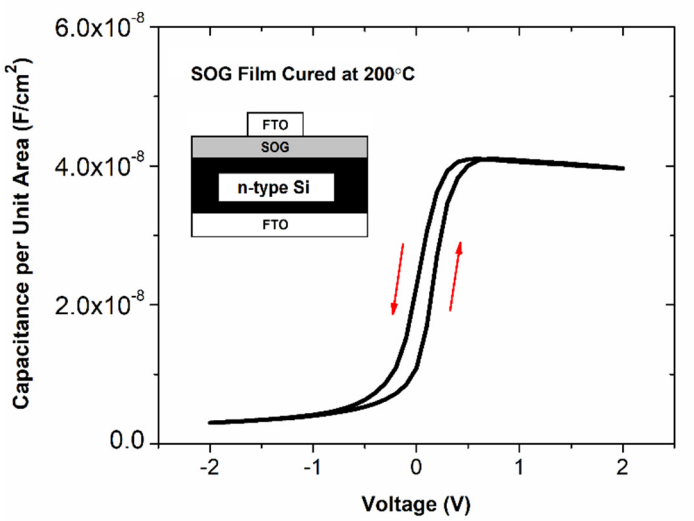

Figure 1. Capacitance-voltage characteristics for the n-type MOS capacitors.

Field-effect devices, such as thin-film transistors, work in accumulation where the channel layer is formed at the dielectric-semiconductor interface. Therefore, in order to study the frequency dependence under electrical stress, the capacitance is measured in the accumulation region of the MOS capacitors (2 V). Figure 2 shows the frequency dependence of the MOS capacitors comparing the initial characteristics and after 5V electrical stress during different times. It can be observed as a frequency dependence, or also called frequency dispersion, at the initial measurement due to interface states [5,19]. On the other hand, the electrical stress induce charge trapping at the dielectric-semiconductor interface (interface charge). This interface charge causes variations in the accumulation capacitance [18–20]. It can be observed, that after a long stress time, the characteristics are very similar.

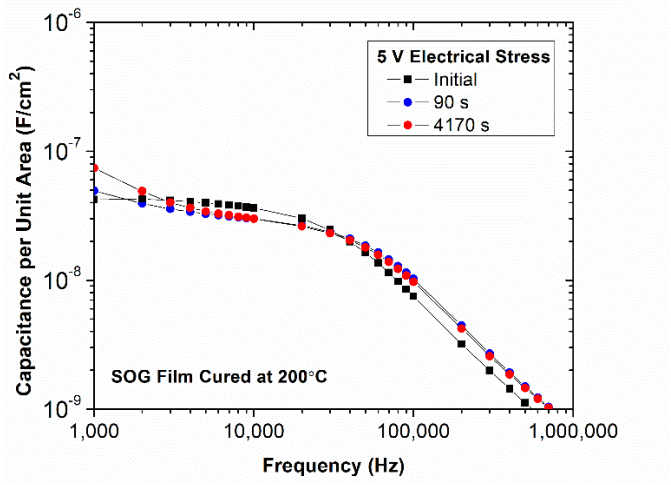

Figure 2. Frequency dependence characteristics for different stress time at 5 V electrical stress.

Figure 3 shows the frequency dependence characteristics for different stress times at 10 V applied. At high frequencies, the accumulation capacitance after electrical stress exhibit similar values than the initial measurement. However, it is clearly exhibited in an increase of the accumulation capacitance at 1–4 KHz due to the higher electrical stress. Some authors have reported a similar behavior in solution-processed dielectric films without electrical stress [21]. They suggest that this behavior can be due to residuals during the deposition of the films. Since our SOG dielectric films are deposited at low temperature, probably some residuals interact with the electrical stress, inducing additional charges. These induced charges can follow the low frequency contributing to the accumulation capacitance [22,23]. This behavior can be expected, since in solution-processed films the evaporation of solvents during the deposition and the low-temperature used, tends to make the films with high leakage current due to residuals [21,24]. In order to analyze these induced charges, the MOS capacitors were kept in rest for 48 h and measured again. Figure 4 shows the comparison of the initial and rested frequency dependence characteristics after the 10 V electrical stress. As can be seen, the characteristics are reestablished, indicating that most of the interface charge is reversible, as many authors suggest [25–30].

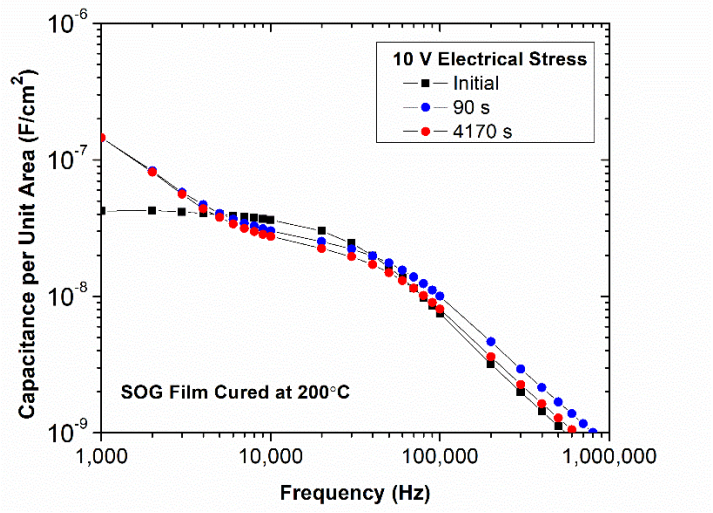

Figure 3. Frequency dependence characteristics for different stress times at 10 V electrical stress.

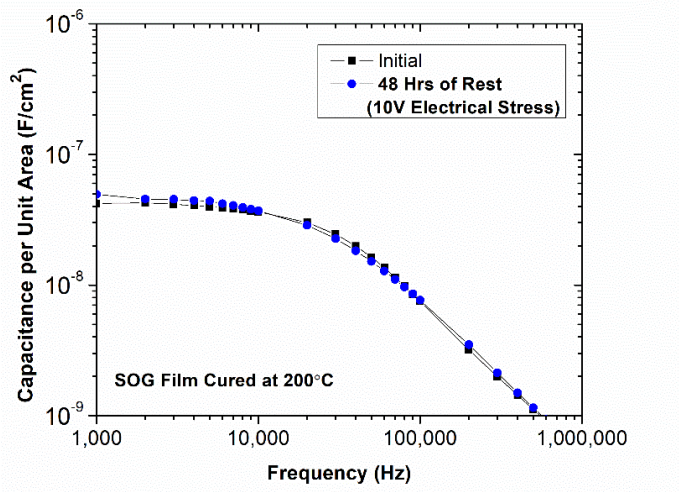

Figure 4. Comparison of the initial and 48 h rested capacitance-frequency characteristics after 10 V electrical stress.

On the other hand, a higher electrical stress was induced by applying 20 V for different times (Figure 5). A clear dependence of capacitance with frequency can be appreciated.

At higher frequencies, there is a decrease in the accumulation capacitance that can be related to a reduction of the accumulation charge in the MOS capacitor, due to the tunneling of electrons through the dielectric [20,31]. Additionally, the accumulation capacitance at 1–4 KHz is increased by the additional interface states. The MOS capacitors were kept in rest for 48 h and measured again. Figure 6 shows the initial and rested frequency dependence characteristics after 20 V electrical stress. It is appreciated that the characteristics are irreversible after 48 h of rest. This suggests that the higher electrical stress induce an irreversible degradation in the dielectric film by a higher tunneling rate through the dielectric, where these carriers slowly degrade the dielectric film making irreversible the effects of the electrical stress [30]. The degradation of the dielectric film by the tunneling of carriers can be correlated with the interaction of electrical stress and residuals in the film. These results can be useful to differentiate the reversible interface charge contribution and the irreversible charge induced by the degradation of the film. All these lead to find an optimum range of stability in the dielectric film to be used in the study of stability of solution-processed electronic devices, such as thin-film transistors.

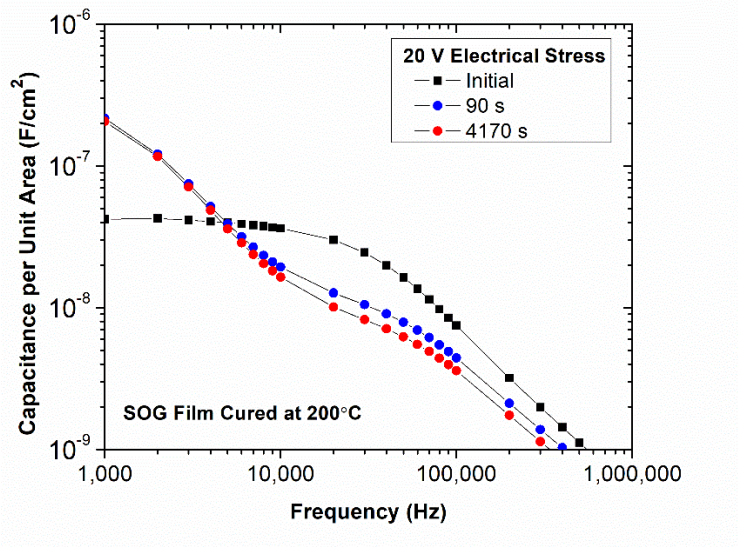

Figure 5. Frequency dependence characteristics for different stress times at 20 V electrical stress.

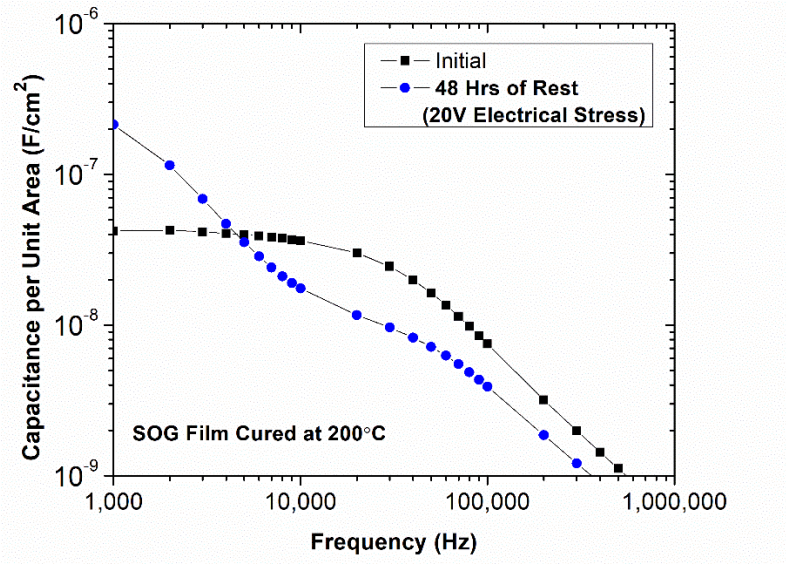

Figure 6. Comparison of the initial and 48 h rested capacitance-frequency characteristics after 20 V electrical stress.

4. Conclusions

The effects of the frequency dependence in a transparent dielectric based on Spin-on Glass under electrical stress is presented. The capacitance-voltage characteristics for the n-type MOS capacitors shows a well-defined accumulation region with very low hysteresis. The low electrical stress induce charge trapping at the dielectric-semiconductor interface (interface charge) which causes variations in the accumulation capacitance. These variations in capacitance are reversible after a period of rest. The results suggest that high electrical stress induce a degradation of the film, resulted by the probable interaction of the residuals within the film with the electrical stress. This behavior is irreversible. This work presents a study to find an optimum range of stability in dielectric films under electrical stress.

Supplementary Materials: The following are available online at https://www.mdpi.com/2673-4591/4/1/2/s1.

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Data Availability Statement: Data is contained within the article.

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