engineering proceedings

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Proceeding Paper

Teaching Experience of Microchip Education during COVID-19 †

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† Presented at the 3rd IEEE International Conference on Electronic Communications, Internet of Things and Big Data Conference 2023, Taichung, Taiwan, 14–16 April 2023.

Abstract: A teaching experience on microchip (chip) education during COVID-19 is shared in this article. The program outcomes obtained and executed in the Teaching Practice Research Program supported by the Ministry of Education (MOE) of Taiwan are described as the teaching experience. In this program, two courses were offered in a semester: (1) Analog IC Design and (2) Full Custom IC Layout. The COVID-19 pandemic interrupted the teaching process, and determining how to maintain the normal teaching process was a significant challenge. The experience in teaching chips during COVID-19 was recorded in the teaching practice research program and shared for the future development of teaching resources.

Keywords: chip design; chip layout; IC education; IC learning; COVID-19 impaction

1. Introduction

The semiconductor industry in Taiwan was valued at TWD 4 trillion in 2022, and the value was over 15% of the gross domestic product (GDP) of Taiwan. Thus, the semiconductor industry is critical to Taiwan's national economy. As machine learning, artificial intelligence (AI), 5G, self-driving cars, virtual reality, cloud computing, and information security continuously develop, the semiconductor demand is growing rapidly. Therefore, human resource development for integrated chip (IC) technology and personnel training for IC design are important tasks. Since 2019 when the first case of COVID-19 was found in China [1,2], its impact has influenced daily life as well as the economy and the teaching-and-learning process in education. Recently, daily life has gradually returned to normal but the impact on education still exists, which is worth reviewing.

The project, Teaching Practice Research Program, was initiated by the Ministry of Education (MOE) of Taiwan in 2020 [3] aiming to improve the teaching quality in university education [4]. In this one-year project, we promoted the basic knowledge and skills of IC design and layout. Two courses including Analog IC Design and Full Custom IC Layout were offered each semester. In Analog IC Design (Course 1), the circuit operation and the principle of the metal–oxide–semiconductor field effect transistor (MOS FET) were introduced and taught. The related sub-blocks of the MOS transistor and circuit such as the current source, current mirror, voltage reference, and single-stage amplifier were described, too. In Full Custom IC Layout (Course 2), lectures on the concept of semiconductor manufacturing and the IC layout technique were given. Students were required to become familiar with related software tools such as IC electronic design automation (EDA). Course 1 was mainly related to theory, while Course 2 was practical training for IC layout skills.

The article is organized into five sections. Section 1 introduces the motivation of the research program. Section 2 describes the background of the semiconductor industrial chain and chip-realization technology. Section 3 describes the lecture of two courses during COVID-19 in detail. The feedback of students is compared with the same courses after COVID-19. Section 4 shows the class activities to improve the student learning achievements. Finally, Section 5 concludes this study.

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Citation: Hung, Y.-C. Teaching Experience of Microchip Education during COVID-19. *Eng. Proc.* **2023**, *38*, 75. https://doi.org/10.3390/engproc2023038075

Academic Editors: Teen-Hang Meen, Hsin-Hung Lin and Cheng-Fu Yang

Published: 10 July 2023

2. Background on Microchip Education

Resistors and inductors in nano-Henry, capacitors in pico-Faraday, and bi-polar junction transistors (BJTs) or metal–oxide–semiconductor field-effect transistors (MOSFETs) can be shrunk in dimension and integrated into a small thin silicon or other material, which is known as an integrated circuit or chip. There are various chips in different packaged forms within modern electronic products. For example, the iPhone 13 contains a 64-bit ARM-based system-on-a-chip (SoC) named Apple A15 Bionic designed by Apple Inc. The A15 is fabricated by Taiwan Semiconductor Manufacturing Company (TSMC) by using 5 nm technology in which 15 billion transistors are included in a die area of one square centimeter. The chip design and manufacturing process are more innovative than conventional sub-micro-fabricated technologies.

The chip fabrication is implemented by a succession of photo-lithography procedures. According to circuit functionality and performance, the circuit schematic is designed by IC designers upon market demand. The corresponding layout diagram is precisely drawn with a computer by IC layout engineers. The layout diagram comprises various colorful forms of rectangles depending on the circuit schematic, in which each color represents one thin-film material or doped action. After this step, the layout diagrams are transferred and fabricated in a set of photomasks (or reticles). The generated photomasks are used in photo-lithography processes to create the specific structure of related thin-film material. The photo-lithography procedures are repeated until the whole chip structure is constructed. Finally, the finished chip wafer is packaged and tested. The aims of the chip's packaging include protection of the bare die, heat removal, and electrical and signal connection, whereas that of the IC test includes general performance verification. Figure 1 shows the whole process of chip production from the circuit design to a standalone device element. A functional chip is manufactured through a complicated process. However, in university education, priority is given to determining how to increase the students' learning interests and promote IC layout design knowledge and skills. As the IC industry is so important, many researchers are studying to improve the teaching and education of chip-related knowledge [5–11].

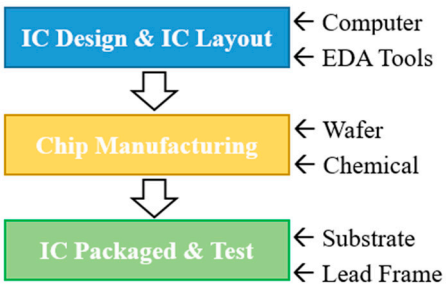

Figure 1. Chip realization process.

3. Teaching Process and Experiences in Chip Education

Lectures for two courses were given from August 2020 to July 2021. Lectures for Course 1 and Course 2 were given in one semester sequentially. In universities in Taiwan, each semester has eighteen weeks, and a course has one to three hours each week. In this research program, the two courses had three lessons each week with fifty-four hours of lectures in one semester. The teaching process was impacted by COVID-19.

3.1. Course 1: Analog IC Design

Course 1 was an elective course for junior or senior students, and 42 students enrolled in the course. The major content of the course included the basic concept of semiconductor technology, the semiconductor manufacturing process, the principle of metal–oxide–semiconductor (MOS) field-effect transistor (FET) operation, a small-signal equivalent circuit, a sub-block analog switch, a bias circuit, a current source, a current mirror, and the

design of a single-stage amplifier. The course content was integrated with two courses to give students the whole outline of analog IC design: Microelectronic Circuits and IC technology. Due to the circuit complexity, we helped students understand the basic operating theorem of the MOS transistor. When students had the correct concept of MOSFET operation, that knowledge could become useful and available. Based on the correct knowledge, students can understand the MOS circuit design and analysis. Therefore, in the teaching strategy, it was planned to give a two-hour instruction in the beginning and a one-hour practice later. All class assignments and additional materials were included in the learning portfolio. Each student in this course was assigned a personal portfolio. After students completed their assignments, the portfolio was submitted for examination and scoring. Praise and encouragement with candies or beverages to students with high achievements encouraged them to be motivated to learn. Encouraging rather than criticizing seems to be a better educational idea.

In the class, teachers gave instructions in the first two lessons, and then students practiced class assignments in the third lesson. In the meantime, students were encouraged to discuss the assignments with classmates to find the proper solutions from information on the internet. The learning outcomes were evaluated from the individual portfolio. Finally, teachers evaluated and encouraged students for their performance and achievement. Three learning models with instruction, practice, and praise were used in the learning cycle, as shown in Figure 2. In the model, students were not passively receiving information or unidirectionally learning but actively surveyed related information. Compared to traditional teaching, a positive learning recycle was created for higher learning efficiency. Even during COVID-19, teaching activities for Course 1 were not impacted significantly, due to the preventive measure.

Figure 2. Three learning situational models in our teaching strategy.

3.2. Course 2: Full Custom IC Layout

In Course 2, it was also planned to have three lessons every week with 40 students. The course focused on practicing IC layout skills. Electronic design automation (EDA) software authorized and approved by Taiwan Semiconductor Research Institute (TSRI) was used in the laboratory as this course demanded students to manipulate the EDA software. The content of the course included the basic concept of the semiconductor manufacturing process, the various methodologies of chip realization, UNIX command, a cross-sectional view of the CMOS transistor, a circuit schematic, an IC layout drawn in the EDA software environment, and IC verifications using design-rule-check (DRC) and layout-vs.-schematic (LVS). In the course, many teaching aids were provided such as Microsoft PowerPoint animations to show the three-dimensional structure of the MOS transistor and its overall structure. A micrographic image of the real chip was observed by using optical microscopes. For the understanding of the CMOS chip process, CMOS logic gate, stick diagram of the layout, and the design of adders, assignments were given in lectures including building a physical layout diagram for the MOS transistor. Teaching aids such as color papers and glue were used to construct the MOS transistor. The auxiliary teaching activities increased students' interest. Since the course aimed to train students using the IC layout EDA tool,

every student was required to use computers. The whole practice was instructed to teach the background and conception and to demonstrate how to build the chip layout step by step by teaching assistants (TAs).

From May 2021, the outbreak of COVID-19 made all schools practice online education in Taiwan. There was still a quarter of the semester until the end of the course. The remaining subjects were important as students needed to finalize their projects and practice computer skills. Thus, how to continue the course was a significant challenge for skill training. The following principles were followed for the course to be continued in distance learning, too.

1. In distance learning, we used Google Meet, Microsoft Teams, or Cisco WebEx to connect and share information with all students at home.
2. Although students could not come to school, the practice of the IC layout skill was continued by using a virtual private network (VPN). The student at home used a personal computer to connect to the layout server through the school network gateway to accomplish the final layout project. Even though the bandwidth was limited, the course continued as normal as before.
3. Lectures on layout skills were provided as video files with the help of teaching assistants. Students repeatedly watched the video during the course.
4. An information platform for the course was offered for exchanging information and announcing the submission status of the final project. We used LINE and Google Drive to construct an information platform. LINE is a freeware app for instant communications, operating on smartphones and personal computers. Google Drive was developed by Google to allow users to store files in the cloud via internet access. The two services are popular in Taiwan. Therefore, the enrolled students and teachers exchanged information and communicated conveniently on the platform.
5. Using the above methods, course-related information on the platform became open and transparent, and students were encouraged and supervised in the course. Each student understood the status of all classmates' final project progress. At the end of the course, 38 enrolled students remained. A total of 36 students completed the final project and fulfilled the requirements with the achievement rate for the IC layout project of 95%. Teachers and students put a lot of effort into learning the course.

A questionnaire was created for the evaluation including various aspects such as teaching strategy and attitude, lecturing skill, learning assistance, learning outcomes, course attention, and self-evaluation. Twenty-one items were contained in this questionnaire. A five-point Likert scale was used for this questionnaire with scores for strongly disagree, disagree, neither agree nor disagree, agree, and strongly agree. The feedback data for teaching were extracted from the school's teaching historical database. Table 1 shows the results of the students' evaluation for the courses, with scores of 4.68 and 4.87.

Table 1. Feedback results of student questionnaires.

Year_Semester	Course 1	Course 2
2014_2	4.79	4.79
2015_2		4.37
2016_1	4.14	
2016_2		4.42
2017_2	4.12	
2018_1	4.39	
2019_1	4.49	
This Study * 2020_1	4.68	
This Study * 2021_2		4.87

* The period of the project execution is from the first semester year of 2020 to the second semester year of 2021.

"Slow and steady wins the race", "Learn to walk before you run", and "Practice makes perfect" were also applied to the teaching of the courses. Since the state-of-the-art IC technologies have been scaled down to the order of nanometers, to maintain high-sensitivity performance, the chip design and layout have become complicated. Therefore, the learning process must be exciting to improve the learning efficiency. Students need to have a firm and clear grasp on basic concepts of the IC processes, design, and layout technology. Step-by-step learning and deep thinking in circuit theory and transistor operation are essential to enhance basic abilities. In the practice experiments of distance learning, video software and apps for instant communications between teachers and students were useful to exchange information.

4. Related Activities

In the research program, many exercises for IC circuit analysis were organized for students. Every student had an individual learning portfolio. According to the progress, every student practiced related skills after the teacher's instruction. During the practice, students were encouraged to find the proper solutions by themselves through discussion with classmates. Figure 3 shows the learning material and small rewards for students. Figure 4 shows a snapshot of the students' practice during Course 1. To relieve study fatigue, the practice was usually scheduled on the third hour after giving a two-hour lecture. Figure 5 shows students using personal computers to practice IC layout skills in Course 2. In Course 2, TAs helped students manipulate the layout software and answered questions.

Figure 3. Learning material and rewards for students.

Figure 4. Students' practice in Course 1.

Figure 5. Students used computers to practice IC layout skills in Course 2.

Figure 6 shows the TA's demonstration of using the IC layout software. To verify the learning outcomes, a midterm practice test was carried out. All students were grouped and sequentially tested for building the circuit schematics. Figure 7 shows the midterm test in Course 2. In the program, teaching aids were self-made for the demonstration of the CMOS transistor structure and the corresponding layout diagram. Figures 8 and 9 show the structure of the MOS transistor in a three-dimensional view and visual aids of the IC layout.

Figure 6. Teaching assistant (TA) instructs and guides the students for IC layout.

Figure 7. The midterm practice test of Course 2 (Full Custom IC Layout).

Figure 8. The teaching aid for structure of MOS transistor in three-dimensional view.

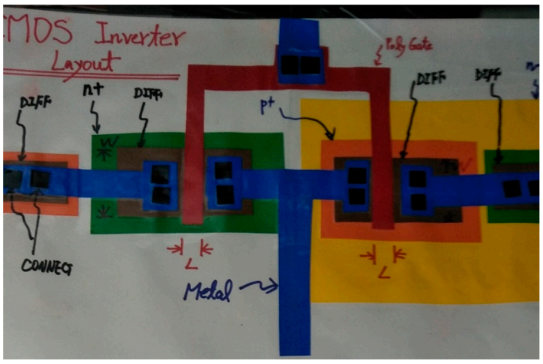

Figure 9. The demonstration aid for IC layout.

Figure 10 shows the samples of students' assignments. In Course 2, silicon wafers, packaged chips, and bare dies are shown. Figure 11 shows the teaching aids and their demonstration. Figures 12 and 13 show students' layout diagrams under the requirements of design-rule-check (DRC) and layout-versus-schematic (LVS). The two IC layout diagrams for the eight-bit adder were sampled from students' final projects. Due to the COVID-19 pandemic, the lecture was difficult to offer. Part of the layout was created in on-site classes, and the remaining part was completed in distance learning.

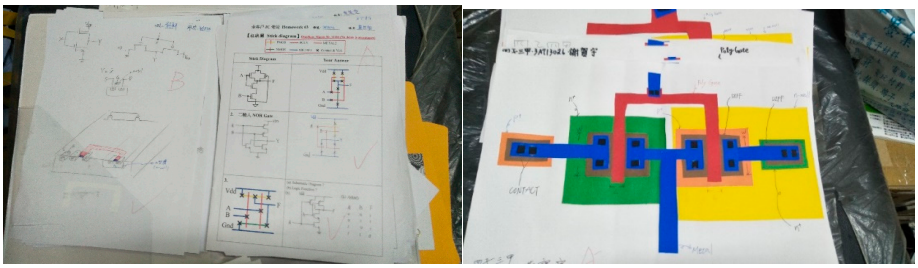

Figure 10. Students' assignments during Course 2.

Figure 11. Wafer and chip physical demonstration by using an optical microscope.

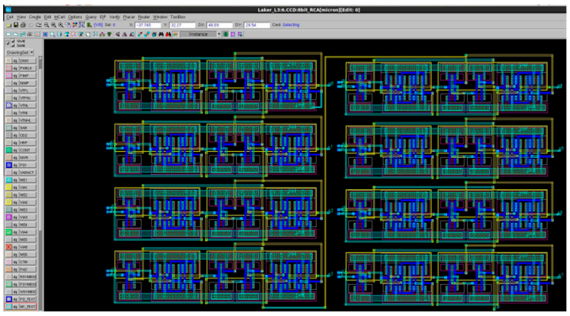

Figure 12. Student's report for the final project.

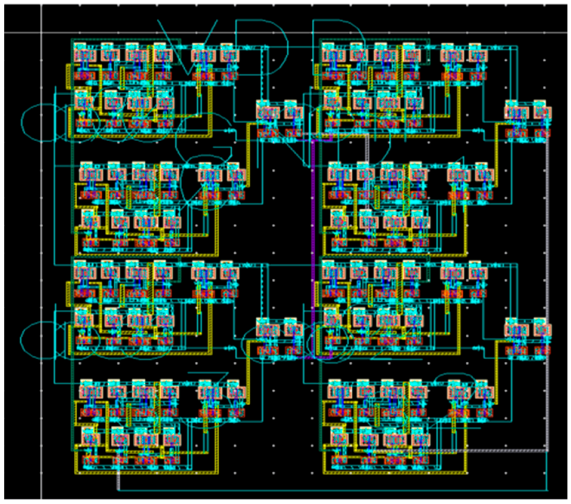

Figure 13. Student's report for the final project.

How to resolve the layout problem efficiently online was a challenge for effective learning. During distance learning, students were required to make a self-test via the internet and self-evaluate the learning outcomes. The quizzes were conducted by using Google Forms. Figure 14 shows the samples of these quizzes created in Google Forms. To improve students' practical ability in the IC layout, we invited IC engineers to give lectures. Figure 15 shows the lecture given by the IC engineers. The overall goal of the research program was achieved with rich and heuristic class activities, and students achieved satisfactory learning results in IC technology, circuit analysis, and IC layout skill.

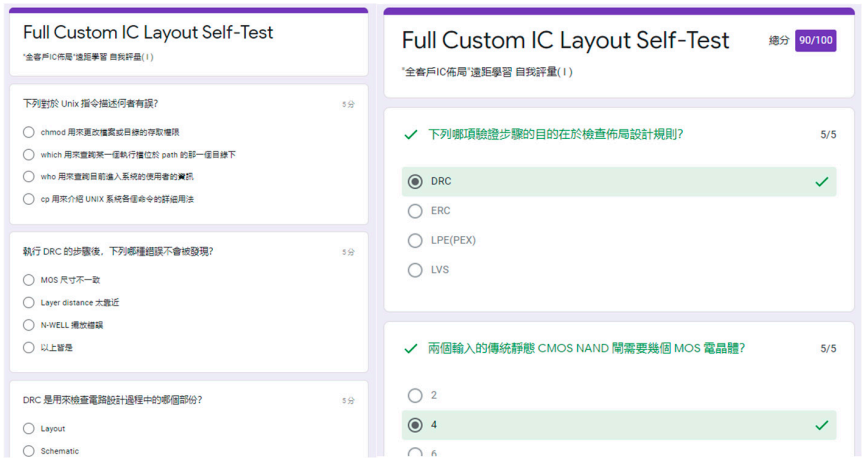

Figure 14. Student's self-test on the internet to self-evaluate the learning outcomes.

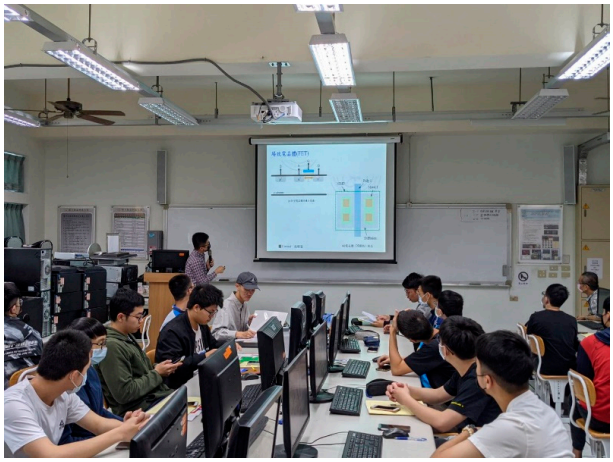

Figure 15. An industry IC engineer was invited to give lectures.

5. Conclusions

Due to the outbreak of COVID-19 in the late stage of Course 2, a proper teaching method needed to be found for distance learning. With internet technology, TAs, and the joint efforts of students, the course continued without interruption. The achieved rate of the IC layout project reached 95%. The student's evaluation results showed that the teaching achievement of the courses was the best compared to the historical data. A new and interesting teaching process in the courses during the period of COVID-19 was achieved in cooperation with the school, students, and teachers owing to internet technology.

Funding: This research was funded by the Teaching Practice Research Program, 2020, Ministry of Education (MOE), Taiwan, R.O.C., grant number No. PEE1090359.

Informed Consent Statement: Informed consent was obtained from all subjects involved in the study.

Data Availability Statement: Data Availability Statements are available in the National Chin-Yi University of Technology, Taichung, Taiwan, R.O.C. at https://evaluation.ncut.edu.tw/ (accessed on 1 September 2021).

Acknowledgments: This work was supported by the Teaching Practice Research Program (No. PEE1090359), Ministry of Education (MOE), Taiwan, R.O.C. We would like to express our sincere thanks to the National Chin-Yi University of Technology, Taiwan for full support and all students who participated in this project. Thanks to teaching assistant Wei-Jen Lin for the video recording and help with the IC layout in the classroom.

Conflicts of Interest: The authors declare no conflict of interest.

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