



Yue Liu 🝺, Jifang Qiu *ⓑ, Chang Liu, Yan He 🖻, Ran Tao 🖻 and Jian Wu

School of Electronic Engineering, Beijing University of Posts and Telecommunications, Beijing 100876, China; LYmoon@bupt.edu.cn (Y.L.); liuchang345@bupt.edu.cn (C.L.); heyan@bupt.edu.cn (Y.H.); taoran2018@bupt.edu.cn (R.T.); jianwu@bupt.edu.cn (J.W.)

* Correspondence: jifangqiu@bupt.edu.cn

Abstract: An optical analog-to-digital converter (OADC) scheme with enhanced bit resolution by using a multimode interference (MMI) coupler as optical quantization is proposed. The mathematical simulation model was established to verify the feasibility and to investigate the robustness of the scheme. Simulation results show that 20 quantization levels (corresponding to 4.32 of effective number of bits (ENOB)) are realized by using only 6 channels, which indicates that the scheme requires much fewer quantization channels or modulators to realize the same amount of ENOB. The scheme is robust and potential for integration.

Keywords: analog-to-digital converter; optical phase-shift quantization; ENOB

1. Introduction

High-speed analog-to-digital converters (ADC) play an important role in modern signal processing, such as high-frequency radar systems [1–5], wireless communications [6,7], and image processing [8,9], etc. However, with more and more wideband applications, such as wireless and radar communications especially when the bandwidth of radar signals is over 10 GHz, traditional electronic ADCs have been unable to meet the requirements of high speed due to timing jitter, thermal noise and uncertainty of electronic components, and so on. In recent years, with the rapid development of photonic technology, using photonic technology to break through the bottleneck of electronic ADC has become a research hotspot in the field of optoelectronic technology [10]. The advantage of using photonic technology in ADC is that the sampling rate can be up to 100GS/s (samples per second) or even higher. Moreover, the timing jitter of the optical pulse can reach the level of femtosecond [11,12], which is two orders of magnitude smaller than that of the electrical sampling pulse. In addition, the pulse width can be compressed to the order of picoseconds or even femtoseconds by using pulse compression technology [13]. Therefore, optical analog-to-digital conversion (OADC) technology has significant advantages compared with traditional electronic ADC technology. In general, OADC has great potential not only in terms of high speed, high precision, and wide bandwidth, etc., but also in commercial applications due to the great development of photonic integration. Thus, it has become one of the main development directions of high-speed ADC.

In last decades, lots of optical-sampling electrical-quantization [14,15] and opticalsampling optical-quantization schemes have been reported, which can be divided into two categories, i.e. intensity-to-wavelength optical quantization and phase-shift optical quantization (PSOQ). Intensity-to-wavelength optical quantization [16,17] usually realizes intensity to wavelength conversion by using nonlinear effects via nonlinear devices, like highly nonlinear fiber (HNLF). However, the length of HNLF is usually up to km level and the optical power required is relatively large to excite the nonlinear effect. On the other hand, the PSOQ scheme, which was firstly proposed by Taylor [18] and then developed in [19–23], typically uses electro-optic modulators with multiplied half-wave voltages. The



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Copyright: © 2021 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (https:// creativecommons.org/licenses/by/ 4.0/). advantages of Taylor's and its developed schemes are potentiality of on-chip integration and have low requirement of input optical power due to operation principle based on optical interference. In general, in Taylor's and its developed schemes, optical quantization of *N* bit requires *N* modulators. To further increase the quantization bits, the half-wave voltage of the last modulator must be significantly reduced. Therefore, we previously proposed a cascade step-size (CSS) multimode interference (MMI) coupler-based phase quantization scheme [24] requiring only one phase modulator (PM). In the scheme reported in [24], in order to realize *N* bit, only one phase modulator and a CSS-MMI with 2^{*N*-1} output channels are needed. This scheme avoids the increasing requirement of the number of modulators when *N* increases in the schemes developed from Taylor's scheme, and eliminates the need for ultra-low half-wave voltage of modulators. However, when *N* is larger, the number of output channels (*K*) increases significantly (for example, when *N* is 4.17 bit, *K* is 9; whereas *N* is 5.09 bit, *K* is 17, and so on), resulting in enormous difficulties in design and fabrication of CSS-MMI.

In this paper, in order to obtain effective number of bits (ENOB) as high as possible in OADC with the required number of modulators and optical output channels as fewer as possible, we propose a new PSOQ scheme of OADC, which effectively increases the number of quantization bits but requires much fewer optical channels and modulators. We numerically demonstrate the scheme with 6 optical channels and 2 modulators by using a 1×4 MMI, a 3×5 MMI, a PM, and a Mach-Zehnder modulator (MZM), which can achieve 4.32 bit. Compared with our previously proposed scheme [24], which needs 9 optical channels to achieve 4.17 bit, this new scheme is easier for design and fabrication. Moreover, we investigated the performance of the proposed scheme by building up a simulation system, and found that compared with the previous scheme, the proposed scheme not only has much fewer output channels, but also has more robustness in presence of timing jitter, intensity noise of optical sampling pulses, and MMI power imbalance.

2. Principle of Operation

The schematic diagram of the proposed OADC is shown in Figure 1. It consists of an optical sampling module, an optical quantization module, and an electrical back-end processing module. The optical sampling module is composed of a pulse laser, a 1×4 MMI (MMI^{1st}), and a PM. The optical quantization module is composed of a 3×5 MMI (MMI^{2nd}) and an MZM. The digital signal processing module is composed of photo-detector (PD) arrays and electric comparator arrays.



Figure 1. Schematic diagram of the proposed 4.32-bit optical analog-to-digital converter (OADC). RF input: Radio-frequency input. PM: phase modulator, MZM: Mach-Zehnder modulator, PD: photo-detector, DSP: digital signal processing.

Firstly, in the optical sampling module, assuming that the injected high-speed pulses emitted by the pulse laser are solitary pulses with Gauss shape, can be represented as

$$E_{in} = \sum_{n=-\infty}^{n=+\infty} R_G(t - nT_S)$$
⁽¹⁾

where $R_G(t) = \sqrt{P_{max}} \cdot e^{-2 \cdot (\frac{t}{T_{FWHM}}^{2m})} \cdot e^{(2\pi f_0 t + \varphi_0)}$, $T_S(T_S = 1/f_S)$ is the sampling rate. P_{max} is the peak power of the pulse. The full width at half maximum power (FWHM) pulse duration is T_{FWHM} and m denotes the order of the super-Gaussian function. The carrier frequency of the optical pulse is defined by emission frequency f_0 and the initial phase is φ_0 . Therefore, the schematic of waveforms of the sampling pulses is shown in Figure 2a.



Figure 2. The proposed OADC with sinusoidal RF input. (**a**) Waveforms and frequency spectrum the high-speed optical sampling pulses. (**b**) Spectral response of both modulators. (**c**) The outputs of 6 channels under single-frequency sinusoidal input signal. (**d**) Spectral response of PDs. (**e**) power spectrum. (**f**) Transmission curves of 6 optical channels and digital output codes with input voltage.

The high-speed pulses E_{in} are divided into four channels with equal power by MMI^{1st}, the outputs of MMI^{1st} can be described as

$$\begin{bmatrix} E_{s2} \\ E_{p2} \\ E'_{s1} \\ E_{p1} \end{bmatrix} = \frac{1}{2} \begin{bmatrix} e^{j0} \\ e^{j\frac{\pi}{2}} \\ e^{j\frac{\pi}{2}} \\ e^{j0} \end{bmatrix} \cdot E_{in}$$
(2)

After splitting, optical pulse E'_{s1} passes through PM which is driven by input signal $V_{in}(t)$, and becomes E_{s1} as

$$E_{s1} = E'_{s1} \cdot e^{j\Delta\Phi_{s1}(t)}, \ \Delta\Phi_{s1}(t) = h_{m1}(t) * (V_{in}(t) + V_{b1})$$
(3)

where $h_{m1}(t)$ is the equivalent model of a phase modulator which reflects the high frequency characteristics of the phase modulator. The electronic frequency response is shown as Figure 2b, where f_m is the frequency of the RF (Radio-frequency) input. $\Delta \Phi_{s1}(t)$ can be equivalent to $\frac{\pi(V_{in}(t)+V_{b1})}{V_{\pi}}$, where V_{π} and V_{b1} are the half-wave voltage and bias voltage of PM, respectively. $\Delta \Phi_{s1}(t)$ is induced by $V_{in}(t)$. Then E_{s1} is injected at the middle position of MMI^{2nd}, while E_{p1} and E_{p2} are injected at positions as

$$\kappa = \frac{K \pm 2}{2K} W_2 \tag{4}$$

where *K* is the number of MMI^{2nd} output channels, here *K* = 5. After carefully choosing the dimensions of MMI^{2nd} , *K* images of equal intensities can be formed at MMI^{2nd} output. The output power can be expressed as

$$I_{i}(t) = \begin{cases} \frac{2\sqrt{2P}}{K} \left(\frac{3\sqrt{2}}{4} + \cos\left(\Delta\Phi_{s1}(t) + \frac{i}{2} \cdot \frac{2\pi}{K} - \frac{3\pi}{4} \right) \right) & \text{for even } i \\ \frac{2\sqrt{2P}}{K} \left(\frac{3\sqrt{2}}{4} + \cos\left(\Delta\Phi_{s1}(t) - \frac{i-1}{2} \cdot \frac{2\pi}{K} - \frac{3\pi}{4} \right) \right) & \text{for odd } i \end{cases}$$
(5)

where i = 1...5. From Equation (5), we can see that the output power of each channel varies sinusoidally with $V_{in}(t)$ as shown in Figure 2f. This is similar to [24] and acts as quantizer which can realize 10 quantization levels (corresponding to 3.32 bit). The output pulses of each channel are shown in Figure 2c. Based on the principle in [24], in order to extend the ENOB, the 3×5 MMI should be replaced by a 3×9 MMI, thus OADC can be extended to 18 quantization levels, which means a 4.17 bit OADC with 9 output channels is obtained.

In this paper, we propose a new scheme to extend the ENOB by introducing a MZM. As shown in Figure 1, the MZM with a half-wave voltage of $2V_{\pi}$ is introduced parallel to the PM, with E_{s2} as input. The output power of MZM can be expressed as

$$I_6(t) = \frac{P}{2}(1 + \cos(\Delta\Phi_{s2}(t))), \Delta\Phi_{s2}(t) = h_{m2}(t) * (V_{in}(t) + V_{b1})$$
(6)

where $h_{m2}(t)$ is the numerical model of MZM and reflects the high frequency characteristics of the MZM. $\Delta \Phi_{s2}(t)$ is equivalent to $\frac{\pi(V_{in}(t)+V_{b2})}{V_{\pi}}$, V_{b2} is the bias voltage applied to MZM.

After the optical-to-electrical (O/E) conversion performed by the PD arrays, we can obtain the electrical signal as

$$V_i(t) = [(I_i(t) + I_n(t)) \cdot h_p(t)] \cdot R_L \quad i = 1 \dots 6$$
(7)

 $I_n(t)$ is the noise current caused by PD in each channel, $h_p(t)$ is the equivalent circuit model of PD as shown in Figure 2d and the power spectrum of $V_i(t)$ is Figure 2e. R_L is load resistance that converts current into voltage output.

Next, the detected signals of the 6 output channels are injected into the electric comparator arrays, judged to "0" or "1" by appropriate threshold as

$$D_{i}(n)|_{t=nT_{s}} = \begin{cases} V_{oh}, & V_{i}(t) - V_{th} > V_{in.min} \\ V_{ol}, & V_{th} - V_{i}(t) > V_{in.min} & i = 1...6 \\ D_{i}(n-1), & |V_{th} - V_{i}(t)| < V_{in.min} \end{cases}$$
(8)

Generally, $V_{oh} = 1$ and $V_{ol} = 0$. V_{th} is the threshold voltage of electric comparator arrays, $V_{in.min} = \frac{V_{oh} - V_{ol}}{A_v}$ is the minimum identification precision voltage, which is related to the conversion precision A_v of the comparator. The higher the A_v is, the smaller the $V_{in.min}$ will be, which shows that the comparator has more accurate comparison results.

At last, after processing these digital signals according to the electronic decision rules as shown in Figure 2f, we can get 20 different quantization levels. We can see from Figure 2f

that, the transmission periods of Channel 1 to Channel 5 are $2V_{\pi}$. For Channel 1 to Channel 5 we can obtain 10 quantization levels range from 0 to $2V_{\pi}$, and the encoding is repeated within $2V_{\pi}$ to $4V_{\pi}$. Channel 6 is synchronized with other channels, but the transmission period is $4V_{\pi}$. By combining all 6 channels, 20 quantization levels are obtained in the input voltage ranging from 0 to $4V_{\pi}$. Compared with our previously proposed scheme (where 18 quantization levels are obtained with 9 output channels), the proposed scheme needs fewer channels (6 channels) to obtain equivalent quantization levels (i.e., ENOB).

3. Simulation Modelling and Performance Analysis

Based on the above models, the OADC is built up to verify the feasibility and investigate the performance of the proposed OADC scheme, as shown in Figure 3. We analyze the OADC performance based on IEEE standard [25], where ENOB is derived as [25]

$$ENOB = \frac{SINAD - 1.76 \text{ dB}}{6.02} \tag{9}$$

SINAD (signal-to-noise ratio) well reflects the overall dynamic performance of the ADC because it includes all factors that constitute noises and distortions. Based on IEEE standard, SINAD is calculated from the frequency spectrum of the digital output codes of the ADC as

$$SINAD = 10lg \frac{\sigma_x^2}{\sigma_q^2 + \sigma_n^2} \tag{10}$$

where σ_x^2 is the electrical signal power, σ_q^2 and σ_n^2 represent inherent quantization errors and errors caused by other noise, respectively.



Figure 3. Schematic of and simulation results of the proposed OADC. AMLL: active mode-locked laser; Demux: wavelength division multiplexer. Mux: wavelength division multiplexer. TDL: time delay line; VOA: tunable optical amplifier; PS: power splitter; MMI1st: 1×4 MMI. MMI2nd: 3×5 MMI. PD: photo-detector. Com: electronic comparators. PLL: phase-locked loop. (**a**) 50 GHz optical pulses are generated by time-wavelength interleaving. (**b**) S21 response and half-wave voltage change with input RF signal. (**c**) FFT spectrum of digital output codes.

We use time-wavelength interleaving (T-W interleaving) to acquire optical sampling pulses with $f_s = 50$ GHz. The waveforms of the output of active mode-locked laser (AMLL) is shown in Figure 3a, whereas the time-wavelength interleaved sampling pulses are shown in Figure 3a. A sine wave signal of 7.01 GHz was used to act as an electrical analog signal, which is divided into two by power splitter (PS), one of which is used to drive the PM, while the other one is used to drive the MZM. Based on the principle analysis, the ideal ENOB is 4.32 bit. Then we took imperfections in the actual system into account to calculate the ENOB. Table 1 shows the main simulation parameters of the OADC. The parameters chosen in Table 1 are based on the datasheet of commercially available devices.

Component		Parameter	Value	
Pulse laser		P_{max} / Intensity jitter Sampling rate / Timing jitter T_{FWHM}	0 dBm/2% 12.5 GHz/100 fs 0.5 ps	
T-W	Demux/mux	Bandwidth Channel interleaving	150 GHz 250 GHz	
interleaving	TDL	Time delay	0 ps 20 ps 40 ps 60 ps	
	VOA	Amplification power	Related with each channel	
Modulator	РМ	Analog bandwidth half-wave voltage	25 GHz 3.3 V(@1 GHz)	
	MZM	Analog bandwidth half-wave voltage	25 GHz 6.6 V(@1 GHz)	
MMI		Normalized channel power imbalance	0.943 1.010 1.027 0.884 1.136	
PDs		Bandwidth R _L Dark current thermal noise	40 GHz 50 Ω 5 nA Related with bandwidth and	
		shot noise	resistance Related with pulse power	
Comparators		Offset voltage A_v	1 mV 30 dB	
PLL		RMS(J _{per})	63 fs	

Table 1. Main parameters and values of the OADC in simulation.

For example, the parameters of AMLL was chosen based on the datasheet of Calmar PS-10-TT series, like timing jitter is 100 fs, the standard deviation of random intensity noise (RIN) is 2% relative to the pulse peak power, and the T_{FWHM} of the Gaussian pulse train is 0.5 ps, peak power is 0 dBm, and wavelength is 1560 nm.

As for modulators, with the increase of input RF frequency, RF and light wave speed mismatch and transmission loss caused by the structural parameters of lithium niobate modulator increase as well, which in turn affects the output optical signal. Therefore, it is important to analyze the performance of OADC under this influence. The RF response of modulator can be represented by S21 response, which decreases with the input frequency increasing. This will affect the OADC output phase $\Delta \Phi_{s1}(t)$ and $\Delta \Phi_{s2}(t)$ as shown in Figure 3b. In our simulation, the half-wave voltages of PM and MZM were set as 3.3 V@1 GHz and 6.6 V@1 GHz referring to the commercial modulator, and the S21 data of commercial devices were taken into account. MMI transmission curves were obtained according to measurement results based on our fabricated MMI [26], which has normalized channel power imbalance of [0.943 1.010 1.027 0.884 1.136], leading to non-uniform quantization and thus decreasing the ENOB of the OADC.

In the electronic processing module, the parameters of PD were chosen according to the silicon germanium PIN structure photodetector mentioned in [27–29], as bandwidth

of 40 GHz, a load resistance of 50 Ω , dark current of 5 nA, electronic measurement bandwidth and resistance-related thermal noise, and shot noise related to input optical power. Similarly, the parameters for electrical comparators were set with reference to the offset voltage and minimum conversion accuracy A_v of commercial electrical comparators (ADI, MP582). The electrical components are synchronized with the active mode-locked laser (AMLL) through a phase-locked loop (PLL). The root mean square period jitter (RMS(J_{per})) caused by phase noise of PLL internal electronic circuits is set to 63 fs according to commercial PLL (Texas Instruments, LMX2820).

At last, according to the output digital code and f_s , the frequency of the input signal is calculated according to the FFT calculation result and Equation (9) as shown in Figure 3c, which is consistent with the given input signal f_m , verifying the correctness of the simulation modelling, the SINAD is calculated to be 26.03 dB. Therefore, the ENOB is 4.03 bit, which is a little slighter than the ideal ENOB of 4.32 bit and demonstrates the accuracy of the simulation modelling of the proposed OADC scheme.

Table 2 compares the performance of different reported schemes based on PSOQ, "-" in Table 2 means that CW (continuous-wave) light was used or non-mentioned in the schemes. We can see from Table 2 that our proposed scheme has a simpler structure due to the fact that the optical quantizer is a passive device and has fewer optical channels and accepted number of modulators, which is a potential for on-chip integration (similar optical quantizer with 5 channels has already been experimentally reported [26]).

Schemes	Year	Type of Result	Sampling Rate	Signal Input	Quantization Type	Number of Modulators	Number of Optical Channels	ENOB
[19]	2011	Experimental	-	10 GHz	PSOQ	1	8	3.2
[20]	2011	Simulated	20 GHz	-	PSOQ	1	8	4
[21]	2014	Simulated	-	25 GHz	PSOQ	1	24	5.28
[22]	2018	Experimental	-	400 MHz	PSOQ	3	8	3.31
[24]	2018	Simulated	-	-	PSOQ	1	5	3.27
[23]	2020	Experimental	-	500 MHz	PSOQ	3	10	3.75
This work	2021	Simulated	50 GHz	7.1 GHz	PSOQ	2	6	4.03

Table 2. The performance comparisons of OADC schemes.

Next, in order to investigate the robustness of the OADC, we investigated the factors that RIN and timing jitter of the pulse source, the MMI channel imbalance and signal noise, phase noise of PLL on ENOB.

3.1. RIN and Timing Jitter

The actual optical sampling pulse has timing jitter, RIN, and limited pulse width. These characteristics of the optical pulse cause errors in sampling process, reduce the SINAD of the OADC, and degrade the ENOB. It is important to investigate the effects of RIN and timing jitter, as both time-wavelength interweaving and back-end electrical processing also lead to mismatches and amplitude fluctuations throughout the OADC. Therefore, we investigated the impact of RIN and timing jitter on ENOB. RIN is defined as $\frac{\delta I}{P_{max}}$, where δI is intensity noise, and P_{max} is pulse peak power. Full scale modulation is assumed in the calculation and the amplitude of the RF input is *A*. Therefore, the error caused by RIN can be substituted into Equation (10) to calculate SINAD

$$SINAD = \begin{cases} \frac{A^{2}/2}{\left(\frac{2A}{N}\right)^{2} + (2K+1)\left(\frac{\arcsin\frac{RIN}{1+RIN} \cdot 2A}{2\pi/N}\right)^{2} \cdot \frac{2}{N}} & K = 5, N = 20\\ \frac{A^{2}/2}{\left(\frac{2A}{N}\right)^{2} + K\left(\frac{\arcsin\frac{RIN}{1+RIN} \cdot 2A}{2\pi/N}\right)^{2} \cdot \frac{2}{N}} & K = 9, N = 18 \end{cases}$$
(11)

Timing jitter can be defined as δT . The judgment time of the sampling pulse is $t = nT_s$. According to the power shape is given by $P(t) = |R_G(t)|^2$, Equation (7), we can calculate the SINAD caused by timing jitter as following

SINAD =
$$\begin{cases} \frac{A^2/2}{\left(\frac{N}{N}\right)^2 + \sum_{i=1}^{i=K+1} \frac{1}{T_s} \int_0^{T_s} [V_i(t) \cdot | P(t-\delta T) - 1|]^2 dt} & K = 5, N = 20\\ \frac{A^2/2}{\left(\frac{2A}{N}\right)^2 + \sum_{i=1}^{i=K+1} \frac{1}{T_s} \int_0^{T_s} [V_i(t) \cdot | P(t-\delta T) - 1|]^2 dt} & K = 9, N = 18 \end{cases}$$
 (12)

It can be seen from Equation (12) that SINAD is related to T_s and the frequency f_m of the input signal. $f_s = 100$ GHz is set in the calculation. SINAD degrades when RIN increases, which can be theoretically obtained as shown in Figure 4a. As shown in Figure 4b, SINAD drops faster when f_m increases, because there is a greater risk of error in judgment time.



Figure 4. SINAD degradation induced by the high-speed pulse RIN and time jitter. (a) Theoretical calculation of the effect of RIN on SINAD. (b) Theoretical calculation of the effect of timing jitter on SINAD with different f_m . The straight lines represent the proposed 6-port scheme and the dashed lines represent the previous 9-port scheme.

We demonstrate how RIN and timing jitter affect system performance from the mathematical model. We carried out the simulation operation when sample rate of optical pulse is 100 GHz and $f_m = 24.9$ GHz in our simulation modelling. The final 2¹⁵ digital codes were selected to calculate FFT and the final ENOB was obtained. Here, P_{max} equals to -5 dBm, we changed RIN from 0 to 10%, timing jitter from 0 ps to 1 ps. The results of ENOB vs. timing jitter and RIN are shown in Figure 5a as a 3D graph. The same investigation was also carried out for our previously 9-port scheme with equivalent ENOB for comparison. The results of the previous 9-port scheme are shown in Figure 5b. We can see from Figure 5 that ENOB decreases greatly with the increase of RIN and timing jitter. When ENOB degrades by 1 bit, in Figure 5a, RIN tolerance is 9.6%, while in Figure 5b RIN tolerance of our previous 9-port scheme is 5.3%. The results indicate that the new proposed OADC has lower requirements on RIN of the sampling pulses. As for timing jitter, we can see that when ENOB degrades by 1 bit, the tolerance of timing jitter is 0.5 ps, while the previous 9-port scheme is 0.4 ps as shown in Figure 5b. The results indicate that the proposed scheme is more robust to timing jitter.



Figure 5. ENOB degradation induced by RIN and time jitter of the optical sampling pulse. (**a**) Simulation results of proposed 6-port scheme. (**b**) Simulation results of previous 9-port scheme.

3.2. Channel Imbalance

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Channel equalization refers to the consistency in amplitude of the modulation curve outputs of the quantizer (MMI^{2nd}). The channel imbalance of the MMI^{2nd} may be caused by manufacturing process errors, or design errors. Therefore, it is important to investigate the effect of channel imbalance of MMI^{2nd} on ENOB.

The power imbalance of each channel is expressed by $\delta P_i = \frac{P_i}{(\sum_{i=1}^{K} P_i)/K}$, $i = 1 \dots K$. Therefore, the SINAD under the error caused by channel imbalance is given by

$$SINAD = \begin{cases} \frac{A^{2}/2}{\left(\frac{2A}{N}\right)^{2} + 2\sum_{i=1}^{i=K} \left(\frac{\arcsin \frac{\delta P_{i}}{1 + \delta P_{i}} \cdot \frac{2A}{N}\right)^{2} \cdot \frac{2}{N}}{K} & K = 5, N = 20\\ \frac{A^{2}/2}{\left(\frac{2A}{N}\right)^{2} + \sum_{i=1}^{i=K} \left(\frac{\arcsin \frac{\delta P_{i}}{1 + \delta P_{i}} \cdot \frac{2A}{N}\right)^{2} \cdot \frac{2}{N}}{K} & K = 9, N = 18 \end{cases}$$
(13)

where *i* = 1 . . . *K*. Since the δP_i of each channel is different, when calculating the effect of δP_i on OADC performance, it can be represented by

$$IM = \sqrt{\frac{\sum_{i=1}^{K} (\delta P_i - 1)^2}{K}}$$
(14)

It can be seen from Equation (13) that SINAD is related to the number of channels of MMI^{2nd}. As shown in Figure 6a, SINAD drops faster with more channels, because there is a greater probability of errors in the judgement. Different IM values are set in the simulation to observe the impact on ENOB of the OADC. In simulation, ENOB was calculated by 50 times for the same IM values. The red curve in Figure 6b shows ENOB degradation induced by IM, the results for previous 9-port scheme are shown as a black curve. We can see that both ENOB degrades with IM increasing, this is because due to the imbalance, the actual quantization step size is different from the ideal quantization step size, which would lead to non-uniform quantization errors and make harmonic noise power increase, resulting in a decrease in ENOB. Furthermore, as shown in Figure 6b, it has been verified by 50-time simulations that if the ENOB degrades by 1 bit, the tolerance of IM of the proposed scheme can be 16%, but the previous 9-port scheme has only 10.9% tolerance. In comparison, the proposed scheme is more robust to the power imbalance of the quantizer. We can also see that under the same IM, because the proposed scheme has fewer ports, the probability of error in the output digital code is smaller than that of the previous 9-port scheme.



Figure 6. The effect of channel imbalance on system performance. (**a**) Theoretical calculation of the effect of channel imbalance on SINAD. (**b**) Simulation results at the condition of MMI with channel imbalance.

3.3. Electronic Devices Noise

The noise introduced by the electrical devices in the OADC also affects the performance of the OADC. Here we analyze two typical effects on the ENOB of the OADC. One is the noise of the input analog RF signal, the other is the phase noise of the PLL used to synchronize the sampling pulses with comparators and coding circuits, etc.

3.3.1. The Noise of Input Signal

The signal source and RF amplifier may introduce noise. Therefore, we analyzed the noisy signal on the performance of OADC. The signal to noise ratio (SNR) of the analogue signal is expressed as SNR_{in} . Assuming that the noise added to the analogue signal is a Gaussian random signal with a mean value of 0. Therefore, the SINAD under the error caused by noise is given by

$$SINAD = \begin{cases} \frac{A^2/2}{\left(\frac{2A}{N}\right)^2 + 2(K+2) \cdot P_{noise} \cdot \frac{2}{N}} & K = 5, N = 20\\ \frac{A^2/2}{\left(\frac{2A}{N}\right)^2 + K \cdot P_{noise} \cdot \frac{2}{N}} & K = 9, N = 18 \end{cases}$$
(15)

where P_{noise} is the power of the noisy signal. It can be seen from Equation (15) that SINAD is related to the quantization level *N*. We carried out the simulation operation with other parameters unchanged. The results of ENOB vs. P_{noise} are shown in Figure 7a. Dozens of simulations have been carried out to eliminate the contingency of the results, which indicate that the higher the number of quantization levels, the faster the ENOB decreases. That is to say that the noise of the input signal has a greater impact on OADC with bigger ENOB, thus the SNR of the input signal cannot be ignored.



Figure 7. The effect of noisy signal and phase noise of PLL on system performance. (**a**) Simulation results of ENOB under different SNR of input analog signal. (**b**) Simulation results of ENOB under different RMS(*J*_{per}) of PLL.

3.3.2. Phase Noise of PLL

The reference clock signal of the PLL is the synchronous output of the pulse laser, thus PLL could provide a locked clock to the electronic comparators and coding circuits. However, the clock signal generated from an actual PLL has phase noise ($\theta(t)$), which is equivalent to the jitter of the clock signal (J_{per}), that represents clock non-synchronization. The clock jitter J_{per} , which is a random disturbance signal and described by root mean square value (RMS) as

$$\operatorname{RMS}(J_{per})(seconds) = \frac{1}{2\pi f_c} \sqrt{\theta^2(t)} = \frac{1}{2\pi f_c} \sqrt{2\int_0^\infty S_\theta(f) df}$$
(16)

where f_c is clock frequency, $S_{\theta}(f)$ is the power spectrum of phase noise.

Different RMSs of clock jitter are added in the theoretical calculation and simulation to analyze the influence on OADC. According to P(t), Equation (7), we can calculate the SINAD caused by clock jitter J_{per} as following

$$SINAD = \begin{cases} \frac{A^{2}/2}{\left[\frac{2A}{N}\right]^{2} + \sum_{i=1}^{i=K+1} \frac{1}{T_{s}} \int_{0}^{T_{s}} \left[\left|V_{i}\left(t-J_{per}\right) \cdot P\left(t-J_{per}\right) - V_{i}(t) \cdot P(t)\right|\right]^{2} dt & K = 5, N = 20\\ \frac{A^{2}/2}{\left[\frac{2A}{N}\right]^{2} + \sum_{i=1}^{i=K} \frac{1}{T_{s}} \int_{0}^{T_{s}} \left[\left|V_{i}\left(t-J_{per}\right) \cdot P\left(t-J_{per}\right) - V_{i}(t) \cdot P(t)\right|\right]^{2} dt & K = 9, N = 18 \end{cases}$$

$$(17)$$

It can be seen from Equation (17) that SINAD drops faster when J_{per} increases, because there is a greater risk of error in judgment time. We changed RMS(J_{per}) from 0 to 1 ps, and maintained the other parameters. The results of ENOB vs. clock jitter are shown in Figure 7b. When ENOB degrades by 1 bit, RMS(J_{per}) tolerance is 226 fs for the proposed scheme, while it is 155 fs for our previous 9-port scheme. The results indicate that the new proposed OADC has lower requirements on phase noise of PLL due to fewer channels than previous 9-port scheme.

4. Conclusions

In this paper, a new OADC scheme with ENOB enhanced by introducing an MZM to increase the optical quantization levels has been proposed and demonstrated in simulation. Based on the operation principle, 20 quantization levels (corresponding to 4.32 of ENOB) are realized by using only 6 channels, which indicates that the scheme requires much fewer quantization channels or modulators to realize the same amount of ENOB. A numerical analysis and proof-of-concept demonstrations were carried out to verify the feasibility and robustness of the scheme. Simulation results show that 4.03 of ENOB is realized for 7.01 GHz RF signal under 50 GHz sampling rate, which indicates that the proposed scheme requires much fewer quantization output channels or modulators to realize the same amount ENOB, compared with our previous 9-port scheme. We analyzed the influence of RIN and timing jitter of sampling pulses and the channel imbalance of MMI^{2nd} on ENOB of both the proposed OADC scheme and the previous 9-port scheme. The simulation results show that the proposed scheme can tolerate up to 9.6% of RIN and up to 0.5 ps of timing jitter of sampling pulses, as well as 16% power imbalance of the MMI output channels when ENOB degrades by 1bit; in contrast, the previous 9-port scheme can tolerate 5.3% of RIN and 0.4 ps of timing jitter of sampling pulses, and 10.9% power imbalance of the MMI. Based on the operation principle, if the proposed scheme extends to a 5 bit operation, only 10 ports are needs to achieve 36 quantization levels (ideally 5.17 bit); in contrast, 17 ports are needed in our previous 9-port scheme to achieve 34 quantization levels (ideally 5.08 bit). When the ENOB continues to increase, the advantage of fewer ports requirement in the proposed scheme becomes even more significant. This advantage makes our scheme more compact and more robustness, and therefore easier for integration and more practical for system applications.

In future, to realize an OADC chip based on our proposed scheme, there exist two main challenges, one of which is heterogeneous integration of optical devices, the other challenge is optoelectronic integration. However, as we know, the above two challenges, optical heterogeneous integration and optoelectronic integration, have been some of the most interesting and promising research fields throughout the world for decades [30,31]. With the breakthrough of the two integration technologies, our OADC would be practically realized.

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