

Article

A Novel ON-State Resistance Modeling Technique for MOSFET Power Switches

Ionuț-Constantin Guran ^{*}, Adriana Florescu  and Lucian Andrei Perişoară

Department of Applied Electronics and Information Engineering, Faculty of Electronics, Telecommunications and Information Technology, University Politehnica of Bucharest, 060042 Bucharest, Romania

^{*} Correspondence: ionut.guran32@gmail.com

Abstract: Nowadays, electronic circuits' time to market is essential, with engineers trying to reduce it as much as possible. Due to this, simulation has become the main testing concept used in the electronics domain. In order to perform the simulation of a circuit, a behavioral model must be created. Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) are semiconductor devices found in a multitude of electronic circuits, and they are also used as power switches in many applications, such as low-dropout linear voltage regulators, switching regulators, gate drivers, battery management systems, etc. A MOSFETs' behavior is extremely complex to model, thus, creating high-performance models for these transistors is an imperative condition in order to emulate the exact real behavior of a circuit using them. An essential parameter of MOSFET power switches is the ON-state resistance ($R_{DS(ON)}$), because it determines the power losses during the ON state. Ideally, the power losses need to be zero. $R_{DS(ON)}$ depends on multiple factors, such as temperature, load current, and gate-to-source voltage. Previous studies in this domain focus on the modeling of the MOSFET only in specific operating points, but do not cover the entire variation range of the parameters, which is critical for some applications. For this reason, in this paper, there was introduced for the first time a novel ON-state resistance modeling technique for MOSFET Power Switches, which solves the entire $R_{DS(ON)}$ dependency on the transistor's variables stated above. The novel $R_{DS(ON)}$ modeling technique is based on modulating the transistor's gate-to-source voltage such that the exact $R_{DS(ON)}$ value is obtained in each possible operating point. The method was tested as a real-life example by creating a behavioral model for an N-channel MOSFET transistor and the chosen simulation environment was Oregon, USA, Computer-Aided Design (OrCAD) capture. The results show that the model is able to match the transistor's $R_{DS(ON)}$ characteristics with a maximum error of 0.8%. This is extremely important for applications in which the temperatures, voltages, and currents vary over a wide range. The new proposed modeling method covers a gap in the behavioral modeling domain, due to the fact that, until now, it was not possible to model the $R_{DS(ON)}$ characteristics in all operating corners.

Keywords: metal-oxide-semiconductor field-effect transistor power switch; ON-state resistance behavioral model; OrCAD capture simulation environment; PSpice Allegro simulator

MSC: 94-10



Citation: Guran, I.-C.; Florescu, A.; Perişoară, L.A. A Novel ON-State Resistance Modeling Technique for MOSFET Power Switches.

Mathematics **2023**, *11*, 72. <https://doi.org/10.3390/math11010072>

Academic Editor: Ioannis K. Argyros

Received: 24 November 2022

Revised: 13 December 2022

Accepted: 21 December 2022

Published: 25 December 2022



Copyright: © 2022 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (<https://creativecommons.org/licenses/by/4.0/>).

1. Introduction

Power electronics is a domain in which the power switches play a key role and employs the use of a multitude of silicon devices, such as diodes, thyristors, bipolar junction transistors (BJT), and unipolar transistors: junction-gate field-effect transistor (JFET) and MOSFET transistor [1,2]. BJTs are easy to manufacture and imply low costs, but the driver circuits are more complicated and lead to increased costs in the end [2]. Due to their reduced-complexity gate driving circuits, high switching speed, high input impedance, and good thermal stability, MOSFET transistors have become, today, one of the main semiconductor devices used as power switches in power electronic circuits [3].

The power levels required by the applications used in power electronics are spread over a large spectrum, as shown in Figure 1. The first category is represented by the applications that use low current levels (around 1A), such as display drives. The second category includes devices that use a small supply voltage (less than 100 V). Automotive electronics and power supplies used in computers represent some examples within this category. The most suitable power device here is the silicon power MOSFET due to its fast switching time and low ON-state resistance. The third category is represented by power devices that use high operating voltages (more than 200 V). Consumer appliances, electric vehicle drives, and lamp ballasts are some typical examples for this category [4]. Considering the previous information, it is generally accepted that any switch that can pass a minimum current of 1 A is a power switch [5].

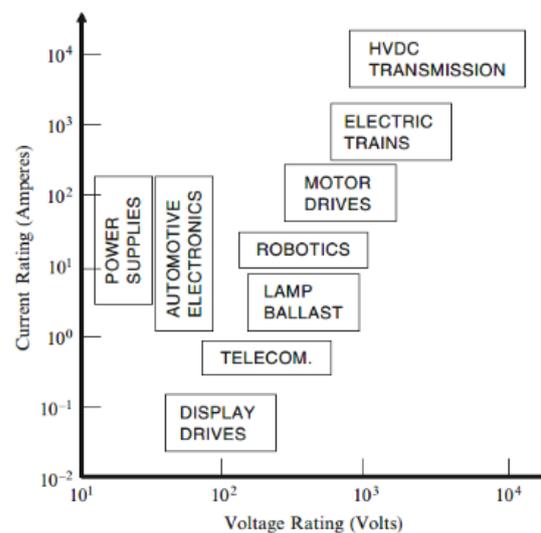


Figure 1. Power device categories [4].

Simulation has become the main testing concept used in the electronics domain because it reduces the testing costs, duration, and can reveal faults and flaws in the design process or validate the correct functioning of the system. A behavioral model is a software file written in a specific simulation language, which emulates the real behavior of a circuit. However, accurate behavioral models are needed for the circuits to be tested, such that the simulated behavior corresponds to the real behavior. One of the most important electronic circuits simulators is PSpice, which can be used for the simulation of a wide range of analog and digital applications. PSpice includes analog and digital libraries of standard components and also emulates multimeters, oscilloscopes, signal generators, and frequency spectrum analyzers [6,7].

In MOSFET power switches, the drain-source ON-state resistance ($R_{DS(ON)}$) is a key parameter, which greatly varies with the junction temperature T_j and with the gate-to-source voltage V_{GS} [8]. Stefanskyi et al. [9] made a comparison between four power MOSFET Simulation Program with Integrated Circuit and Phases (SPICE) models provided by main transistor manufacturers and they reveal that each model is created by using Analog Behavioral Modeling (ABM) sources that create complex structures, but none of the models can be easily customized by external users. Moreover, the results show that the model characteristics do not accurately match the datasheet ones. However, the models were only tested at a junction temperature T_j of 25 °C and only the drain current vs. drain-source voltage characteristics are provided and, hence, no $R_{DS(ON)}$ variation analysis was performed. Pratap et al. [1] proposed a simplified SPICE model for a power MOSFET. Their approach is the reuse of the available built-in MOSFET SPICE model, to which they add a series voltage source on the transistor gate and a parallel current source to the transistor drain-source channel for temperature compensation. Only the drain current vs. drain-source voltage characteristics are simulated and compared to the datasheet

characteristics. The results show a very close match. However, only a temperature of 25 °C is used so that the $R_{DS_{ON}}$ variation cannot be interpreted. He et al. [10] introduced an approach to the generation of corner and statistical models limited to Silicon Carbide (SiC) MOSFETs. The method is able to produce good results, but the temperature effects are not taken into account. In addition, it was tested only for a finite set of $R_{DS_{ON}}$ values. Hsu et al. [11] presented a simple SPICE modeling method for SiC MOSFETs, which is based on mathematical equations and also uses a diode along with a JFET transistor. The method accounts for the $R_{DS_{ON}}$ variation with the gate voltage and obtains good fitting results compared to the conventional manufactures' approach. Further, the $R_{DS_{ON}}$ variation with the junction temperature is studied but only in a finite number of points without giving clear results on the fitting error. Borghese et al. [12] described a compact electrothermal SPICE model for a SiC MOSFET that can be also used for other MOSFET types. The method uses only a small set of parameters to fit the MOSFET performance. The simulated drain current vs. drain-source voltage and drain current vs. gate-source voltage are compared with the datasheet characteristics and the results show a very good match. This analysis is conducted only for two junction temperatures, 25 °C and 125 °C; hence, the $R_{DS_{ON}}$ variation over temperature cannot be determined. For this reason, the paper puts forward a novel method of modeling the ON-state resistance of MOSFET power switches that studies and covers the entire $R_{DS_{ON}}$ variation range given in the datasheet.

The main contributions of this paper are listed below:

- Simulation of the existing model of CSD13380F3 N-channel MOSFET transistor from Texas Instruments and plotting its $R_{DS_{ON}}$ characteristics;
- Implementation of a new model for CSD13380F3 N-channel MOSFET transistor using the novel method, which focuses on the $R_{DS_{ON}}$ characteristics, as listed in the datasheet;
- Implementation of an external temperature pin that allows one to emulate the self-heating effect of the transistor;
- Simulation of the new CSD13380F3 model using OrCAD Capture environment and PSpice Allegro simulator;
- Comparison between the existing model and the new model from the achieved performance point of view;
- The simulation results based on the novel $R_{DS_{ON}}$ modeling technique show that it is possible to model the transistor $R_{DS_{ON}}$ in all operating corners accurately;
- Using this novel method, the switching behavior of the MOSFET power switch model is able to match the real-life characteristics of the component over the entire operating range, not only in discrete operating points;
- Highly reliable MOSFET power switch models can be built using the new $R_{DS_{ON}}$ modeling technique in a fast and efficient manner, only by defining the theoretical $R_{DS_{ON}}$ characteristics and without having to set other parameters.

The remainder of this paper is organized as follows: Section 2 reveals the background related to MOSFET $R_{DS_{ON}}$, Section 3 presents the existing CSD13380F3 transistor model designed by Texas Instruments and the simulation of its $R_{DS_{ON}}$ characteristics, Section 4 shows materials and methods for the new transistor model implementation, Section 5 presents the simulation results for the new model, Section 6 comprises a comparison between the existing model from Texas Instruments and the new proposed model, and finally, the conclusions are presented in Section 7.

2. Background of the MOSFET Used as Power Switch

The selection of the most appropriate device for a certain application is a difficult task for an engineer, since it requires knowledge about the characteristics of the device and its unique features. Compared to low-power devices, power devices present a more complex structure and Operational current vs. Voltage characteristics. Moreover, the transistor driver design sees an increase in complexity [13].

The MOSFET transistor symbols are shown in Figure 2. Each MOSFET has a gate (G), drain (D), and source (S) terminals. There is also a fourth terminal, but it is usually connected internally to the source in power MOSFETs, so that is why it is omitted in some symbols. There are two main MOSFET transistor types: N-channel, where the drain current i_D flows from D to S, and P-channel, where i_D flows from S to D. For each channel, there are two other transistor types: depletion and enhancement MOSFETs, depending on the barrier layer used [14–16].

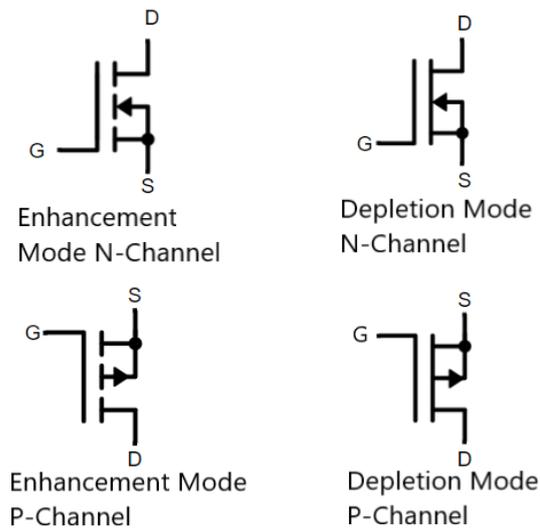


Figure 2. MOSFET transistor symbols [16].

Figure 3 presents the ideal MOSFET power switch drain current vs. drain-source voltage family of characteristics $i_{DS}(v_{DS})$ at increasing gate voltages v_{GS} as a parameter. The ideal MOSFET power switch is able to conduct current in the ON state with a zero-voltage drop and has no leakage current during the OFF state when it blocks the voltage. In the active region, the ideal MOSFET power switch can operate at high current (i_{DS}) and voltage (v_{DS}). The characteristics are uniformly spaced in the active region, indicating that the gain is independent of the i_{DS} and v_{DS} [4,13].

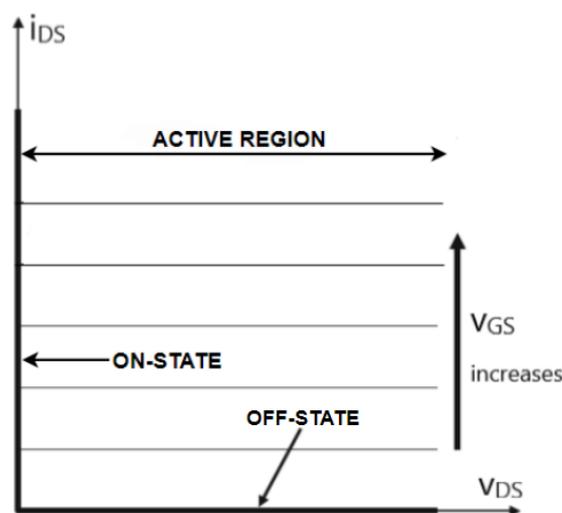


Figure 3. Ideal MOSFET power switch characteristics [4,13].

The $i_D(v_{DS})$ family of characteristics of a real MOSFET power switch is shown in Figure 4. The real power switch is characterized by a finite ON-state resistance $R_{DS(ON)}$ in the linear region, as well as a finite leakage current in the OFF state (cutoff region). The

$i_D(v_{DS})$ characteristics are not uniformly spaced in the active region due to the square law dependency on the gate voltage v_{GS} . The i_D dependency on the v_{DS} voltage in the active region (also known as channel length modulation) is not shown here [4,5,13].

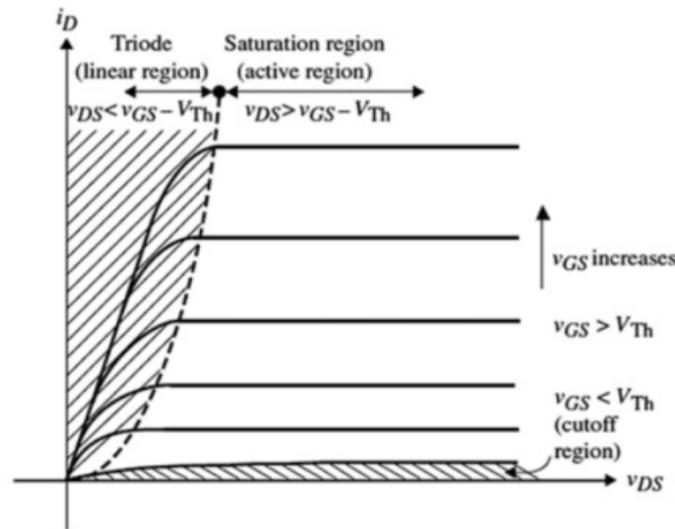


Figure 4. Real MOSFET power switch characteristics [13].

One of the key parameters of a MOSFET power switch is the drain-source ON-state resistance ($R_{DS_{ON}}$). When the power MOSFET is in the linear region, the device behaves like a constant resistance, which is linearly proportional to the change between the drain-source voltage v_{DS} and the drain current i_D , at a constant gate-source voltage V_{GS} and at a constant junction temperature T_J [2,8,13]:

$$R_{DS_{ON}} = \left. \frac{\partial v_{DS}}{\partial i_D} \right|_{V_{GS}, T_J = \text{constant}} \tag{1}$$

The $R_{DS_{ON}}$ value has a great significance and can vary between tens of milliohms for low-voltage MOSFETs and a few ohms for high-voltage MOSFETs. The importance of $R_{DS_{ON}}$ lies in determining the forward voltage drop across the transistors and the power losses during the ON state ($P_{ON,LOSS}$). For a constant drain current I_D , the power losses are computed as shown [2,8,17]:

$$P_{ON,LOSS} = I_D^2 \cdot R_{DS_{ON}} \tag{2}$$

N-channel, enhancement type is the most used MOSFET switch in the power electronics domain. The drain current i_D starts flowing when a channel between the drain and the source is established. The channel creation occurs when the gate-source voltage exceeds the transistor threshold voltage V_T . The power MOSFET operates in the cutoff region when the gate-source voltage is lower than the threshold voltage, $v_{GS} < V_T$; hence, no channel is induced and only a leakage current i_{LEAK} flows. For $v_{GS} > V_T$, the MOSFET can operate either in the linear region (triode region) or in the saturation region, depending on the value of the drain-source voltage v_{DS} . For the linear region of operation, the conditions are: $v_{DS} < v_{GS} - V_T$ and $v_{GS} > V_T$. For the saturation region, the following conditions apply: $v_{DS} > v_{GS} - V_T$ and $v_{GS} > V_T$. In the linear region, the channel is continuous, having no pinch-off and this results in the drain current i_D being proportional to the channel resistance. In the saturation, the channel pinches off and a constant-drain current I_D results. When v_{GS} exceeds V_T , it is the v_{DS} that decides whether the channel pinches off or not [4,8,13].

3. Simulation Results for the CSD13380F3 MOSFET Model Designed by Texas Instruments

There are already MOSFET models on the market from companies, such as Infineon, NXP Semiconductors, Analog Devices, and Texas Instruments, but only few of them have simulation models (the vast majority are from Texas Instruments), and their behavior is not entirely emulating the real characteristics and their variation [18–20].

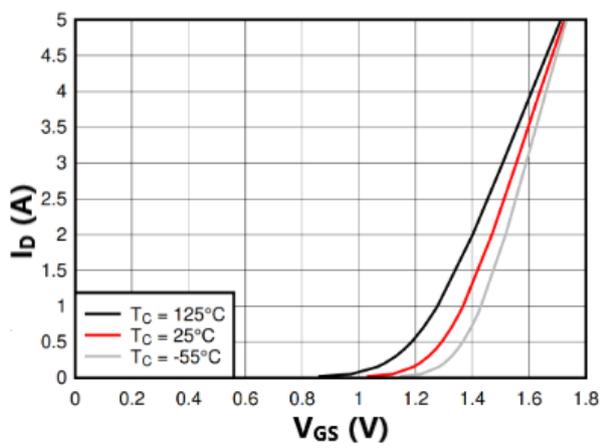
CSD13380F3 from Texas Instruments is a 12 V N-channel MOSFET, which can be used for load-switch applications, general-purpose switching applications, as well as battery, handheld, and mobile applications. It has a low ON-state resistance, a high operating drain current, and an ultra-small footprint (0.73 mm × 0.64 mm) with a low profile (0.36 mm maximum height). The transistor absolute maximum ratings at 25 °C are:

- Maximum drain-source voltage $V_{DS,max}$: 12 V
- Maximum gate-source voltage $V_{GS,max}$: 8 V
- Maximum continuous-drain current $I_{D,max}$: 3.6 A
- Maximum pulsed-drain current: $I_{DM,max}$: 13.5 A (pulse duration lower than 100 μ s and duty cycle lower than 1%)
- Operating junction temperature T_j : -55 °C to 150 °C [21].

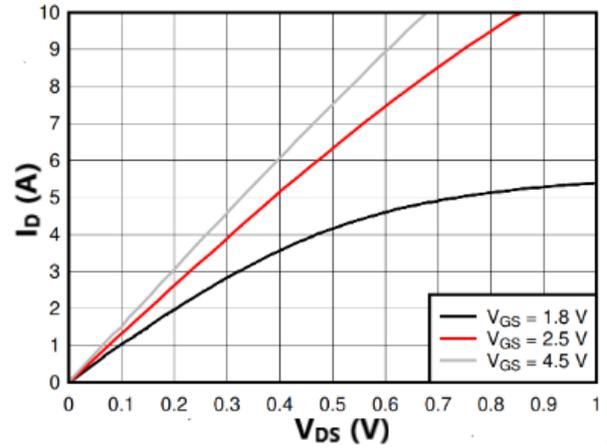
Figure 5 shows some important characteristics of the CSD13380F3 MOSFET, such as:

- Drain Current vs. Gate-Source voltage at three distinct temperatures (-55 °C, 25 °C, 125 °C), where the drain current increases quadratically with V_{GS} after the threshold voltage. This happens due to the drain current i_D quadratic dependency on the gate-source voltage v_{GS} when operating in saturation and is detailed in Section 4.
- Drain Current vs. Drain-Source Voltage at three different V_{GS} voltages (1.8 V, 2.5 V, 4.5 V), where the drain current increases linearly with the drain-source voltage until it saturates. This happens due to the resistor-like behavior of the MOSFET in the linear region. In the saturation region, the drain-source voltage v_{DS} has minimal influence on the drain current i_D . More details can be found in Section 4.
- Threshold Voltage vs. Case Temperature, where the threshold voltage decreases linearly with the increase in temperature, due to the direct dependency of the threshold voltage V_T on the thermal voltage $k \cdot T/q$, where k is the Boltzmann constant (1.380649×10^{-23} m² kg s⁻² K⁻¹) and q is the charge of an electron ($1.60217663 \times 10^{-19}$ C).
- Maximum safe operating area, which shows that starting with a certain V_{DS} , the maximum drain current decreases. This happens due to the maximum power capabilities of the MOSFET, where the current decreases to limit the power dissipation.
- Maximum Drain current vs. Temperature curve, which shows that the temperature negatively affects the maximum current. This happens due to the maximum power dissipation allowed on the MOSFET, beyond which the transistor would be destroyed. This characteristic is obtained by experimental results in the laboratory.

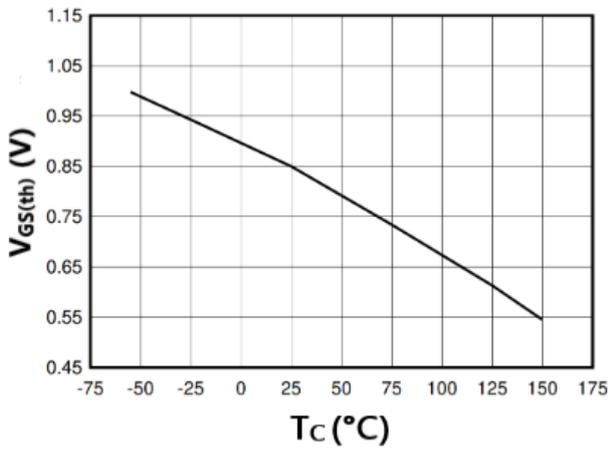
The ON-state resistance $R_{DS,ON}$ vs. Gate-Source voltage V_{GS} characteristic of the CSD13380F3 transistor is presented in Figure 6. The characteristic was determined for a drain current $I_D = 0.4$ A. It can be noticed that at low V_{GS} voltage, $R_{DS,ON}$ has a higher value (200 m Ω) and decreases based on a square-root dependency until it reaches lower values (79 m Ω at 25 °C and 60 m Ω at 125 °C) at high V_{GS} values (>8 V). $R_{DS,ON}$ decreases with the V_{GS} increase because the drain current increases, but it saturates at high V_{GS} voltages due to approaching the saturation region conditions. This dependency is mathematically explained in more detail by relations (3)–(7) in Section 4.



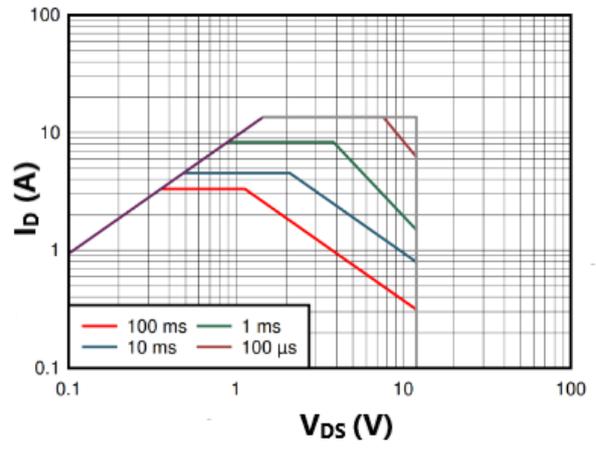
(a) Drain Current vs. Gate-Source Voltage



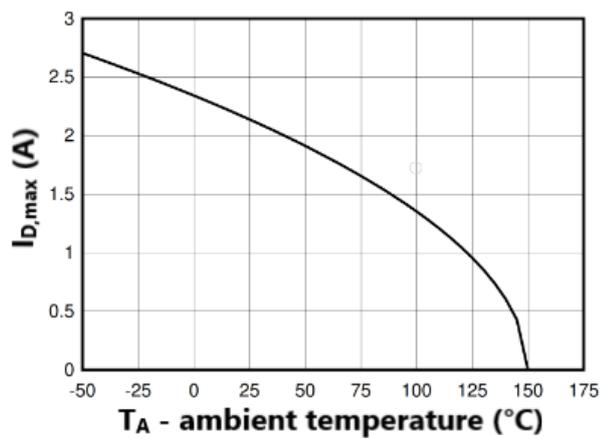
(b) Drain Current vs. Drain-Source Voltage



(c) Threshold Voltage vs. Case Temperature



(d) Maximum safe operating area



(e) Maximum Drain current vs. Temperature

Figure 5. CSD13380F3 MOSFET characteristics [21].

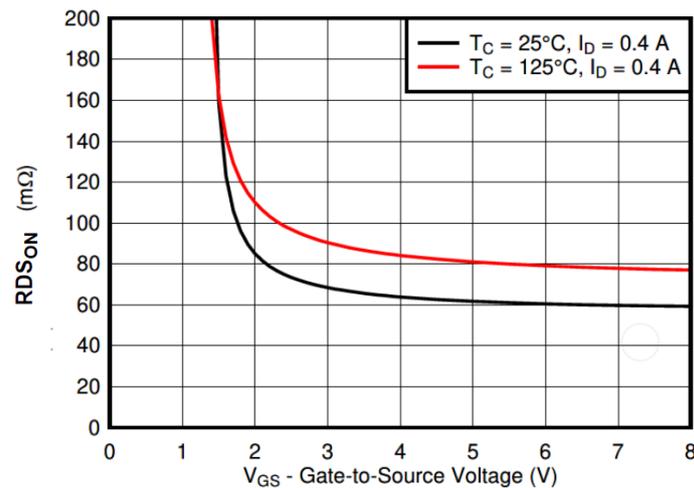


Figure 6. $R_{DS_{ON}}$ vs. V_{GS} characteristic of CSD13380F3 [21].

The normalized ON-state resistance $R_{DS_{ON}}$ vs. Case Temperature characteristic is shown in Figure 7, for two V_{GS} voltages (1.8 V and 4.5 V) and a drain current I_D of 0.4 A. In this case, the values are normalized to a temperature of 25 °C (value at a temperature of 25 °C is 1). It can be observed that the MOSFET $R_{DS_{ON}}$ increases with the case temperature. The dependency is determined experimentally based on laboratory measurements. The $R_{DS_{ON}}$ variation with the temperature is important because the load switches can be used in all types of environments (from cold to hot, as recommended in the manufacturer’s datasheet presented in Figure 7) and they also heat up to high temperatures during functioning at high switching currents.

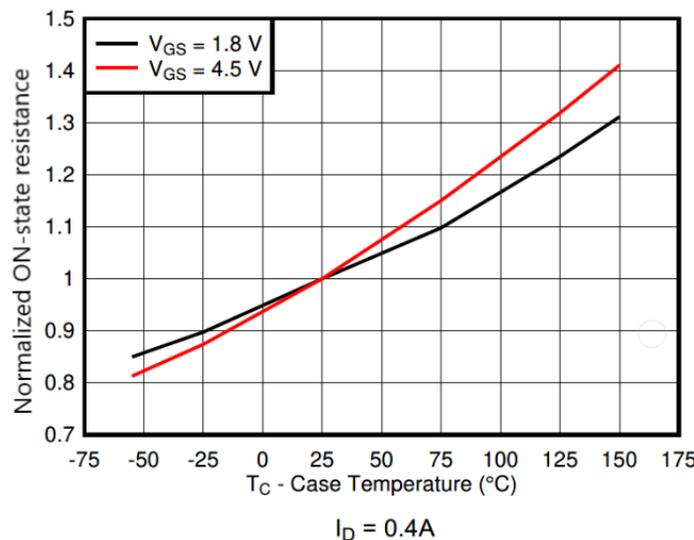


Figure 7. Normalized ON-state resistance vs. Case temperature [21].

The starting point in building the new CSD13380F3 MOSFET model using the novel ON-state resistance modeling technique was the simulation of the transistor model provided by Texas Instruments. The model can be downloaded from Texas Instruments’ website [22] and it contains the CSD13380F3 symbol for Orcad Capture (with the extension .olb) and the library file for PSpice Allegro simulator (having the extension .lib). Based on these two files, the simulation test-bench was built and it is used to determine the initial $R_{DS_{ON}}$ characteristics presented previously in Figures 6 and 7. The simulation test-bench is displayed in Figure 8, which consists of the piecewise linear voltage source V_{GS} , which

sets the gate-source voltage of the MOSFET, the CSD13380F3 MOSFET symbol, and the piecewise linear current source I_D that sets the drain current of the transistor.

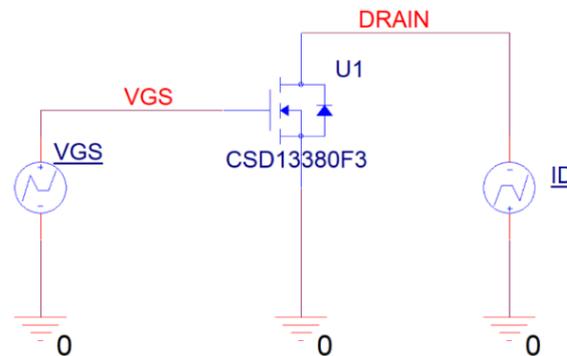


Figure 8. Simulation test-bench for CSD13380F3.

In the first setup, the gate-source voltage V_{GS} is varied between 1.5 V and 8 V, while the drain current I_D is set at 0.4 A. Two simulations are performed corresponding to two junction temperatures T_J (25 °C and 125 °C). The results are presented in Figure 9. It can be seen that the drain-source V_{DS} is influenced by the junction temperature T_J .

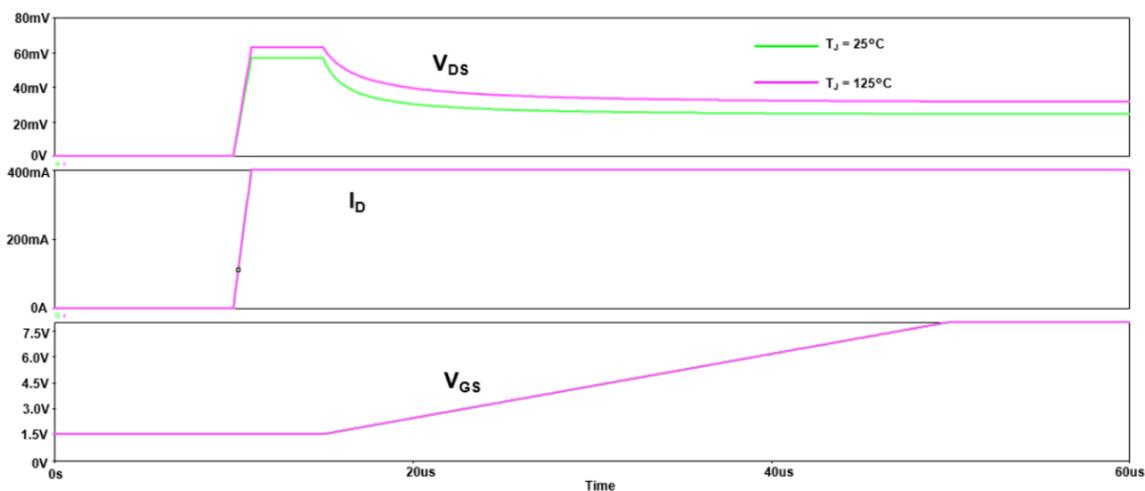


Figure 9. Simulation setup for determining the Texas Instruments CSD13380F3 model $R_{DS(ON)}$ vs. V_{GS} characteristics.

The results presented in Figure 9 can be numerically found in Table 1. At a case temperature of 25 °C, the $R_{DS(ON)}$ varies between 141.75 mΩ and 60.92 mΩ, while at 125 °C, $R_{DS(ON)}$ varies between 157.65 mΩ and 78.98 mΩ.

Figure 10 presents the simulated $R_{DS(ON)}$ vs. V_{GS} characteristics for Texas Instruments’ CSD13380F3 model, based on the results obtained in Table 1. It can be noted that at V_{GS} voltages above 2 V, the characteristic is very similar to the theoretical one presented in Figure 6, but at voltages below 2 V, the simulated characteristic does not match the theoretical one. The simulated $R_{DS(ON)}$ for a V_{GS} of 1.5 V is 141.75 mΩ at 25 °C and 157.65 mΩ at 125 °C. The theoretical characteristic is 200 mΩ at $V_{GS} = 1.5$ V for both temperatures, hence, the relative errors are 29.12% at 25 °C and, respectively, 21.17% at 125 °C, so the simulated $R_{DS(ON)}$ vs. V_{GS} characteristics is not accurate at low V_{GS} voltages. The simulation results show that Texas Instruments’ model exhibits large errors for low V_{GS} values.

Table 1. $R_{DS(ON)}$ vs. V_{GS} calculations for Texas Instruments’ model.

$T_{CASE} = 25\text{ }^{\circ}\text{C}$			
I_D	V_{GS}	V_{DS}	$R_{DS(ON)}$
[A]	[V]	[mV]	[m Ω]
0.4	1.5	56.7	141.75
0.4	2	34.25	85.62
0.4	2.5	29.72	74.3
0.4	3	27.75	69.39
0.4	3.5	26.67	66.68
0.4	4	26	64.98
0.4	4.5	25.53	63.82
0.4	5	25.2	63
0.4	5.5	24.95	62.39
0.4	6	24.77	61.93
0.4	6.5	24.63	61.58
0.4	7	24.52	61.3
0.4	7.5	24.43	61.09
0.4	8	24.37	60.92
$T_{CASE} = 125\text{ }^{\circ}\text{C}$			
0.4	1.5	63.06	157.65
0.4	2	44.11	110.29
0.4	2.5	38.88	97.2
0.4	3	36.38	90.96
0.4	3.5	34.93	87.33
0.4	4	34	84.97
0.4	4.5	33.33	83.34
0.4	5	32.86	82.15
0.4	5.5	32.5	81.26
0.4	6	32.22	80.57
0.4	6.5	32	80.03
0.4	7	31.84	79.6
0.4	7.5	31.7	79.26
0.4	8	31.59	78.98

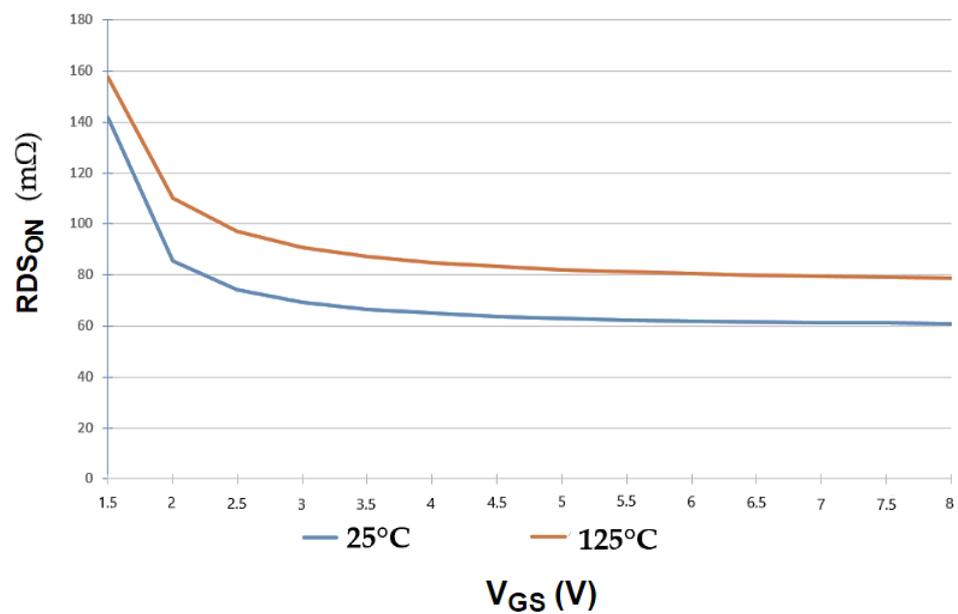


Figure 10. Simulated $R_{DS(ON)}$ vs. V_{GS} for Texas Instruments’ CSD13380F3 model.

In order to obtain the normalized $R_{DS(ON)}$ vs. Temperature characteristic presented in Figure 7, the same simulation test-bench as shown in Figure 8 is used. The drain current source I_D is set to 0.4 A, as in the previous case. The simulator temperature is swept between $-50\text{ }^\circ\text{C}$ and $150\text{ }^\circ\text{C}$ with a step of $25\text{ }^\circ\text{C}$, while the voltage source V_{GS} varies between 1.8 V and 4.5 V. In order to normalize the characteristic, the initial resulting curves are divided into the $25\text{ }^\circ\text{C}$ values for each V_{GS} voltage. Figure 11 presents the second simulation setup used for determining the normalized $R_{DS(ON)}$ vs. Case temperature T_C characteristics. Only three temperatures were chosen to be shown in these waveforms ($-50\text{ }^\circ\text{C}$, $25\text{ }^\circ\text{C}$, $150\text{ }^\circ\text{C}$) such that the figure is more visible. The downside of the Texas Instrument implementation is that the temperature can only be set as a simulator parameter and cannot be adjusted dynamically during the simulation; hence, the self-heating effect cannot be seen.

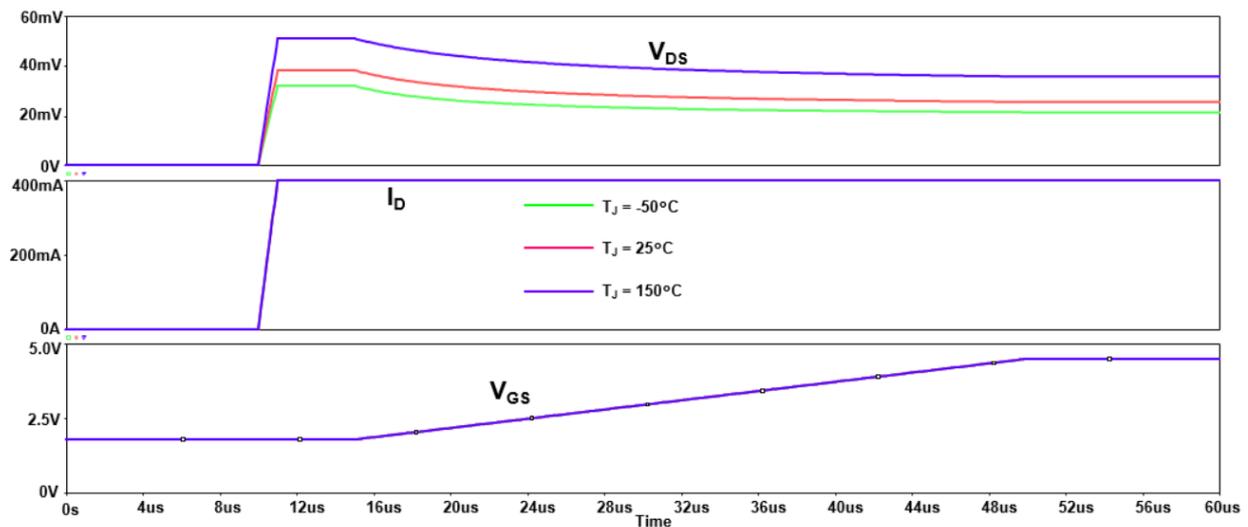


Figure 11. Simulation setup for determining the Texas Instruments CSD13380F3 model normalized $R_{DS(ON)}$ vs. T_C characteristics.

The waveforms in Figure 11 are transposed in Table 2, which presents the simulation results along with the calculated $R_{DS(ON)}$ and normalized $R_{DS(ON)}$ for both V_{GS} voltages (1.8 V and 4.5 V) for temperatures between $-50\text{ }^\circ\text{C}$ and $150\text{ }^\circ\text{C}$. It can be noted that for $V_{GS} = 1.8\text{ V}$, the normalized $R_{DS(ON)}$ varies between 0.83 and 1.34, while for $V_{GS} = 4.5\text{ V}$, the normalized $R_{DS(ON)}$ takes values between 0.83 and 1.4. The temperature step is chosen at $25\text{ }^\circ\text{C}$.

Figure 12 presents the normalized $R_{DS(ON)}$ vs. Case Temperature characteristics for Texas Instruments' CSD13380F3 MOSFET model, drawn based on results shown in Table 2. It can be seen that until $50\text{ }^\circ\text{C}$, the two curves for $V_{GS} = 1.8\text{ V}$ and $V_{GS} = 4.5\text{ V}$ are identical and only separate at temperatures above $50\text{ }^\circ\text{C}$. Looking at the theoretical characteristic presented in Figure 7, the two curves are different in each temperature point, except at $25\text{ }^\circ\text{C}$ (due to normalization of the results to the $25\text{ }^\circ\text{C}$ temperature). The relative errors for the temperature of $-50\text{ }^\circ\text{C}$ are 2.4% at 1.8 V and 2.3% at 4.5 V, while for the temperature of $150\text{ }^\circ\text{C}$, the relative errors are 2.29% at 1.8 V and 0.7% at 4.5 V.

Table 2. $R_{DS(ON)}$ vs. Temperature simulation results for Texas Instruments’ model.

$V_{GS} = 1.8\text{ V}$				
I_D	T_{CASE}	V_{DS}	$R_{DS(ON)}$	Normalized $R_{DS(ON)}$
[A]	[°C]	[mV]	[mΩ]	
0.4	−50	31.81	79.53	0.83
0.4	−25	33.79	84.49	0.88
0.4	0	35.89	89.74	0.94
0.4	25	38.11	95.29	1
0.4	50	40.46	101.16	1.06
0.4	75	42.94	107.36	1.12
0.4	100	45.55	113.88	1.19
0.4	125	48.29	120.73	1.26
0.4	150	51.16	127.91	1.34
$V_{GS} = 4.5\text{ V}$				
0.4	−50	21.19	52.97	0.83
0.4	−25	22.42	56.06	0.88
0.4	0	23.82	59.56	0.94
0.4	25	25.39	63.49	1
0.4	50	27.13	67.83	1.06
0.4	75	29.03	72.59	1.14
0.4	100	31.1	77.76	1.22
0.4	125	33.33	83.34	1.31
0.4	150	35.73	89.33	1.4

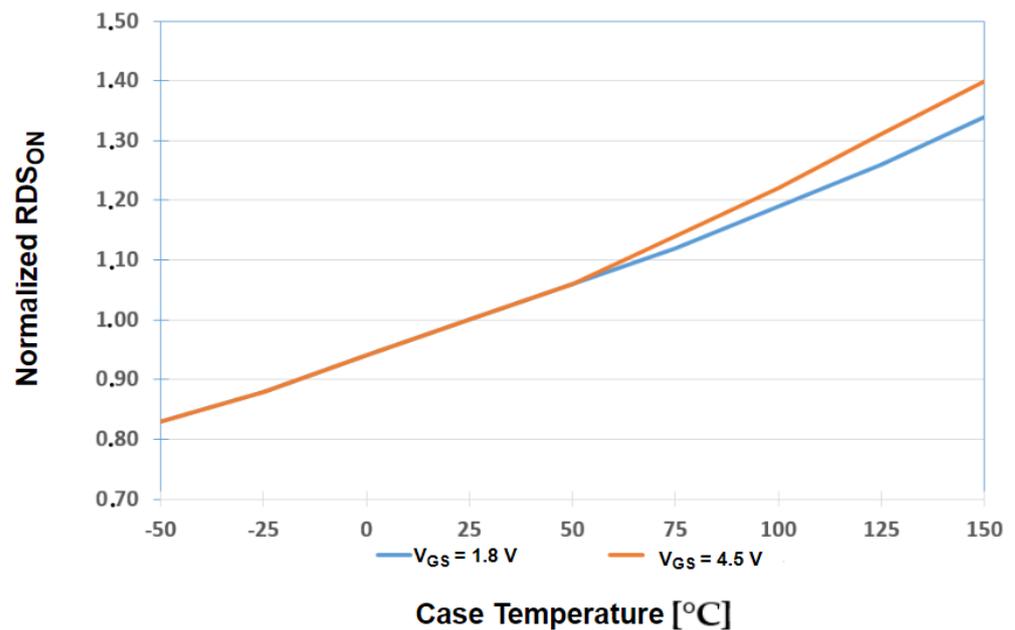


Figure 12. Simulated $R_{DS(ON)}$ vs. Case Temperature for Texas Instruments’ CSD13380F3 model.

4. Materials and Methods for the New CSD13380F3 MOSFET Model

As materials, the starting point was the MOSFET functioning equation set. If the gate-source voltage V_{GS} is higher than the threshold voltage V_T , the MOSFET can operate either in the linear region or in the saturation region.

The condition needed for the operation in the linear region is $V_{DS} < V_{GS} - V_T$, and the drain current I_D can be expressed as [23,24]:

$$I_D = k_n \cdot \frac{W}{L} \cdot \left(V_{GS} - V_T - \frac{V_{DS}}{2} \right) \cdot V_{DS}, \tag{3}$$

where k_n is transconductance coefficient (A/V^2), W is the MOSFET width, L is the MOSFET length, and V_{DS} is the drain-source voltage [7].

For the operation in the saturation region, the condition is $V_{DS} \geq V_{GS} - V_T$, and the drain current I_D becomes independent of the V_{DS} voltage if the channel length modulation effect is neglected [23,24]:

$$I_D = \frac{k_n}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_T)^2 \tag{4}$$

The novel ON-state resistance modeling principle is shown in Figure 13. The first step in the implementation of the above equations into the new model consists of setting the target ON-state resistance $R_{DS_{ON,t}}$ chosen by the user based on the catalogue data, which can be a function of temperature, V_{GS} , and load current, depending on the information that the user has. Next step is the calculation of the theoretical drain gate-source voltage $V_{GS,t}$ based on the specified $R_{DS_{ON,t}}$ and the monitored drain current I_D . When $V_{GS,t}$ is applied as the gate-source voltage, the transistor ON-state resistance automatically sets at $R_{DS_{ON,t}}$.

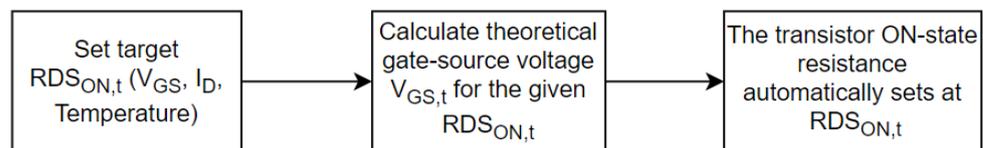


Figure 13. Novel ON-state resistance modeling principle.

Based on (1), the transistor’s V_{DS} for the transistor operating at $R_{DS_{ON,t}}$ becomes:

$$V_{DS} = R_{DS_{ON,t}} \cdot I_D \tag{5}$$

By replacing (5) in (3), the drain current I_D becomes:

$$I_D = k_n \cdot \frac{W}{L} \cdot \left[(V_{GS} - V_T) \cdot R_{DS_{ON,t}} \cdot I_D - \frac{R_{DS_{ON,t}}^2 \cdot I_D^2}{2} \right] \tag{6}$$

The theoretical gate-source voltage $V_{GS,t}$, which assures that the transistor ON-state resistance is $R_{DS_{ON,t}}$ is calculated based on (6) as follows:

$$V_{GS,t} = 1V + \frac{2 + k_n \cdot \frac{W}{L} \cdot I_D \cdot R_{DS_{ON,t}}^2}{2 \cdot k_n \cdot \frac{W}{L} \cdot R_{DS_{ON,t}}} \tag{7}$$

The transistor model senses the V_{GS} voltage that is set externally and based on its value, along with the temperature and drain current I_D , chooses the appropriate theoretical $R_{DS_{ON,t}}$ value. Based on the drain current I_D and the $R_{DS_{ON,t}}$ value, the actual V_{GS} controlling the transistor is set to $V_{GS,t}$.

The PSpice CSD13380F3 model source code is presented in Figure 14. The voltage sources EA1, EA2, and EA3 are used to define the normalizing factor. Based on the normalizing factor, the target $R_{DS_{ON,t}}$ is set. The drain current I_D is monitored through 0 V voltage source VSENSE. The $R_{DS_{ON,t}}$ and monitored I_D are then used to define the target gate-source voltage $V_{GS,t}$. A generic NMOS transistor is also used. Its parameters are not important, since the gate-source voltage automatically adapts in order to set the correct $R_{DS_{ON}}$ value.

```

.SUBCKT CSD13380F3 D G S TJ
EA1 NORM_1V8 0 VALUE={TABLE(V(TJ), -50, 0.85, -25, 0.9, 0, 0.95, 25, 1, 50, 1.05, 75, 1.1, 100, 1.175, 125, 1.23, 150, 1.31)}
EA2 NORM_4V5 0 VALUE={TABLE(V(TJ), -50, 0.82, -25, 0.88, 0, 0.94, 25, 1, 50, 1.08, 75, 1.15, 100, 1.24, 125, 1.32, 150, 1.41)}
EA3 NORM 0 VALUE={TABLE(V(G, S), 1.8, V(NORM_1V8), 4.5, V(NORM_4V5))}
ERDSON RDS_ON 0 VALUE={TABLE(V(G, S), 1.5, 200m, 1.6, 100m, 2, 85m, 2.5, 75m, 3, 70m, 3.5, 66.5m, 4, 62m, 5, 61m, 6, 60m)*V(NORM)}
E0 KP 0 VALUE={1}
VSENSE D D2 0.0
ELOAD VLOAD 0 VALUE={I(VSENSE)}
E1 G2 S VALUE={1+ ((2+V(KP)*MAX(V(VLOAD), 10m)*V(RDS_ON)*V(RDS_ON))/(2*V(KP)*V(RDS_ON)))}
M1 D2 G2 S S GENERIC_NMOS
.MODEL GENERIC_NMOS NMOS (LEVEL=1 VTO=1 W=1 L=1 CGSO=1p LAMBDA=0.0001 KP=1)
.ENDS CSD13380F3
    
```

Figure 14. PSpice CSD13380F3 model source code.

5. Simulation Results for the New CSD13380F3 MOSFET Model

The OrCAD Capture simulation test-bench of the new CSD13380F3 MOSFET model is presented in Figure 15. Additionally, from the test-bench shown in Figure 8, there is a fourth pin, TJ, which is the device temperature as a voltage. The advantage of this implementation is that the temperature can vary during the simulation and emulate the self-heating effect, which plays an important role in load switches. The same steps as for the Texas Instruments’ model are applied. For the $R_{DS(ON)}$ vs. V_{GS} characteristic, the current source is set to 0.4 A and the V_{GS} voltage source is swept between 1.5 V and 8 V.

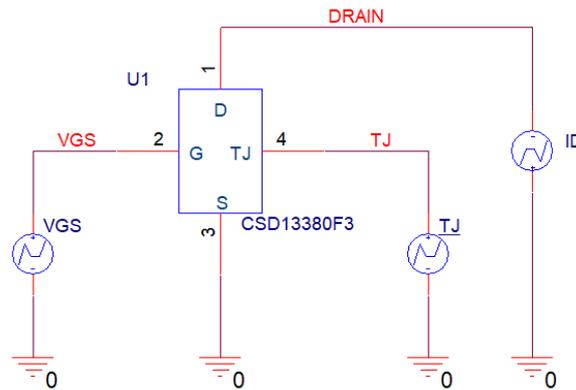


Figure 15. Simulation test-bench for the new CSD13380F3 model.

The setup used to determine the new $R_{DS(ON)}$ vs. V_{GS} characteristics is shown in Figure 16. The drain current is set to 0.4 A and V_{GS} varies between 1.5 V and 8 V for two junction temperatures (25 °C and 125 °C). It can be seen that the junction temperatures influence the V_{DS} voltage.

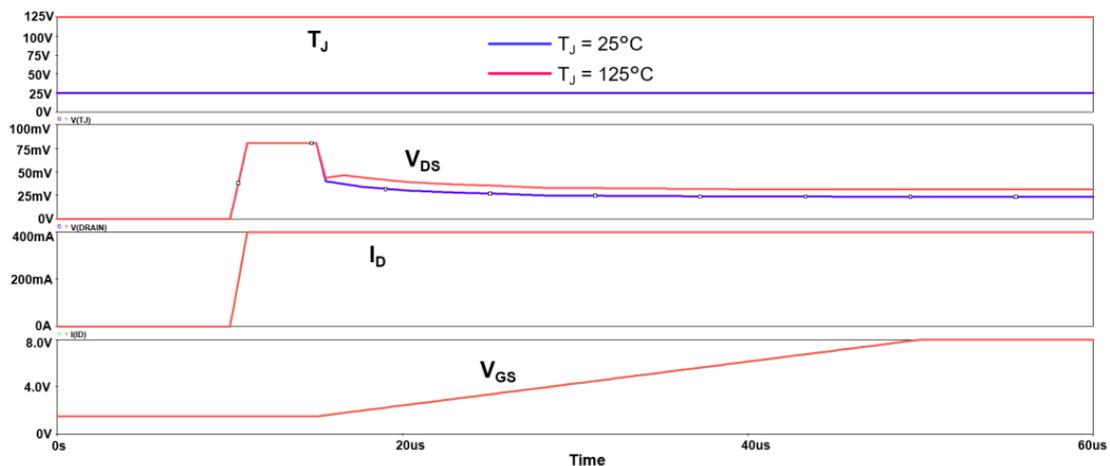


Figure 16. Simulation setup for determining the new CSD13380F3 model $R_{DS(ON)}$ vs. V_{GS} characteristics.

The waveforms shown in Figure 16 are also linked to Table 3, which presents the $R_{DS(ON)}$ calculations for the new CSD13380F3 model at V_{GS} between 1.5 V and 8 V for temperatures of 25 °C and 125 °C. It can be seen that at 25 °C, $R_{DS(ON)}$ varies between 200 mΩ and 60 mΩ, while at 125 °C, $R_{DS(ON)}$ varies between 200 mΩ and 78.6 mΩ, just like in the theoretical characteristic shown in Figure 6.

Table 3. $R_{DS(ON)}$ vs. V_{GS} calculations for the new CSD13380F3 model.

$T_{CASE} = 25\text{ }^{\circ}\text{C}$			
I_D	V_{GS}	V_{DS}	$R_{DS(ON)}$
[A]	[V]	[mV]	[mΩ]
0.4	1.5	80	200
0.4	2	34	85
0.4	2.5	30	75
0.4	3	28	70
0.4	3.5	26.6	66.5
0.4	4	24.8	62
0.4	4.5	24.6	61.5
0.4	5	24.4	61
0.4	5.5	24.2	60.5
0.4	6	24	60
0.4	6.5	24	60
0.4	7	24	60
0.4	7.5	24	60
0.4	8	24	60
$T_{CASE} = 125\text{ }^{\circ}\text{C}$			
0.4	1.5	80	200
0.4	2	43.86	109.65
0.4	2.5	38.94	97.35
0.4	3	36.56	91.41
0.4	3.5	34.95	87.38
0.4	4	32.78	81.96
0.4	4.5	32.71	81.8
0.4	5	32.38	80.95
0.4	5.5	32.04	80.12
0.4	6	31.71	79.3
0.4	6.5	31.64	79.11
0.4	7	31.57	78.94
0.4	7.5	31.5	78.77
0.4	8	31.44	78.6

Figure 17 presents the simulated $R_{DS(ON)}$ vs. V_{GS} characteristic for the newly implemented CSD13380F3 model, based on the measurements in Table 3. It can be seen that the $R_{DS(ON)}$ vs. V_{GS} characteristic of the newly implemented model matches the theoretical one shown in Figure 6, and the relative error in all voltage points is 0 or very close to 0. These remarkable obtained results prove the very high accuracy of the proposed modeling method.

The same simulation test-bench presented in Figure 15 is used to determine the normalized $R_{DS(ON)}$ vs. Temperature characteristics of the newly implemented model. For this setup, the drain current is set to 0.4 A and the temperature T_J is varied between $-50\text{ }^{\circ}\text{C}$ and $150\text{ }^{\circ}\text{C}$. Two simulations are performed for $V_{GS} = 1.8\text{ V}$ and $V_{GS} = 4.5\text{ V}$. The waveforms are presented in Figure 18. It can be noted that the V_{DS} voltage is influenced by V_{GS} and T_J .

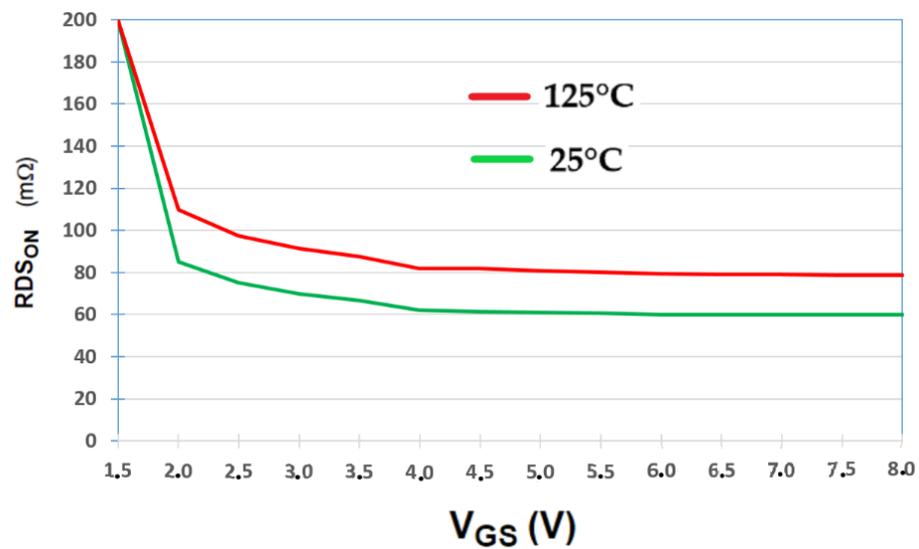


Figure 17. Simulated RDS_{ON} vs. V_{GS} for the new CSD13380F3 model.

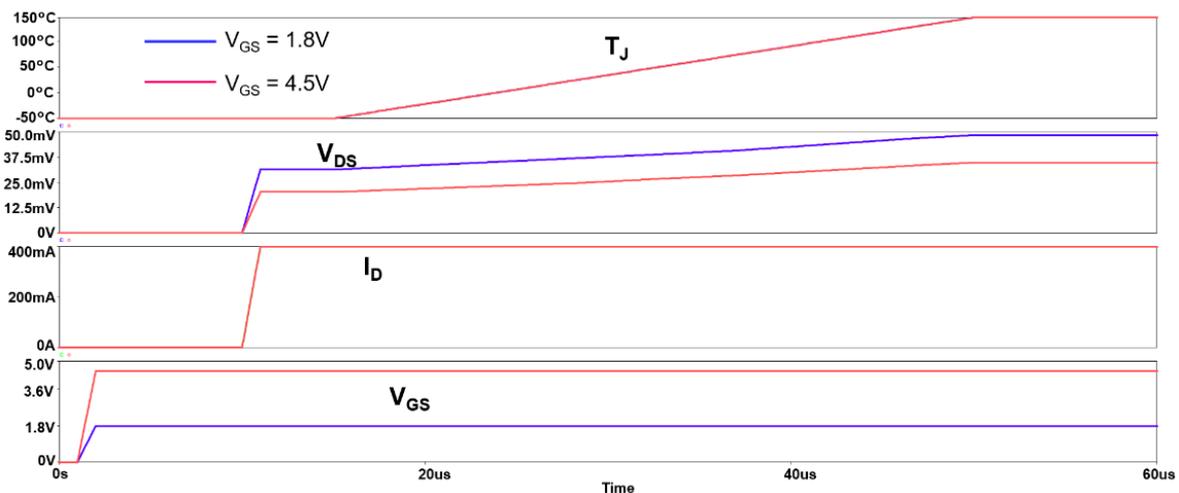


Figure 18. Simulation setup for determining the Texas new CSD13380F3 model normalized RDS_{ON} vs. T_C characteristics.

The waveforms in Figure 18 are also used to create Table 4, which contains the simulation results of the new CSD13380F3 model along with the calculated RDS_{ON} and normalized RDS_{ON} for both V_{GS} voltages (1.8 V and 4.5 V) V for temperatures between −50 °C and 150 °C, with a chosen step of 25 °C. It can be noted that for V_{GS} = 1.8 V, the normalized RDS_{ON} varies between 0.85 and 1.31, as stated before, while for V_{GS} = 4.5 V, the normalized RDS_{ON} takes values between 0.82 and 1.41.

Figure 19 presents the normalized RDS_{ON} vs. Case Temperature characteristic for the new CSD13380F3 MOSFET model, based on the results obtained in Table 4. It can be seen that the characteristic matches the theoretical one in Figure 7, the values in each frequency point being identical, which proves the value of the newly implemented model.

Table 4. $R_{DS(ON)}$ vs. Temperature simulation results for the new CSD13380F3 model.

$V_{GS} = 1.8\text{ V}$				
I_D	T_{CASE}	V_{DS}	$R_{DS(ON)}$	Normalized $R_{DS(ON)}$
[A]	[°C]	[mV]	[mΩ]	
0.4	−50	31.45	78.62	0.85
0.4	−25	33.3	83.25	0.9
0.4	0	35.15	87.87	0.95
0.4	25	37	92.5	1
0.4	50	38.85	97.12	1.05
0.4	75	40.7	101.75	1.1
0.4	100	43.47	108.68	1.175
0.4	125	46.25	115.62	1.25
0.4	150	48.47	121.17	1.31
$V_{GS} = 4.5\text{ V}$				
0.4	−50	20.17	50.43	0.82
0.4	−25	21.64	54.12	0.88
0.4	0	23.12	57.8	0.94
0.4	25	24.6	61.5	1
0.4	50	26.56	66.42	1.08
0.4	75	28.29	70.72	1.15
0.4	100	30.5	76.25	1.24
0.4	125	32.71	81.8	1.33
0.4	150	34.68	86.71	1.41

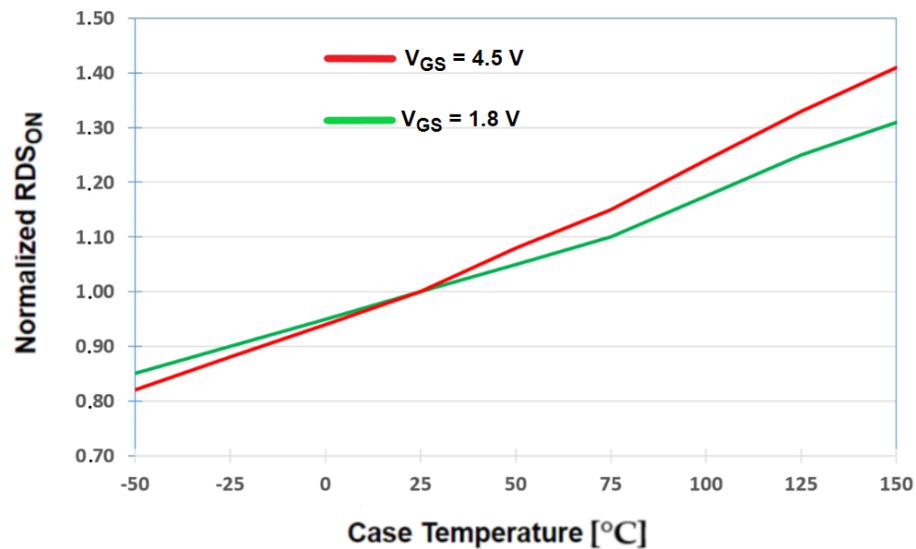


Figure 19. Simulated $R_{DS(ON)}$ vs. Case Temperature for Texas the new CSD13380F3 model.

6. Discussion and Comparison of Theoretical, Old, and New ON-State Resistance Characteristics Implementations

Table 5 compares the theoretical $R_{DS(ON)}$ vs V_{GS} characteristics of the CSD13380F3 transistor with the old Texas Instruments’ and the new proposed implementations. The relative error to the theoretical characteristic of the Texas Instruments’ model ($R_{SD(ON, TI)}$ Error) varies between 0.08% and 29.12%, while for the new model, the relative error ($R_{DS(ON, new)}$ Error) varies between 0% and 0.08%, which proves the enhancement of the new model compared to the model designed by Texas Instruments.

Table 5. $R_{DS_{ON}}$ vs. V_{GS} characteristics comparison.

$T_{CASE} = 25\text{ }^{\circ}\text{C}$					
V_{GS}	$R_{DS_{ON,theoretical}}$	$R_{DS_{ON,TI}}$	$R_{DS_{ON,TI}}$ Error	$R_{DS_{ON,new}}$	$R_{DS_{ON,new}}$ Error
[V]	[m Ω]	[m Ω]	[%]	[m Ω]	[%]
1.5	200	141.75	29.12	200	0
2	85	85.62	0.72	85	0
2.5	75	74.3	0.93	75	0
3	70	69.39	0.87	70	0
3.5	66.5	66.68	0.27	66.5	0
4	62	64.98	4.8	62	0
4.5	61.5	63.82	3.77	61.5	0
5	61	63	3.27	61	0
5.5	60.5	62.39	3.12	60.5	0
6	60	61.93	3.21	60	0
6.5	60	61.58	2.63	60	0
7	60	61.3	2.16	60	0
7.5	60	61.09	1.81	60	0
8	60	60.92	1.53	60	0
$T_{CASE} = 125\text{ }^{\circ}\text{C}$					
1.5	200	157.65	21.17	200	0
2	109.6	110.29	0.62	109.65	0.04
2.5	97.3	97.2	0.1	97.35	0.05
3	91.4	90.96	0.48	91.41	0.01
3.5	87.4	87.33	0.08	87.38	0.02
4	82	84.97	3.62	81.96	0.04
4.5	81.8	83.34	1.88	81.8	0
5	80.9	82.15	1.54	80.95	0.06
5.5	80.1	81.26	1.44	80.12	0.02
6	79.3	80.57	1.6	79.3	0
6.5	79.1	80.03	1.17	79.11	0.01
7	79	79.6	0.75	78.94	0.07
7.5	78.7	79.26	0.71	78.77	0.08
8	78.6	78.98	0.48	78.6	0

Table 6 compares the theoretical normalized $R_{DS_{ON}}$ vs Case temperature characteristics of the CSD13380F3 transistor with the ones obtained with the old Texas Instruments' model and the new proposed MOSFET model. For the Texas Instruments' model, the normalized $R_{DS_{ON,TI}}$ relative error varies between 0% and 2.35%, while for the new model, the normalized $R_{DS_{ON,new}}$ relative error varies between 0% and 0.8%, which proves once again the performance of the new proposed model.

The Texas Instruments' implementation uses a generic NMOS transistor in which the parameters are set to certain values. This way, it is impossible to control the $R_{DS_{ON}}$ precisely over a wide domain of temperatures and voltages. The advantage of this novel technique is that, in addition to using a generic NMOS transistor, it monitors the temperature, load current, and automatically adapts internally the applied V_{GS} voltage, such that the transistor $R_{DS_{ON}}$ matches the theoretical value. Hence, the $R_{DS_{ON}}$ accuracy can be kept over the entire range of temperatures, currents, or voltages.

Table 6. $R_{DS_{ON}}$ vs. Case temperature characteristic comparison.

$V_{GS} = 1.8 \text{ V}$					
Temperature	Normalized $R_{DS_{ON,theoretical}}$	Normalized $R_{DS_{ON,TI}}$	Normalized $R_{DS_{ON,TI}}$ Error	Normalized $R_{DS_{ON,new}}$	Normalized $R_{DS_{ON,new}}$ Error
[°C]			[%]		[%]
−50	0.85	0.83	2.35	0.85	0
−25	0.9	0.88	2.22	0.9	0
0	0.95	0.94	1.05	0.95	0
25	1	1	0	1	0
50	1.05	1.06	0.95	1.05	0
75	1.1	1.12	1.81	1.1	0
100	1.18	1.19	0.84	1.175	0.42
125	1.24	1.26	1.61	1.25	0.8
150	1.31	1.34	2.29	1.31	0
$V_{GS} = 4.5 \text{ V}$					
−50	0.82	0.83	1.21	0.82	0
−25	0.88	0.88	0	0.88	0
0	0.94	0.94	0	0.94	0
25	1	1	0	1	0
50	1.08	1.06	1.85	1.08	0
75	1.15	1.14	0.86	1.15	0
100	1.24	1.22	1.61	1.24	0
125	1.32	1.31	0.75	1.33	0.75
150	1.41	1.4	0.7	1.41	0

7. Conclusions

In this paper, for the first time, a novel ON-state resistance modeling technique for MOSFET power switches was presented, which is based on modulating the gate-source voltage of the MOSFET such that the target $R_{DS_{ON}}$ is obtained.

The new proposed method combines mathematical relations and circuits' relations, as follows:

- The starting point was a transistor model existing on the market, CSD13380F3, from Texas Instruments, which is a 12 V N-channel MOSFET that can be used for load switching applications. The transistor's model is available on the website of Texas Instruments [22] and contains the transistor symbol and the PSpice library file.
- Firstly, the transistor model designed by Texas Instruments was simulated using OrCAD Capture environment and its $R_{DS_{ON}}$ vs. V_{GS} characteristics at 25 °C and 150 °C, along with the $R_{DS_{ON}}$ vs. Case Temperature at $V_{GS} = 1.8 \text{ V}$ and $V_{GS} = 4.5 \text{ V}$ were plotted. The $R_{DS_{ON}}$ vs. V_{GS} relative error to the theoretical characteristics varies between 0.08% and 29.12%, while the $R_{DS_{ON}}$ vs. Case Temperature error varies between 0% and 2.35%. It was noticed that the temperature can be set only as a simulator parameter and cannot be modified dynamically during the simulation.
- Afterwards, the new CSD13380F3 MOSFET model was implemented using the novel $R_{DS_{ON}}$ modeling technique. This technique calculates the necessary voltage V_{GS} needed, such that the MOSFET switch operates at a certain $R_{DS_{ON}}$. When setting the V_{GS} externally, the $R_{DS_{ON}}$ value automatically sets at the target value and the only input needed from the user is the theoretical $R_{DS_{ON}}$ characteristic.
- After simulating the newly proposed model, the $R_{DS_{ON}}$ vs. V_{GS} and $R_{DS_{ON}}$ vs. Case Temperature characteristics were plotted. The relative error for the $R_{DS_{ON}}$ vs. V_{GS} curves varies between 0% and 0.08%, while the relative error for the $R_{DS_{ON}}$ vs. Case Temperature characteristics is between 0% and 0.8%.

Comparing the Texas Instruments' model and the newly implemented model, the advantages are:

- ✓ The new model accurately matches the datasheet characteristics presented in Figures 6 and 7. The maximum error obtained for this new model is 0.8%, whereas the maximum Texas Instruments model error is 29.12%.
- ✓ The new MOSFET model has an independent temperature pin, which allows the user to adjust the temperature dynamically during the simulation and, in this way, can emulate the self-heating effect of the transistor.
- ✓ The novel ON-state resistance modeling technique allows for the accurate modeling of any MOSFET power switch only by defining the datasheet $R_{DS(ON)}$ variation. The literature does not provide any research on modeling the $R_{DS(ON)}$ in all possible corners, only at discrete temperature and/or voltages, so the new proposed method is a breakthrough in the simulation domain and can be used successfully in creating accurate MOSFET behavioral models.
- ✓ A transistor model created using the novel $R_{DS(ON)}$ modeling technique is able to match the real behavior of the component over the entire operating range, thus, assuring compatibility between simulation and physical testing.
- ✓ Highly reliable MOSFET power switch models can be built using the new technique in a fast and efficient manner, only by defining the theoretical $R_{DS(ON)}$ characteristics.

The implementation achieved in this paper also proves extremely important in the electronics domain, where the simulation has become the main testing concept. Through simulation, the engineers are able to validate the circuit before the physical implementation and this avoids additional costs involved by faults present in the circuit's design. Since the MOSFET transistors are found in many applications (low-dropout linear voltage regulators, switching regulators, gate drivers, battery management systems), it is mandatory to create accurate behavioral models for them, but in order to achieve this goal, an essential parameter must be taken into consideration, namely the ON-state resistance. Using the novel technique presented in this paper, the transistor model $R_{DS(ON)}$ accuracy can be kept over the entire range of temperatures, currents, or voltages.

Other future research directions consist of enhancements in the current CSD13380F3 MOSFET model in order to integrate the output voltage slew rate setting when using the transistor as a MOSFET switch.

Author Contributions: Conceptualization, I.-C.G., A.F. and L.A.P.; methodology, I.-C.G., A.F. and L.A.P.; software, I.-C.G.; validation, I.-C.G., A.F. and L.A.P.; formal analysis, I.-C.G., A.F. and L.A.P.; investigation, I.-C.G.; resources, I.-C.G., A.F. and L.A.P.; data curation, I.-C.G., A.F. and L.A.P.; writing—original draft preparation, I.-C.G.; writing—review and editing, A.F. and L.A.P.; visualization, A.F. and L.A.P.; supervision, A.F. and L.A.P.; project administration, I.-C.G., A.F. and L.A.P.; funding acquisition, A.F. and L.A.P. All authors have read and agreed to the published version of the manuscript.

Funding: This work was supported by a grant from the Romanian Ministry of Education and Research, CCCDI—UEFISCDI, project number PN-III-P2-2.1-PED-2019-2862, within PNCDI III.

Data Availability Statement: Data is contained within the article.

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Pratap, R.; Singh, R.K.; Agarwal, V. SPICE Model development for SiC Power MOSFET. In Proceedings of the 2012 IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES), Bengaluru, India, 16–19 December 2012; pp. 1–5.
2. Baba, S.; Gieraltowski, A.; Jasinski, M.; Blaabjerg, F.; Bahman, A.; Zelechowski, M. Active Power Cycling Test Bench for SiC Power MOSFETs—Principles, Design, and Implementation. *IEEE Trans. Power Electronics* **2021**, *36*, 2661–2675. [[CrossRef](#)]
3. Galadi, A. Dynamic model of power Mosfet for Spice circuit simulation. In Proceedings of the 2019 IEEE 5th International Conference on Optimization and Applications (ICOA), Kenitra, Morocco, 25–26 April 2019; pp. 1–4.
4. Bayant Jaliga, B. *Advanced Power Mosfet Concepts*; Springer: New York, NY, USA, 2010; pp. 1–4.
5. Barkhordarian, V. Power Mosfet Basics. Available online: <https://www.infineon.com/dgdl/mosfet.pdf?fileId=5546d462533600a4015357444e913f4f> (accessed on 8 September 2022).

6. Zhao, W.; Wei, P. PSpice system simulation application in electronic circuit design. In Proceedings of the 32nd Chinese Control Conference, Xi'an, China, 26–28 July 2013; pp. 8634–8636.
7. Cadence Design System. In *PSpice Reference Guide*, 2nd ed.; Cadence Design Systems: Tigard, OR, USA, 2000.
8. Berry, A.; Brown, A.; Clifton, B.; Dyer, J. *The Power MOSFET Application Handbook; Design Engineer's Guide*; NXP Semiconductors: Manchester, UK, 2017; pp. 19–30.
9. Stefanskyi, A.; Starzak, L.; Napieralski, A.; Lobur, M. Analysis of SPICE models for SiC MOSFET power devices. In Proceedings of the 2017 IEEE 14th International Conference The Experience of Designing and Application of CAD Systems in Microelectronics (CADSM), Lviv, Ukraine, 21–25 February 2017; pp. 79–81.
10. He, C.; Victory, J.; Xiao, Y.; Vleschouwer, H.; Zheng, E.; Hu, Z. SiC MOSFET Corner and Statistical SPICE Model Generation. In Proceedings of the 2020 IEEE 32nd International Symposium on Power Semiconductor Devices and ICs (ISPSD), Vienna, Austria, 13–18 September 2020.
11. Hsu, F.-J.; Yen, C.-T.; Hung, C.-C.; Lee, C.-Y.; Lee, L.-S.; Chu, K.-T.; Li, Y.-F. High accuracy large-signal SPICE model for silicon carbide MOSFET. In Proceedings of the 2018 IEEE 30th International Symposium on Power Semiconductor Devices and ICs (ISPSD), Chicago, IL, USA, 13–14 May 2018; pp. 403–406.
12. Borghese, A.; Riccio, M.; Maresca, L.; Breglio, G.; Irace, A. An Electrothermal Compact Model for SiC MOSFETs Based on SPICE Primitives with Improved Description of the JFET Resistance. In Proceedings of the 2022 IEEE 34th International Symposium on Power Semiconductor Devices and ICs (ISPSD), Vancouver, BC, Canada, 22–25 May 2022; pp. 37–40.
13. Batarseh, I.; Harb, A. *Power Electronics. Circuit Analysis and Design*, 2nd ed.; Springer: Cham, Switzerland, 2018; pp. 60–67.
14. Lu, B.; Cui, M.; Liu, W. The Impact of AlGaN Barrier on Transient VTH Shifts and VTH Hysteresis in Depletion and Enhancement mode AlGaN/GaN MIS-HEMTs. In Proceedings of the 2019 IEEE International Conference on IC Design and Technology (ICICDT), Suzhou, China, 17–19 June 2019; pp. 1–4.
15. Zhang, B.; Wang, J.; Wang, C.; Wang, X.; Huang, C.; He, J.; Wang, M.; Mo, J.; Hu, Y.; Wu, W. Monolithic Integration of GaN-Based Enhancement/Depletion-Mode MIS-HEMTs With AlN/SiN Bilayer Dielectric. *IEEE Electron Device Lett.* **2022**, *43*, 1025–1028. [[CrossRef](#)]
16. Marshall Leach, W. *The MOSFET*; Georgia Institute of Technology, School of Electrical and Computer Engineering: Atlanta, Georgia, 2010; pp. 1–10.
17. Liou, J.J.; Ortiz-Conde, A.; Garcia-Sanchez, F. *Analysis and Design of MOSFETs. Modeling, Simulation and Parameter Extraction*; Springer Science + Business Media: New York, NY, USA, 1998; pp. 216–220.
18. Load Switches. Available online: https://www.nxp.com/products/power-management/load-switches:MC_71730 (accessed on 13 September 2022).
19. High-Side Switches and MOSFET Drivers. Available online: <https://www.analog.com/en/parametricsearch/11395#/> (accessed on 13 September 2022).
20. N-channel MOSFETs. Available online: <https://www.ti.com/power-management/mosfets/n-channel-transistors/overview.html> (accessed on 13 September 2022).
21. CSD13380F3 12-V N-Channel FemtoFET MOSFET. 2022. Available online: https://www.ti.com/lit/ds/symlink/csd13380f3.pdf?ts=1663568836532&ref_url=https%253A%252F%252Fwww.google.com%252F (accessed on 19 September 2022).
22. Texas Instruments. Available online: www.ti.com (accessed on 20 September 2022).
23. Cheung, N. MOSFET I-V Analysis. EE143 Lecture #24; University of California: Berkeley, CA, USA.
24. Palermo, S. *Analog & Mixed-Signal Center, ECEN474: (Analog) VLSI Circuit Design Fall 2012. Lecture 4: MOS Transistor Modeling*; Texas A&M University: College Station, TX, USA, 2012.

Disclaimer/Publisher's Note: The statements, opinions and data contained in all publications are solely those of the individual author(s) and contributor(s) and not of MDPI and/or the editor(s). MDPI and/or the editor(s) disclaim responsibility for any injury to people or property resulting from any ideas, methods, instructions or products referred to in the content.