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Optimized Power Supply Rejection Ratio Modeling Technique for Simulation of Automotive Low-Dropout Linear Voltage Regulators

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Abstract: In the automotive domain, the vast majority of testing is performed through simulations, which can validate a system design before the actual implementation and can emphasize eventual faults in the design process. Hence, the simulation is of utmost importance. Behavioral models are necessary for the creation of each electronic device desired in the system, and some of the components have very complex behavior: low-dropout linear voltage regulators (LDOs), gate drivers, and switching regulators. In the automotive industry, LDOs are essential components because they power all the other subsystems and very accurate behavior is needed to make sure that the system behaves as in reality. LDO models are already commercially available and most of their intrinsic characteristics are modeled (dropout voltage, line regulation, load regulation, etc.). However, one characteristic that is extremely useful, yet the hardest to model, is the power supply rejection ratio (PSRR). This paper proposes a new PSRR modeling technique for automotive low-dropout voltage regulators. The new PSRR characteristic was modeled for an automotive LDO product in a Texas Instruments portfolio, which has a commercially available model, and was simulated using the PSpice Allegro simulator and the OrCAD Capture CIS environment.

Keywords: simulation; optimal behavioral modeling; automotive; low-dropout linear voltage regulator; power supply rejection ratio

MSC: 97M50

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1. Introduction

In recent years, the automotive domain has seen an increase in the complexity of modern cars, which will continue to become increasingly complex. The number of electronic functions and components in cars is also rapidly increasing, which can lead to design problems in complex modular systems [1].

Supplying and conditioning electrical power are the most important features of an electrical system. No application can fully perform its function without a stable supply. Batteries, generators, and other off-line supplies provide substantial voltage and current variations over time and over a wide range of operating conditions [2]. Noise is produced due to their inherent nature, but also by high-power switching circuits such as DC–DC converters, controllers for electric motors, actuators, and relays. This noise analysis is increasingly important in the case of Electric Vehicles (EVs) or Hybrid Electric Vehicles (HEV) from the Electromagnetic Interference (EMI) point of view [2,3].

Rapidly changing loads result in unwanted voltage changes and frequency harmonics over an ideal direct current (DC) component. The goal of a voltage regulator is to convert the noisy supply into a stable, accurate, load-independent voltage and hence attenuate the fluctuations to desired levels [2–4]. One of the most used power supply circuits in the

automotive domain is the low dropout (LDO) voltage regulator, which uses a unipolar MOS or a bipolar pass transistor in its structure as a series control element to provide a regulated output voltage over a wide range of supply voltages or load current variations [5–8].

Simulation is used in the automotive domain for the validation of a design before physical implementation, and can indicate flaws and faults in the design process or reinforce the correct functioning of the system. For a highly reliable simulation, accurate component models are necessary, for which the simulated behavior must be as close as possible (ideally, identical) to the real behavior. Simulation Program for Integrated Circuits Emphasis (SPICE) is a general-purpose analog and mixed-mode simulator that is used to verify and predict circuit behavior. PSpice is the PC version of SPICE, and is used to simulate the behavior of circuits on a digital computer, emulating the signal generators, multimeters, oscilloscopes, and frequency spectrum analyzers, and includes analog and digital libraries of standard components. As a result, it is an important tool for a wide range of analog and digital applications [9].

In automotive design, internal clean power supplies having a high Power Supply Rejection Ratio (PSRR) are a vital requirement to increase power management efficiency in system-on-chip circuitry [10].

The literature focuses only on PSRR physical design and measurement [3,5,7,10], and does not provide any research on PSRR modeling techniques. This paper proposes an optimization approach in the simulation domain, and emphasizes a highly accurate method of modeling the PSRR for automotive LDOs. The main contributions are listed below:

- implementation of a new PSRR model for the TPS785-Q1 automotive LDO from Texas Instruments;
- simulation of the LDO model with the initial PSRR functionality, as is currently commercially available;
- simulation of the LDO model with the new PSRR functionality added using the PSpice Allegro simulator and OrCAD Capture CIS 17.2 simulation environment;
- comparison of the results using the values of the theoretical and previous approaches.

The remainder of the paper is organized as it follows: Section 2 shows the background related to this work and presents the currently existing PSRR vs. frequency characteristic of TPS785-Q1 from Texas Instruments, Section 3 emphasizes the materials and methods for the new PSRR model implementation, and Section 4 presents the numerical simulation results in tables and waveform figures. The comparison between the theoretical, previous, and new PSRR characteristics of the TPS785-Q1 model is presented in Section 5. The conclusions are synthesized in Section 6.

2. Background of LDO PSRR

The LDO is commonly used in power electronics design as the last stage of the power-distribution tree. In the first stage, an intermediate voltage is obtained from the input voltage of a supply system using other topologies, such as DC–DC or AC–DC converters. These topologies introduce harmonics and supraharmonics, generating a noisy intermediate voltage. The supraharmonics are defined as current and voltage waveforms distortion within the range 2–150 kHz, that can be intentionally created by power line communication systems or unintentionally by power electronic converters. In stage two, the LDO regulator generates the system output voltage from the intermediate voltage. The objective is to achieve a high power conversion efficiency in stage one and to remove the switching noise in stage two. The noise can be technically translated into an unwanted voltage ripple that must be eliminated [11], thus justifying the study of PSRR in this paper. For example, in automotive applications, the car battery delivers the supply voltage that can vary between 6 and 30 V, having slew rates of up to 1 V/µs. In addition, the load current can vary drastically, with slew rates of up to 50–100 mA/µs. These very high slew-rates also introduce harmonics, which translate into unwanted voltage spikes that must also be eliminated; this elimination is also achieved by the new proposed PSRR model [6].

The simplified working principle of a regular LDO voltage regulator is shown in Figure 1, and contains the input voltage V_{IN}, the pass transistor element Q, the error amplifier K, and the resistive network (R_1, R_2), which sets the desired output voltage V_{OUT}. The error amplifier compares the positive terminal voltage of $V_{OUT} * [R_2/(R_1 + R_2)]$ with the reference voltage V_{REF} connected to the negative terminal and drives the pass transistor accordingly such that the two voltages become equal.

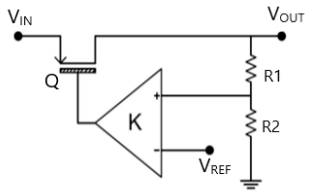

Figure 1. LDO voltage regulator principle [12].

The most common characteristics that need to be taken into consideration when creating a LDO voltage regulator model are: output voltage accuracy, line regulation, load regulation, current consumption, dropout voltage, output voltage slew-rate, protections, and PSRR [13,14].

Some examples of these characteristics are presented in Figure 2a–f, being taken from Texas Instruments' TPS785-Q1 automotive LDO product [14].

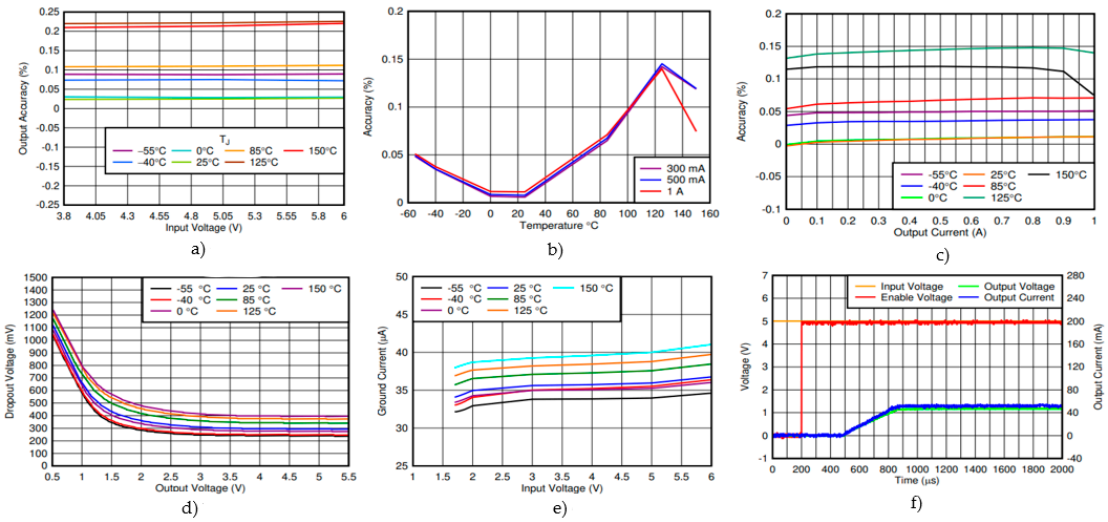

Figure 2. Examples of characteristics for TPS785-Q1: (**a**) output voltage accuracy vs input voltage; (**b**) output voltage accuracy vs temperature; (**c**) output voltage accuracy vs output current; (**d**) dropout voltage vs output voltage; (**e**) ground current vs input voltage; (**f**) output voltage and slew-rates.

Existing LDO models are commercially available from companies such as Texas Instruments, Infineon, and Analog Devices, but only newer products have different behavioral models for some simulation software environments, such as PSpice Allegro, TINA, SIMetrix.

TPS785-Q1 from Texas Instruments portfolio is an ultra-low-dropout regulator with a low quiescent current that can source 1 A with excellent load and line transient performance. It is qualified for automotive applications according to the AEC-Q100 standard, and has a junction temperature varying from −40 to +150 °C. The low output noise and good PSRR performance make the product suitable for power-sensitive analog loads [14].

TPS785-Q1's typical application circuit as a post regulator is shown in Figure 3. The DC–DC converter is used as the main regulator. It is supplied by the battery voltage V_{BAT} and produces an output voltage V_{OUT1}, which is inherently noisy. Capacitors C_{OUT1} and

C_{IN} have the role of reducing the ripple appearing at the input of TPS785-Q1, and capacitor C_{OUT} reduces the output voltage V_{OUT} ripple [14].

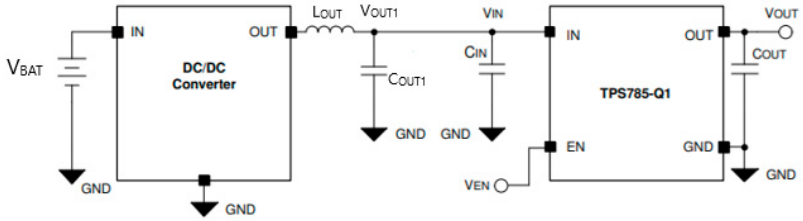

Figure 3. Typical application for the TPS785-Q1 voltage regulator [14].

The post regulator supports an input voltage range from 1.7 to 6.0 V and offers an adjustable output range of 1.2 to 5.5 V. TPS785-Q1 takes the output voltage of the DC–DC converter and regulates it to the desired level V_{OUT}, eliminating the switching noise introduced by the converter [14].

The power supply rejection ratio is defined as the measurement of the magnitude of the output voltage ripple ΔV_{OUT} compared to the input voltage ripple ΔV_{IN} [11,15]:

$$\text{PSRR} = 20 \log_{10} \left(\frac{\Delta V_{IN}}{\Delta V_{OUT}} \right) \quad (1)$$

Theoretically, the ideal PSRR is infinite. In practice, PSRR has a big value, so that the measurement unit used is decibel (dB). Empirically, a high PSRR is considered to be a value over 60 dB [11,15].

The PSRR is a very important characteristic in the power electronics and automotive domains. Figure 4 represents the PSRR characteristic of the TPS785-Q1 automotive high PSRR LDO [14], which has its maximum PSRR of around 70 dB between 10 and 40 Hz. This value of PSRR is enough to consider it a high PSRR LDO, but the input voltage supply's switching frequency is also vital [11,16,17]. For example, the switching frequency of newer switching regulators is between 300 kHz and 6 MHz, and the LDO response time is too slow to efficiently filter out the switching noise, due to the fact that the noise is outside the bandwidth of most typical high PSRR regulators [11,18].

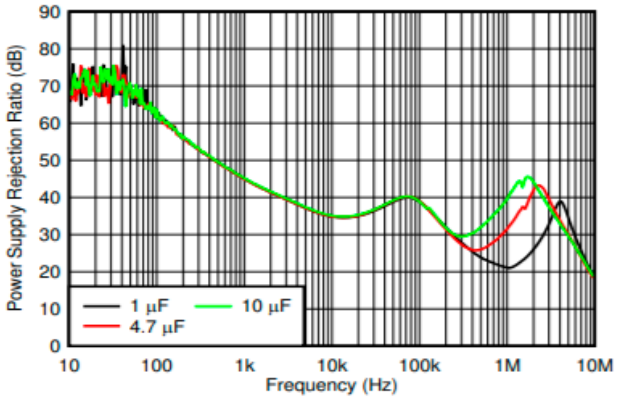

Figure 4. PSRR vs. C_{OUT} at V_{OUT} = 3.3 V and I_{OUT} = 1 A [14].

There are five regions represented in Figure 4. The first region contains the frequency range from 10 to 40 Hz, where the PSRR has its peak (70 dB), and is approximately a flat curve. The frequency range 40 Hz–10 kHz, where PSRR decreases steadily at 20 dB/decade, forms the second region. In the third region (10–70 kHz) PSRR increases again to 40 dB. The fourth region sees a decrease in PSRR from 40 to 30 dB at 300 kHz. The first four regions are the effective PSRR bandwidth; thus, TPS785-Q1 has an effective frequency range between 0 Hz and 300 kHz. In the fifth region (300 kHz–10 MHz), the change in PSRR depends on

the numerical value of the output capacitor C_{OUT} (Figure 3) and its impedance, and the parasitic board impedance; thus, the LDO contribution to PSRR decreases.

The behavioral model of TPS785-Q1 provided by Texas Instruments is a PSpice Allegro library file [19]. We ran the model with the simple application circuit created in the OrCAD Capture CIS environment (Figure 5). The output voltage was set at 2.4 V and the load current at 1 mA.

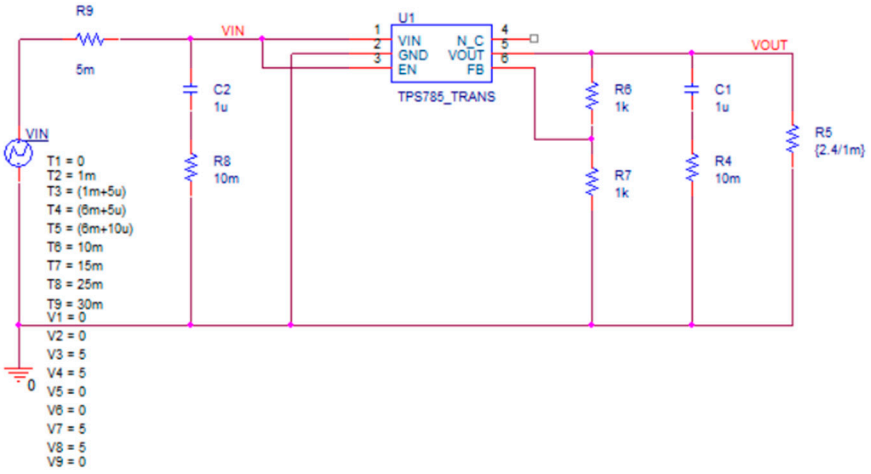

Figure 5. Demonstration application circuit of TPS785-Q1 provided by Texas Instruments [19].

Figure 6 shows the results obtained using the demo application test-bench. In the beginning of the simulation, there is an abrupt 5 V pattern of the input voltage V_{IN} for both rising and falling edges (1–6 ms) and the output voltage V_{OUT} regulates at 2.4 V within a certain slew-rate. The second pattern shows slower slopes of the input voltage VIN for the rising and falling edges (10–30 ms). It can be noted that there is a certain threshold of the input voltage above which the LDO starts working.

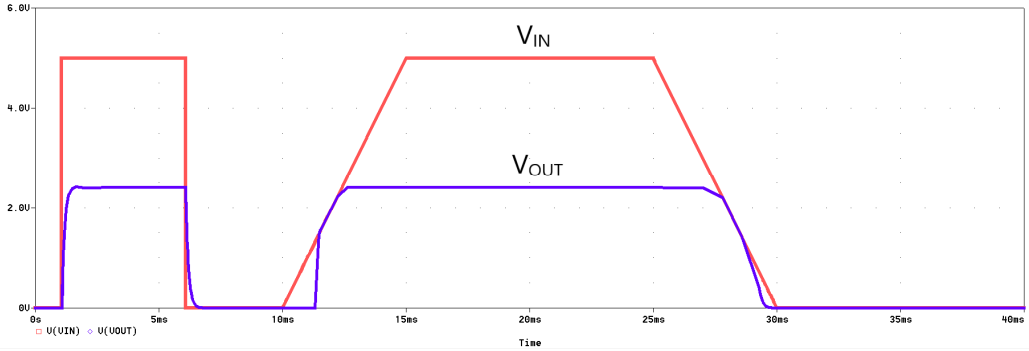

Figure 6. Simulation results for the demo application circuit of TPS785-Q1.

From the unencrypted library file, we found that this TPS785-Q1 model is a transient model, built for the PSpice Allegro simulator only, and is in its first version. The existing implemented characteristics are the following: start-up time, PSRR, enable/VIN shutdown, load and line transients, and internal current limit, and the model supports inverting the topology. In order to better understand how the PSRR model works, we further performed a reverse engineering of the library file code, so Figure 7a represents the simplified concept of the TPS785-Q1 model, along with the general PSRR concept that is currently implemented [11,20]. It consists of the error amplifier EA, the reference voltage V_{REF}, the pass transistor MOS1, the feedback resistors R_{UP} and R_{DW}, the output capacitor C_{OUT} with its series resistance R_{ESR}, and load resistor R_{LOAD}. The components can be grouped into two impedances, Z_A and Z_B.

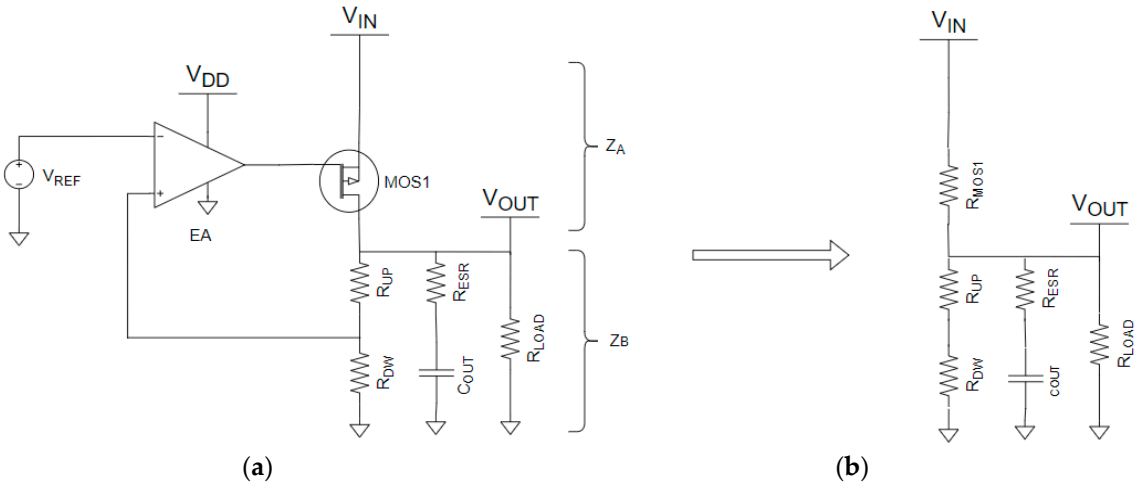

Figure 7. Concept diagram of TPS785-Q1 model: (**a**) general simplified PSRR model concept; (**b**) high frequency PSRR model concept.

The PSRR can be calculated as it follows:

$$\text{PSRR} = 20\ \log_{10}\left(\frac{Z_A + Z_B}{Z_B}\right) \tag{2}$$

In the first region of PSRR vs. frequency characteristic from Figure 4, the error amplifier has a large gain and this results in Z_A being well controlled, which translates into a high PSRR. In the second region, the gain of the amplifier starts dropping at 20 dB/decade. The sensitivity of the loop with respect to the changes in the output voltage decreases because the amplifier gain decreases; thus, the impedance of the transistor adjusts slower to the changes and this results in a decrease in PSRR. The impedance of the output capacitor decreases with the increase in the input signal frequency and this increases the LDO PSRR in the fifth region. The impedance Z_B decreases to the point where most of the signal is short-circuited across the capacitor instead of being attenuated by the LDO. In this case, where the LDO no longer contributes significantly to the PSRR, the pass transistor MOS1 is treated as a simple resistor and only attenuates the ripple passively [11,20]. This situation is revealed in Figure 7b, which was drawn for high frequencies, and differs from Figure 7a by eliminating the LDO and replacing the pass transistor MOS1 with a simple resistor R_{MOS1}.

We also simulated the PSRR characteristic of the already existing TPS785-Q1 model. The PSRR simulation test-bench is provided in Figure 8.

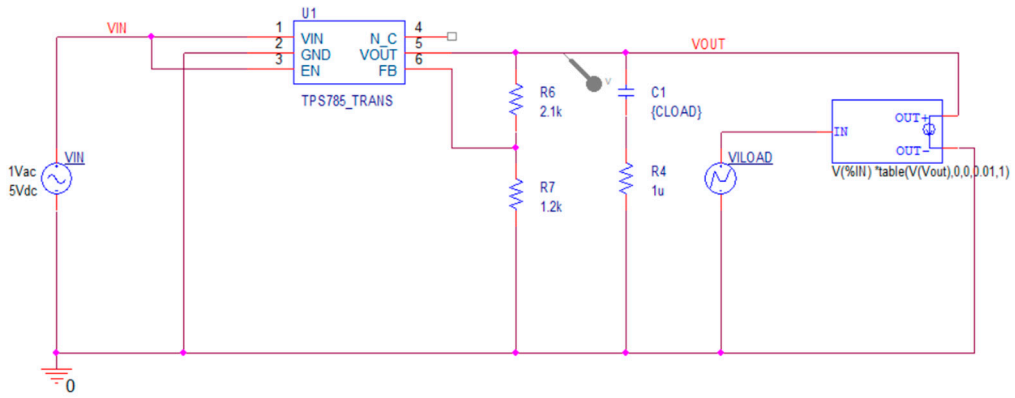

Figure 8. Test-bench circuit for AC analysis of TPS785-Q1 PSRR.

The input voltage source V_{IN} is a 5 V DC component on which a 1 V amplitude sine component modeling the additive noise is overlapped. The output voltage V_{OUT} is set

at 3.3 V and the load current is set at 1 A, as specified by the PSRR conditions. The load capacitor C1 is given three values (1, 4.7, and 10 µF) through parameter {CLOAD}, so three simulations were performed.

Figure 9 shows the family of simulated PSRR characteristics vs. frequency, having the capacitor C1 {CLOAD} from Figure 8 as the parameter. Thus, the violet curve shows the 1 µF capacitor's value, the red curve shows the 4.7 µF capacitor's value, and the green curve shows the 10 µF capacitor's value. Compared to the datasheet characteristic presented in Figure 4, the flat region is at 60 dB instead of 70 dB, which represents a disadvantage of the old PSRR model given in [14]. The capacitor influence is visible from around 1 kHz, whereas the datasheet characteristic sees a capacitor influence starting at 300 kHz.

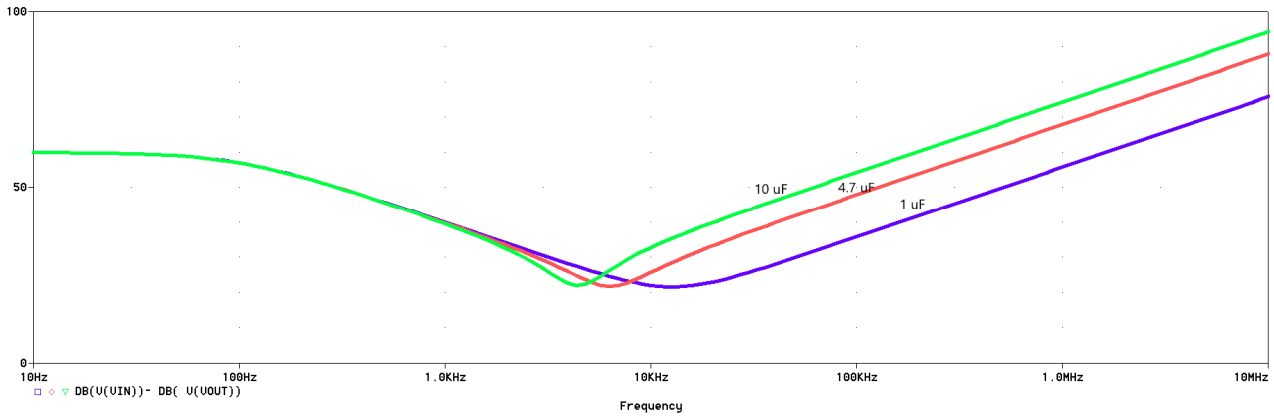

Figure 9. Simulated old PSRR characteristic of the TPS785-Q1 model.

3. Materials and Methods for the New Proposed PSRR Model Implementation

For materials, we started from the existing TPS785-Q1 model from Texas Instruments, from which we eliminated the old PSRR characteristic, and added our new PSRR concept, as shown in Figure 10. For the method, we implemented the PSRR functionality by modifying the reference voltage V_{REF_IN}. The ideal reference voltage V_{REF_IN} of the LDO is added to the PSRR voltage source V_{PSRR}, which depends on the ripple of the input voltage V_{IN} and its frequency, and the result is V_{REF_OUT}. Then, V_{REF_OUT} is sent through the feedback resistors R_{UP} and R_{DW} (Figure 7a), and yields the output voltage V_{OUT} and its variations (Figure 7a).

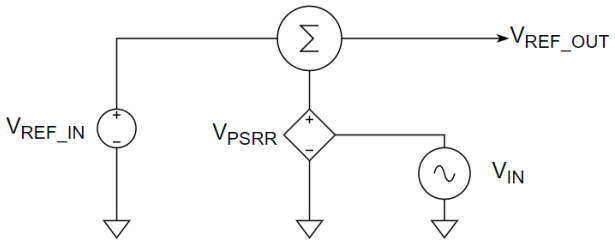

Figure 10. New LDO PSRR model concept.

In Figure 10, the PSRR source V_{PSRR} holds the information about the input voltage source ripple ΔV_{IN} and frequency, which is demonstrated below. V_{IN} is DC shifted and the DC information needs to be eliminated from the original signal. We used a first order passive low pass filter to determine the input signal V_{IN} frequency, and a second order active low pass filter to eliminate the DC component of V_{IN}. The first order low pass filter schematic is shown in Figure 11a, and the second order active low pass filter concept is presented in Figure 11b.

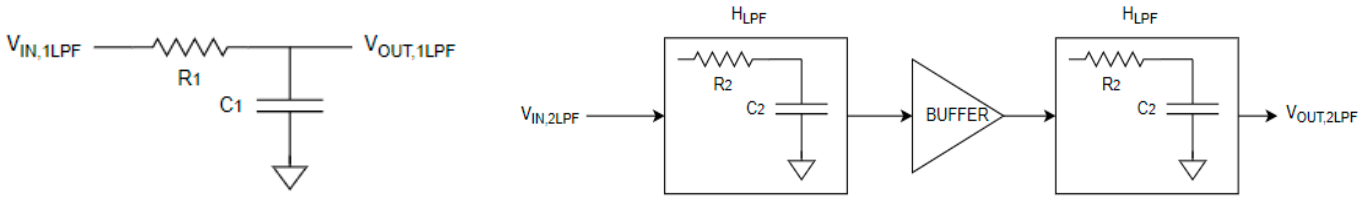

Figure 11. First and second order low pass filters: (**a**) first order passive filter schematic; (**b**) second order active low pass filter concept.

The transfer function of the first order low pass filter is:

$$H_{1LPF}(j\omega) = \frac{1}{1 + j\omega R_1 C_1} = \frac{1}{1 + j2\pi f R_1 C_1} \tag{3}$$

where $\omega = 2\pi f$ is the angular frequency, f is the frequency, R_1 is the low pass filter resistance value, and C_1 is the low pass filter capacitance value (Figure 11a).

The transfer function magnitude of the first order low pass filter is:

$$|H_{1LPF}(j\omega)| = \frac{1}{\sqrt{1 + \omega^2 R_1^2 C_1^2}} = \frac{1}{\sqrt{1 + 4\pi^2 f^2 R_1^2 C_1^2}} \tag{4}$$

and the transfer function phase of the first order low pass filter is:

$$\varphi_{1LPF}(j\omega) = -\tan^{-1}(\omega R_1 C_1) = -\tan^{-1}(2\pi f R_1 C_1) \tag{5}$$

Having a second order active filter in which the two stages are separated galvanically by a buffer, the total transfer function can be written as shown in Equation (6), based on relation Equation (3), with the magnitude and phase calculated in Equations (7) and (8). The components' values are chosen to be equal due to the simplicity of calculations (Figure 11b) [21–23].

$$H_{2LPF}(j\omega) = H_{LPF}(j\omega) \cdot H_{LPF}(j\omega) = \frac{1}{1 + j\omega R_2 C_2} \cdot \frac{1}{1 + j\omega R_2 C_2} = \frac{1}{(1 - \omega^2 R_2^2 C_2^2) + j2\omega R_2 C_2} \tag{6}$$

where the magnitude of the transfer function is:

$$|H_{2LPF}(j\omega)| = \frac{1}{\sqrt{(1 - \omega^2 R_2^2 C_2^2)^2 + 4\omega^2 R_2^2 C_2^2}} = \frac{1}{1 + \omega^2 R_2^2 C_2^2} = \frac{1}{1 + 4\pi^2 f^2 R_2^2 C_2^2} \tag{7}$$

and its phase is:

$$\varphi_{2LPF}(j\omega) = -\tan^{-1}\frac{2\omega R_2 C_2}{1 - \omega^2 R_2^2 C_2^2} = -\tan^{-1}\frac{4\pi f R_2 C_2}{1 - 4\pi^2 f^2 R_2^2 C_2^2} \tag{8}$$

The cutoff frequency (where the magnitude of the transfer function drops to −3 dB) of the second order active filter is:

$$f_{-3dB,\,2LPF} = \frac{1}{2\pi R_2 C_2} \tag{9}$$

In order to achieve the DC component of the voltage V_{IN}, we used relations Equations (6) and (7), in which we chose the resistance value R_2 of 1 MΩ and capacitance C_2 of 1 mF, which leads to f_{-3dB} = 0.000160 Hz, i.e., a numerical value very near to 0 Hz.

Another challenge of modeling the characteristic PSRR vs. frequency is to determine the frequency of the input signal V_{IN}, by filtering the input ripple signal ΔV_{IN}, once again using a first order low pass filter, and then compute the root mean square (RMS) values of

the input and output signals of the filter, $V_{RMS,IN}$ and $V_{RMS,OUT}$ [24,25]. We set the filter cutoff frequency to 40 Hz, where the PSRR characteristic starts dropping at 20 dB/decade from the flat region (Figure 4). The cutoff frequency of the first order low pass filter is identical to that of the second order low pass filter, which uses the same values for the resistors and for the capacitors. In order to achieve this cutoff frequency, the filter resistor R_1 was set to 10 kΩ and, based on relation Equation (9), the resulting value of capacitor C_1 was 1.6 nF.

Since the signal at the output of the filter is phase shifted, the ratio of the instant values of the input and output signals of the first order low pass filter cannot be performed, but the RMS values are stationary, and their ratio $V_{RMS,IN}/V_{RMS\_OUT}$ reflects the signal V_{IN} frequency. The formula used for RMS calculation is:

$$V_{\mathrm{RMS}} = \sqrt{\frac{1}{T}\int_0^T v^2(t)dt}, \tag{10}$$

where T is the signal period and $v(t)$ is the time-varying signal.

The implementation of relation Equation (10) in PSpice poses a challenge and cannot be performed directly. The time integral of the squared signal is computed by injecting a current having the value $v^2(t)$ into a 1 F capacitor. Then, the value of time integral is divided by time and the square root value is extracted. The operating principle of the capacitor used for the implementation of the RMS formula is given as:

$$I_C(t) = C\frac{dU_C(t)}{dt} => U_C(t) = \frac{1}{C}\int I_C(t)dt \tag{11}$$

The principle of RMS code implementation from relation Equation (11) is given in Figure 12.

```
G1   0 SQUARE VALUE={V(SIGNAL) * V(SIGNAL)}
C1   SQUARE 0 1
E1   RMS    0 VALUE={SQRT(V(SQUARE)/TIME)}
```

Figure 12. PSpice time integral computation principle.

The ratio of the RMS values of the input and output signals of the low pass filter is:

$$\frac{\mathrm{RMS}_{in}}{\mathrm{RMS}_{out}} = \sqrt{1 + 4\pi^2 {f_{signal}}^2 R_1^2 C_1^2} => f_{signal} = \sqrt{\frac{\frac{{\mathrm{RMS}_{in}}^2}{{\mathrm{RMS}_{out}}^2} - 1}{4\pi^2 R_1^2 C_1^2}} \tag{12}$$

We associated a PSSR value in *dB* for each frequency of interest in PSpice using the TABLE function. The PSRR values between the two frequencies of interest are interpolated. In order to obtain a smoother PSRR vs. frequency characteristic, more frequency points were chosen.

The PSRR values in *dB* from the PSpice TABLE need to be converted to numerical values as follows:

$$\mathrm{PSRR}_{numerical} = 10^{\frac{\mathrm{PSRR}_{dB}}{20}} \tag{13}$$

The final V_{PSRR} that is added to the ideal reference voltage V_{REF_IN}, and gives the output reference voltage V_{REF_OUT} (Figure 10), is computed as:

$$V_{\mathrm{PSRR}} = \frac{\Delta V_{IN}}{\mathrm{PSRR}_{numerical}} \tag{14}$$

The frequency computation, PSRR TABLE implementation, and V_{PSRR} determination in PSpice are presented in Figure 13, in which relations Equations (12)–(14) were used.

```
E2 FREQ 0 VALUE={SQRT((1-V(RMS_IN)/V(RMS_OUT))/(4*3.14**2*{RLPF}*{CLPF}))}

E3 PSRR_TABLE 0 VALUE={TABLE(V(FREQ), {FREQUENCY_1}, {DB_VALUE_1},FREQUENCY_2}, {DB_VALUE_2},
+{FREQUENCY_3}, {DB_VALUE_3}, {FREQUENCY_4}, {DB_VALUE_4}, {FREQUENCY_5}, {DB_VALUE_5}  )}

E4 VPSRR 0 VALUE={V(RIPPLE)/(10**(V(PSRR_TABLE)/20))}
```

Figure 13. PSpice frequency and V_{PSRR} computation.

4. PSRR Simulation Results

The AC analysis used in PSpice is a linear analysis. The simulator calculates the frequency response by linearizing the circuit around the bias point. All voltage and current sources that have AC values are inputs of the circuit. During the AC analysis, the only sources that have non-zero amplitudes are those using AC specifications [26]. Because our PSRR modeling method is non-linear, the PSRR was analyzed using the transient simulation.

The transient simulation test-bench, presented in Figure 14, consists of the TPS785-Q1 model with resistors R6 and R7 chosen such that the output voltage is set to 3.3 V and the load current is set to 1 A, as specified by the PSRR conditions. The load capacitor C1 is parameterized with value {CLOAD}, and the input voltage source VIN is parameterized with {FREQ}, which sets the input voltage sine frequency. The amplitude is set to 0.5 V and the offset to 5 V.

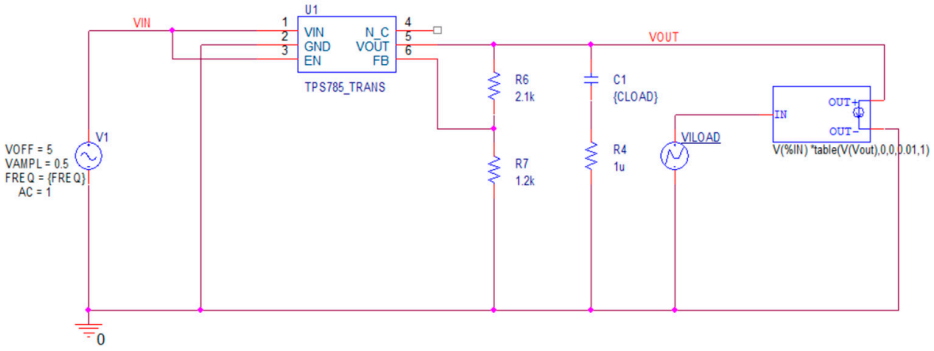

Figure 14. Transient test-bench circuit for TPS785-Q1 PSRR simulation.

For each frequency of interest, a transient simulation was performed and the peak-to-peak amplitude of the output voltage was extracted. The simulator options were set to default and the maximum time step was set to the 100th part of the input signal period. The waveforms of the input (red curve) V_{IN} and output (green curve) V_{OUT} voltages are shown in Figure 15 for a chosen frequency of 100 kHz (where the output voltage ripple is visible), and the PSRR calculations are shown in Table 1. In Table 1, we chose 20 frequency values within the range 10 Hz–10 MHz (as specified in Figure 4) in order to demonstrate the accuracy of the results while the frequency is rising.

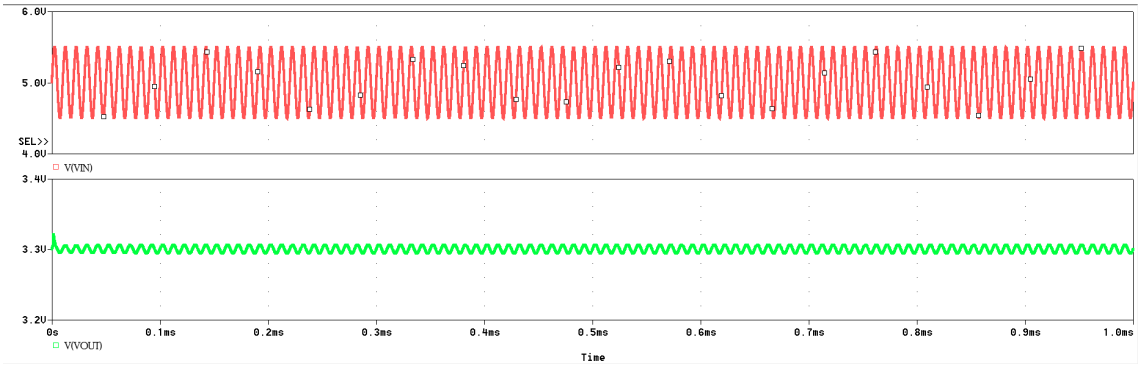

Figure 15. PSRR simulation waveforms at 100 kHz.

Table 1. Simulated new PSRR vs. frequency.

Frequency	$VOUT_{MAX}$	$VOUT_{MIN}$	PSRR
[Hz]	[V]	[V]	[dB]
10	3.2999	3.2996	70.00
20	3.2999	3.2996	70.00
40	3.2999	3.2995	68.09
100	3.3002	3.2992	59.98
200	3.3005	3.2989	55.95
500	3.3013	3.2981	49.98
1 k	3.3025	3.2969	44.99
2 k	3.3029	3.2944	41.41
5 k	3.3060	3.2934	37.99
10 k	3.3086	3.2908	35.00
50 k	3.3053	3.2941	38.99
70 k	3.3047	3.2947	39.99
100 k	3.3060	3.2934	37.99
200 k	3.3172	3.2822	29.12
300 k	3.3276	3.2719	25.08
500 k	3.3310	3.2645	23.53
1 M	3.3014	3.2555	26.75
2 M	3.2943	3.2686	31.80
4 M	3.3031	3.2918	38.95
10 M	3.2828	3.2720	39.37

Figure 16 presents the simulated new PSRR vs. frequency characteristic drawn based on Table 1, compared with the theoretical characteristic, shown in Figure 4. The simulated PSSR curve was determined only for a load capacitor of 1 µF. The reason behind this decision is that the capacitor only influences the PSRR at frequencies over 300 kHz, and lower frequencies, which are not influenced by the load capacitor value, are much more important than the higher ones.

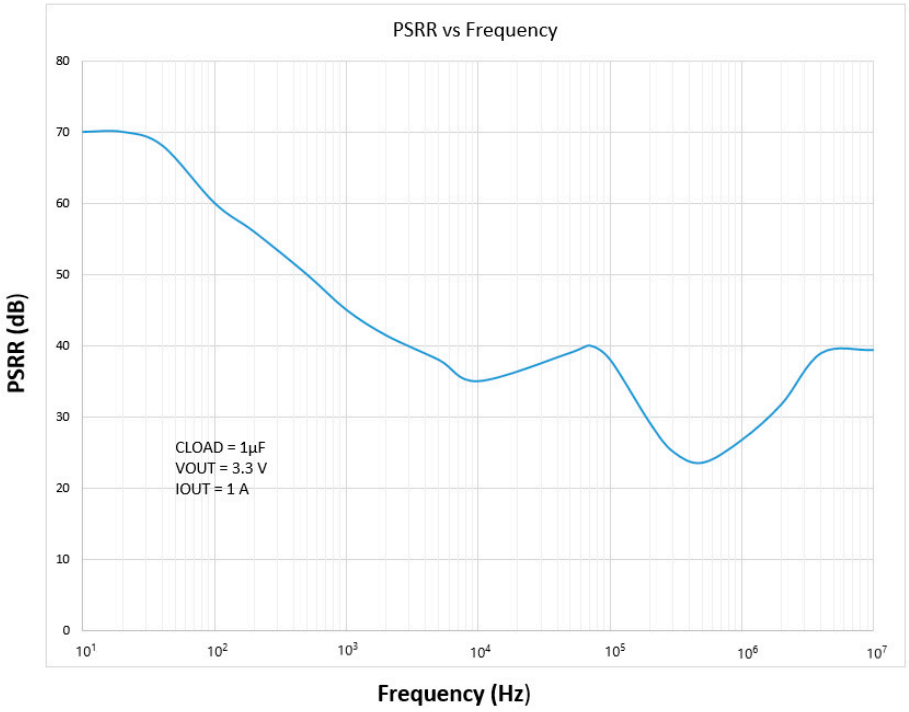

Figure 16. Simulated new PSRR characteristic of the TPS785-Q1 model.

5. Discussion and Comparison of Theoretical, Old, and New PSRR Simulations

Table 2 compares the theoretical, original model, and the newly proposed PSRR model results at various frequencies for a load capacitor of 1 µF.

Table 2. Theoretical PSRR vs. Simulated Old PSRR vs. Simulated New PSRR for a load capacitor of 1 µF.

Frequency	Theoretical PSRR	Simulated Old PSRR	Simulated New PSRR
[Hz]	[dB]	[dB]	[dB]
10	70	60	70.00
20	70	60	70.00
40	68	59	68.09
100	62	57	59.98
200	56	53	55.95
500	50	46	49.98
1 k	45	40	44.99
2 k	41	34	41.41
5 k	38	27	37.99
10 k	35	22	35.00
50 k	39	30	38.99
70 k	40	33	39.99
100 k	38	36	37.99
200 k	30	42	29.12
300 k	27	45	25.08
500 k	25	50	23.53
1 M	21	55	26.75
2 M	25	61	31.80
4 M	39	68	38.95
10 M	20	75	39.37

The results in Table 2 show that the absolute difference value between the simulated new PSRR curve and the theoretical curve until 500 kHz is 2 dB, whereas between the simulated original PSRR and theoretical PSRR there is an absolute difference of 25 dB.

The issue encountered in this work was that for frequencies above 500 kHz, the new PSRR error starts increasing, but remains within a tolerance of 5 dB until 10 MHz, when the absolute error becomes 20 dB. This happens due to the limitations of the LDO model error amplifier, as shown in Figure 17. The red curve represents the reference voltage V_{REF} of the chip and the green curve is the feedback voltage V_{FB} at an input signal frequency of 10 MHz. It can be clearly seen that the feedback voltage cannot track the reference voltage properly and this limits the model performance. In this case, the error amplifier EA in Figure 7a has to be redesigned, which is not the subject of this paper.

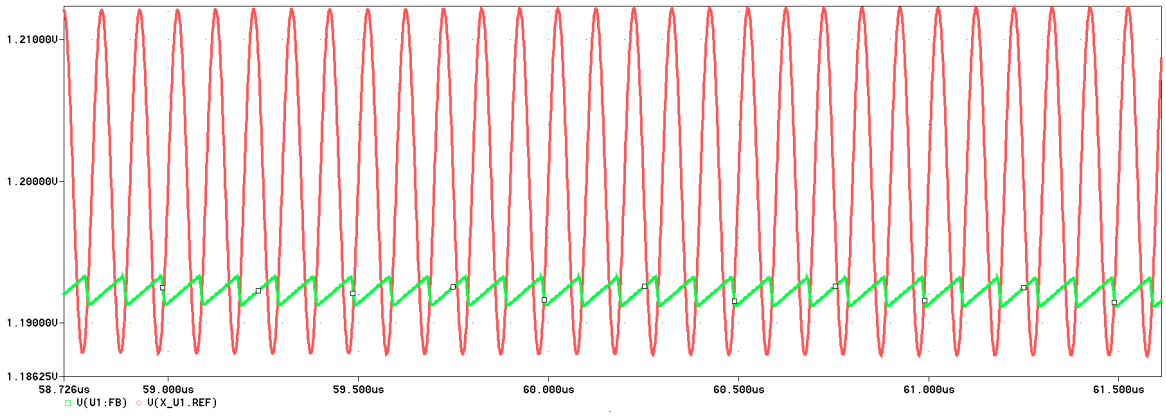

Figure 17. LDO model limitations at 10 MHz.

Table 3 shows the relative errors with respect to the theoretical curve over the frequency range of the initial PSRR method and our method.

Table 3. Original PSRR error and New PSRR error vs. Frequency.

Frequency	Theoretical PSRR	Old PSRR Error	New PSRR Error
[Hz]	[dB]	[%]	[%]
10	70	14.28	0
20	70	14.28	0
40	68	13.23	0.13
100	62	8.06	3.25
200	56	5.35	0.08
500	50	8.00	0.03
1 k	45	11.11	0.01
2 k	41	17.07	1.01
5 k	38	28.94	0.01
10 k	35	37.14	0
50 k	39	23.07	0.01
70 k	40	17.50	0.01
100 k	38	5.26	0.01
200 k	30	40.00	2.90
300 k	27	66.66	7.08
500 k	25	100.00	5.84
1 M	21	161.90	27.41
2 M	25	144.00	27.20
4 M	39	74.35	0.10
10 M	20	275.00	96.85

A graph is plotted in Figure 18 based on the results in Table 3.

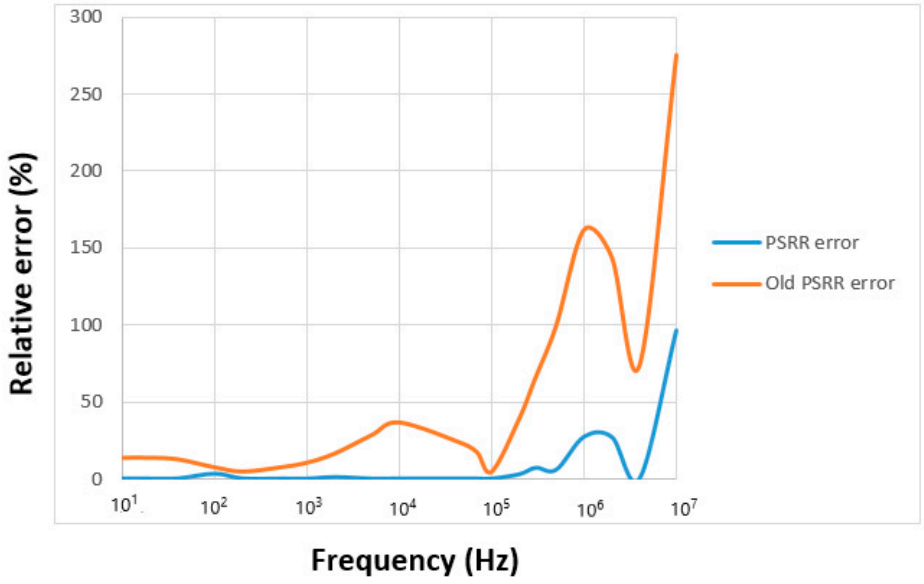

Figure 18. Original PSRR approach and new PSSR approach relative errors.

The results in Table 3 and presented graphically in Figure 18 indicate that our new model delivers high quality performance for frequencies lower than 500 kHz, resulting in a relative error of around 0% to 7%, compared with the old PSRR model given in [14,19], which has significantly higher values at any frequency point (from around 5% to 100%). Moreover, we can observe that both the old PSRR and the new PSRR errors increase significantly over 500 kHz. We found that this is due to the error amplifier EA (Figure 7a),

which must be redesigned in order to increase PSRR's performance at high frequencies; however, this is not treated in this paper.

6. Conclusions

In this paper, we proposed a new method for improving the PSSR response of automotive LDO behavioral models for frequencies below 500 kHz, which is based on mathematical relations combined with circuits' relations.

We first used an existing commercially available automotive LDO model (TPS785-Q1 from Texas Instruments), which is available on Texas Instruments' official website [19]. We began by simulating the original model and plotted its PSRR characteristic, then we built a new PSRR model and integrated it into the LDO model, from which we eliminated the previous PSRR approach. The proposed method is not linear, so the PSRR characteristic was plotted using transient simulations. During the simulation phase, we noticed that the PSRR characteristic behaves extremely well at frequencies below 500 kHz, having an error lower than 7%, whereas for frequencies over 500 kHz up to 10 MHz, we concluded that the inaccurate behavior of the error amplifier greatly influences the PSRR response.

The implementation achieved in this paper proves extremely important in the automotive domain, in which simulations are usually chosen over real testing. Since the LDO is one of the most used power supply circuits in cars, this totally justifies the need for accurate LDO models. One of the most critical requirements of the LDO is the PSRR, which has not been explicitly addressed until now in circuit modeling. Most of the exiting commercially available LDO models show basic behavior and do not model the PSRR characteristic. Newer LDO models also include very simple PSRR functionality, but this is inaccurate and does not model the real characteristic properly over the functioning frequency range. Our work provides an optimized PSRR modeling method that models the real PSRR characteristic accurately for frequencies below 500 kHz, thus filling an important gap in the field. In order to accurately model the entire frequency range, the error amplifier also needs to exhibit accurate behavior, and this error amplifier redesign represents a future research direction.

Other future research directions consist of the enhancement of the current PSRR approach to also support variation with the load capacitor. The ripple of the output current needs to be measured using the same methodology as for the output voltage presented in this paper; the current ripple frequency using the RMS integration should then be determined, and another variation added to the existing one.

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