Article

Parasitic Coupling in 3D Sequential Integration: The Example of a Two-Layer 3D Pixel [†]

Petros Sideris [1,2] **, Arnaud Peizerat** [2]**, Perrine Batude** [2]**, Gilles Sicard** [2] **and Christoforos Theodorou** [1,]*

[1] University Grenoble Alpes, Univ. Savoie Mont Blanc, Centre National de la Recherche Scientifique (CNRS), Grenoble INstitut Polytechnique (Grenoble INP), Institut de Microélectronique Electromagnétisme Photonique-LAboratoire d'Hyperfréquences et de Caractérisation (IMEP—LAHC), 38000 Grenoble, France; psiderisd@gmail.com

[2] Commissariat à l'Energie Atomique et aux Energies Alternatives—Laboratoire d'Electronique des Technologies de l'Information (CEA—LETI), University Grenoble Alpes, 38054 Grenoble, France; arnaud.peizerat@cea.fr (A.P.); perrine.batude@cea.fr (P.B.); gilles.sicard@cea.fr (G.S.)

[*] Correspondence: christoforos.theodorou@grenoble-inp.fr

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Abstract: In this paper, we present a thorough analysis of parasitic coupling effects between different electrodes for a 3D Sequential Integration circuit example comprising stacked devices. More specifically, this study is performed for a Back-Side Illuminated, 4T–APS, 3D Sequential Integration pixel with both its photodiode and Transfer Gate at the bottom tier and the other parts of the circuit on the top tier. The effects of voltage bias and 3D inter-tier contacts are studied by using TCAD simulations. Coupling-induced electrical parameter variations are compared against variations due to temperature change, revealing that these two effects can cause similar levels of readout error for the top-tier readout circuit. On the bright side, we also demonstrate that in the case of a rolling shutter pixel readout, the coupling effect becomes nearly negligible. Therefore, we estimate that the presence of an inter-tier ground plane, normally used for electrical isolation, is not strictly mandatory for Monolithic 3D pixels.

Keywords: image sensors; 3D pixels; 3D sequential integration; 3DSI; monolithic 3D; M3D; coupling; parasitic capacitances

1. Introduction

User-interactive applications are continuously emerging and driving the electronics industry towards the adoption of heterogeneous technologies in the sense that the analog sensing parts are integrated together with digital processing parts. The More-than-Moore technology development direction is a key enabler for such heterogeneous integrations, as it involves a wide variety of people–environment interaction applications [1].

An important driving application within the More-than-Moore scheme is the CMOS Image Sensor (CIS), because it is a circuit that requires the heterogeneous integration of different system parts: a photon-to-electron converter (photodiode) functions as the sensing interface in the pixel array and the readout part consists of an analog circuit that transmits information from the pixel to a digital circuit for processing. Moreover, CIS is an ideal candidate for studying coupling effects in 3D integration technologies, as it is highly sensitive to noise (dynamic) and mismatch (static) variations, while simultaneously being an extremely attractive application of 3D Integration for the semiconductor industry [2]. In particular, 3D CIS allows the development of smarter, more advanced sensors by co-integrating different blocks (Analog, Digital and RF) in multiple stacked tiers. By using the 3D stack integration process, the CMOS processing part can be stacked on top of the pixel, enabling the use of more advanced technology nodes for the processing circuit.

Although, until today, 3D stacking is predominantly used for 3D CIS, constraints concerning the alignment capabilities cannot allow more aggressive pixel miniaturization, which is required for future CIS generations [3,4]. However, in the case of 3D Sequential Integration (3DSI) [5,6], where one tier is processed on top of the other instead of being stacked, this drawback can be overcome, achieving pixel partitioning with state-of-the-art pixel pitch. In addition, 3DSI offers 3D contacts of outstanding high-density between tiers (up to 10^8 3D via/mm^2), enabling partitioning with high connectivity and low latency. Therefore 3DSI allows the co-integration of dense logic and memory layers but also heterogeneous components such as MEMS/NEMS for the compact coexistence of sensing and computing [7].

Despite the fact that the 3DSI technology approach offers great opportunities for the domain of CSI, it is also prone to many challenges, such as the limited Thermal Budget (TB) for the fabrication of the top-tier devices. To date, Low Temperature (LT) devices have been successfully fabricated and optimized for both low-voltage (LV) [5] and high-voltage (HV) [8] applications. Using such LT devices, Coudrain et al. [9] have investigated the feasibility of a 3DSI Back-Side Illuminated (BSI) CIS with miniaturized pixels, achieving a photodiode area increase by 44% for a 1.4 µm pitch. However, the other major challenge, concerning the impact of the inter-tier parasitic coupling on a 3DSI CIS performance, has not been examined in depth.

In this work, we present a thorough analysis of the possible coupling effects in the realization of a BSI 4–Transistor (4T) pixel with its diode and Transfer Gate (TG) on the bottom tier and the rest of its circuitry on the top tier of a 3DSI process, as an example of parasitic coupling analysis in a 3DSI circuit. In Section 2, the general principles and operation scheme of a CMOS imager are presented, including a presentation of the basic CIS architectures and the most critical performance metrics. In Section 3, the inter-tier coupling effects are analyzed, first at a single device level and then at the pixel level.

2. CMOS Imager: Architectures and Integration

2.1. CIS Standard Architectures and Operation

The most basic pixel architecture, called Passive Pixel Sensor (PPS) [10], contains passive pixels with no amplification, with only a photodiode for light detection and transistor switch for row selection, as shown in Figure 1a. Due to the lack of amplification or more sophisticated circuit, this architecture suffers from poor image quality, high KTC noise level and slow readout [11,12].

A major improvement to PPS architecture is the so-called Active Pixel Sensor (APS) [13], which incorporates an in-pixel amplifier for every pixel. Therefore, each pixel is composed of a photodiode (PD), a reset transistor (RST) and a source-follower (SF) amplifier, as demonstrated in Figure 1b. This architecture has reduced power consumption, random access and high-speed readout, thanks to the fact that the readout output is a voltage instead of charge transfer. On the downside, having additional transistors per pixel degrades the Fill-Factor. Finally, the issue of the kTC noise generated by the photodiode reset is not resolved.

In order to address the high reset noise issue, a Pinned Photodiode (PPD) pixel was introduced [14], resulting in the architecture shown in Figure 1c, which is the same as the APS one, but with the PPD connected to the readout circuit. This is achieved by an extra Transfer Gate (TX) and a Sense Node (SN). This 4T–APS architecture further allows the implementation of a fast Correlated Double Sampling (CDS) technique at the column level. Finally, thanks to the superior noise performance of the PPD [3], 4T–APS is currently the preferred architecture for CIS pixels in a variety of applications such as mobile imaging, digital still and video cameras, as well as surveillance cameras.

A schematic representation of the voltage output for a 3T–APS pixel is presented in Figure 2, showing how the operation sequence consists of three stages:

1. Reset (RST ON): The photodiode voltage is set to a reference voltage V_{ref};

2. Exposure (RST OFF): The detected photons decrease the reverse photodiode voltage during the integration time (t_{int});
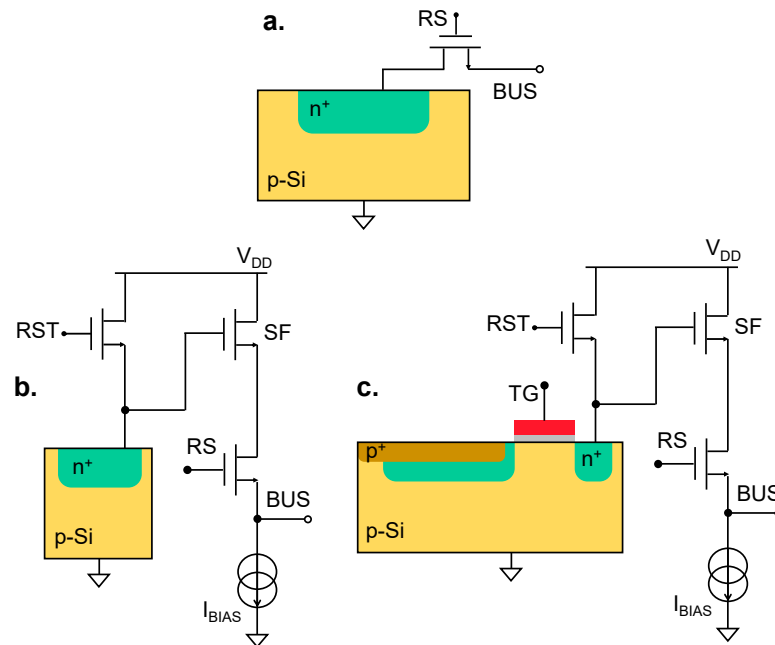3. Readout (RS and SF ON): The output voltage level is sampled and further processed at the column level.

Figure 1. (**a**) Passive CMOS pixel based on a single in-pixel transistor, (**b**) active CMOS pixel based on an in-pixel amplifier and (**c**) active CMOS pixel based on an in-pixel amplifier in combination with a pinned photodiode.
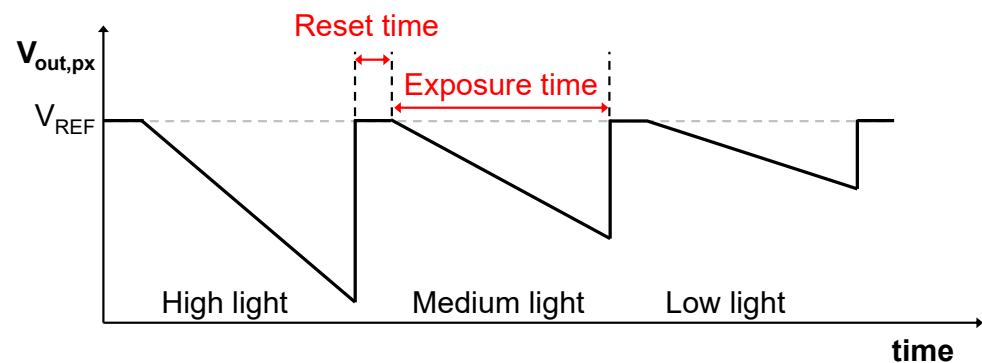

Figure 2. Operation principle of a 3T–APS pixel.

2.2. The Back-Side Illumination Integration Scheme

In the case of Front-Side Illumination, the optical path includes the total Back End Of Line (BEOL) thickness, inducing losses and crosstalk between pixels, because of the reflection on the metal lines. By flipping the sensor so that light drops directly on the photodiode without passing through the pixel's BEOL, the BSI integration scheme can be achieved. This is illustrated schematically in Figure 3, along with the example of stacked tiers of a 3D integration. The BSI scheme has become the preference for high-end consumer applications, dictated by the mobile phone market which requires continuously higher resolution for the same sensor size [3,4]. Currently, more than half of the mobile phone market utilize BSI integration [15]. Since 2010, the industrial trend is to combine BSI and 3D stacking/integration to reach ultimate performance, while at the same time maintaining a small pixel size.
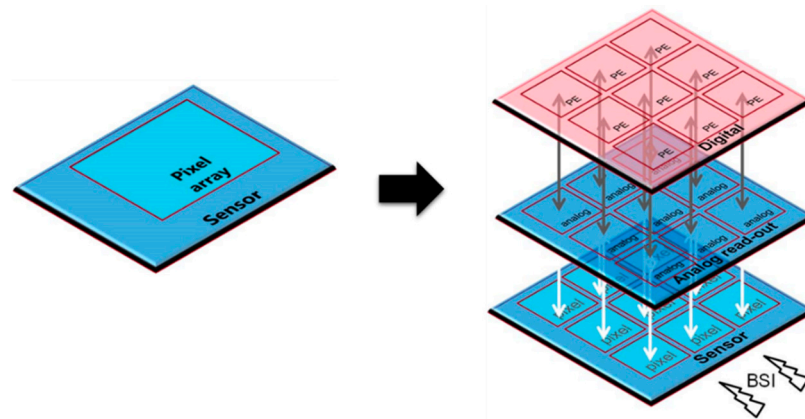
Figure 3. Realization of a CIS with planar (**left**) and three-dimensional partitioning (**right**).

2.3. CIS Performance Metrics

There are a series of important performance metrics for a CIS that are worth mentioning, before presenting our simulation study, such as the Signal-to-Noise Ratio (SNR), the Dynamic Range (DR) and the Conversion Gain (CG) amongst others.

SNR is defined as the ratio of the useful signal amplitude to the amplitude of undesirable noise and is a good indicator of image quality. Therefore it has to be maximized either by increasing the sensitivity and CG or by decreasing the noise floor [11,16]. SNR is reduced in the case of a smaller pixel area, which means less absorbed photons for the same duration. However, the reduction in pixel size provides higher spatial resolution, at a lower light sensitivity as a trade-off. Minimizing the pixel size will also affect the Full Well Capacity (FWC) and, thus, the DR (these parameters will be below).

The Fill Factor (FF) is another parameter that is affected by pixel scaling [11,16]. It is defined as the percentage of the photosensitive area with regards to the total pixel area. Thus, it expresses what portion of the total pixel area is utilized for photon collection. A high FF value means higher sensitivity; thus, it ought to be maximized, for example, by downscaling pixel transistors or by adding microlenses to guide the light towards the photodiode area.

Regarding the sensitivity of a sensor with linear response, as is the case of 3T/4T–APS, it is equal to the slope of the transfer function (in V/lux.s or e^-/lux.s). It corresponds to the change in output potential for a given light intensity and integration time. It is highly dependent on the Quantum efficiency (QE) of the sensor [11], a quantity that shows how efficiently the photons are collected and converted to electrons. One method to maximize it is to use anti-reflecting coating or optimize the stack between the sensor surface and the photodiode, or to use BSI, in order to avoid reflections at the interfaces.

The DR of a CIS is defined as the range of light intensity that can be measured with no distortion by the sensor [11,16]. It can be calculated as $DR = 20\log(S_{max}/S_{min})$, where S_{max} is the highest detectable signal and S_{min} the lowest one (essentially the noise floor). On the other hand, S_{max} is limited by the Full Well Capacity and pixel saturation.

An important parameter for our study is CG, which is defined as $CG = \Delta V_{out}/N_e$, where ΔV_{out} is the pixel output ($V_{out,int} - V_{out,ref}$) when the number of electrons is equal to N_e in a single packet [11,16]. N_e depends on photon flux and QE. It is measured in V/e^- and it characterizes the charge-to-voltage conversion; thus, a high CG results in higher sensitivity, especially at low light. Another method to express CG is through (X), taking into account SN capacitance, C_{SN}, and any additional parasitic capacitance, C_P.

$$CG = \frac{q}{C_{SN} + C_P} \tag{1}$$

Finally, the amount of charge that can be detected without reaching saturation is expressed through the FWC metric, which is measured in number of charges and determines

the sensor's DR [11,16]. If we neglect the noise, FWC can be roughly approximated by FWC = $qC_{PD}V_{PD}$, where V_{PD} is the applied voltage across the photodiode, and C_{PD} is the photodiode capacitance. By increasing C_{PD}, therefore, one can directly increase the sensor's FWC. However, in that case, CG would be decreased due to the increased capacitance. This in turn may result in a range decrease at the low intensity end, and this contradiction is actually the well-known DR/sensitivity tradeoff.

3. Parasitic Capacitance Coupling in a Two-Layer 3DSI Pixel

As already mentioned in the Introduction, pixel partitioning in two layers of a 3DSI process is a very promising technique to boost an imager's performance by increasing the photodiode area ratio, and it has dedicated layers for each type of circuit (read-out, digital etc.). Nevertheless, positioning transistors right above the photodiode's transfer gate at a submicrometre distance introduces a high risk of parasitic capacitance coupling, which will be investigated in this Section. At first, in order to be certain if there can be a significant coupling-induced threshold voltage shift and, if so, to quantify it, we performed simulations at a device level, without taking into account the particularities of a pixel's circuit operation and chronogram. Afterwards, in Section 3.2, we present the simulation results we obtained at a circuit level, examining in which cases the parasitic coupling can affect or not the pixel's output precision.

3.1. Investigation at Device Level
3.1.1. Simulated Structure Details

In order to carry out our study, the simulation structure depicted in Figure 4 was considered. As shown in the cross-section of Figure 4a, our setup has its pixels sequentially integrated in such a manner that PPD and TG are placed at the bottom layer and the rest of the readout circuitry is placed right above them, with an Inter-Layer Dielectric (ILD) of 200 nm thickness separating them. TG can toggle between 0 and V_{DD}, enabling photo-generated electrons to be transferred from the photodiode area to SN and then to the drain of RST and the gate of the SF via a 3D contact.
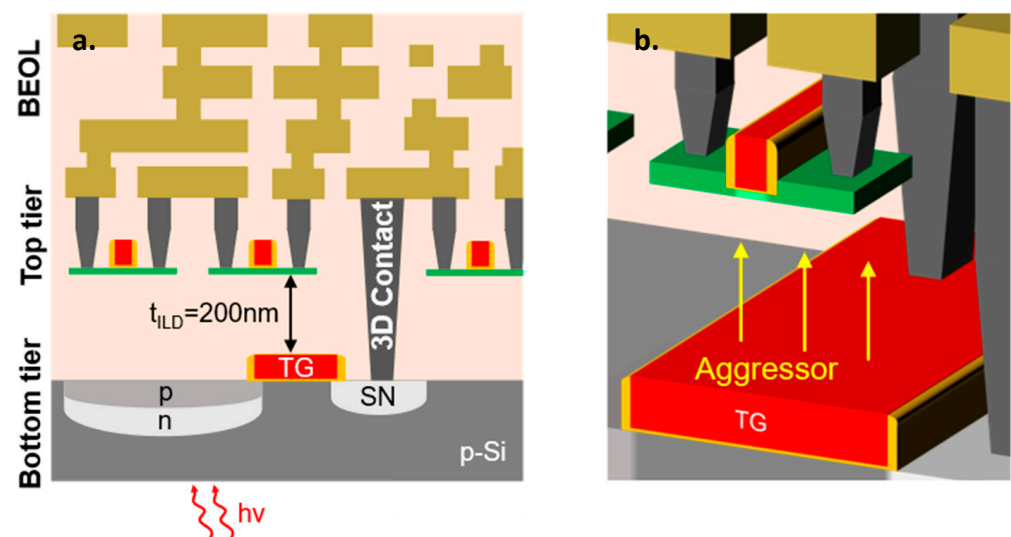

Figure 4. (**a**) Cross-section of 4T pixel, partitioned in 3DSI. (**b**) In the most critical case, the top device is placed right above the TG electrode carrying a voltage that can go up to V_{DD} = 2.5 V.

In order to extend the voltage swing of top-tier devices, analog devices with power supply of 2.5 V were considered for the top layer. In addition, the most critical condition of inter-tier coupling has been chosen by placing the TG electrode right under each one of the top layer devices, as shown in Figure 4b.

3.1.2. Impact of Inter-Tier Coupling on Electrical Parameters

In order to assess whether inter-tier static coupling can be detrimental to the functionality of the 3DSI pixel, we investigated the impact of the capacitive coupling of the TG placed at the bottom tier on each top device performance. By varying the TG gate voltage bias within its normal operation limits (0–2.5 V), we observe a shift of the I_D–V_G characteristics for the top devices, as shown in Figure 5a. This behavior can be attributed to the fact that the top devices are actually asymmetrical SOI structures, where ILD plays the role of the Buried Oxide (BOX). It is well-known in SOI devices [17] that this effect is nonlinear, with its maximum in weak inversion and equal to a constant value when the device enters strong inversion.
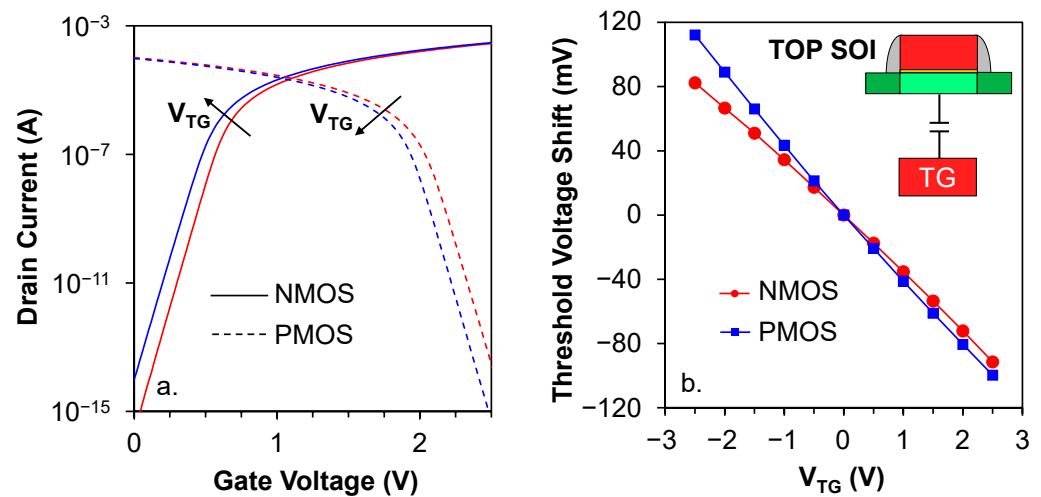

Figure 5. (**a**) Impact of TG coupling ($V_{TG} = 0$ (red) -2.5 V (blue)) on the input characteristics for NMOS and PMOS devices. (**b**) Extracted threshold voltage shift versus TG voltage bias (-2.5 V to 2.5 V with 0.5 V step).

Figure 5b shows the extracted threshold voltage shift (ΔV_{TH}) versus V_{TG} (from -2.5 V to $+2.5$ V) and a nearly linear relation was obtained, which allowed the extraction of the back-bias efficiency γ for the top devices (35 mV/V for NMOS and 42 mV/V for PMOS). V_{TH} was extracted using the constant current method [18] for each I_D–V_G curve.

In order to evaluate the strength of TG-induced static coupling on the top device performance, we benchmarked it against a temperature variation of 100 °C, which is a typical range in consumer electronics. Contrary to capacitive coupling, the effect of temperature varies depending on the gate voltage V_G. Indeed, our simulations (Figure 6) show that when proceeding from 253 K to 353 K (-20 °C to 80 °C), an increase in the leakage current and a decrease in ON current were observed, whereas at a specific gate voltage around V_{TH}, the drain current remains unaffected by T. This effect is well known in the literature and is due to the canceling out between the rise in carrier concentration with temperature for low V_G and the decrease in carrier mobility at high V_G [19]. The voltage at which this happens is characterized as the Zero Temperature Coefficient (ZTC) point [20].

Eventually, the I_D–V_G shift resulting from both coupling and temperature variation can be translated in an alteration of the top device electrical parameters, namely the V_{TH}, the leakage current (I_{OFF}) and the saturation current (I_{ON}). The comparison of the extracted parameters for the two effects is shown in Figures 7 and 8. The results show that they are approximately in the same order of magnitude while the limited ΔV_{TH} due to the temperature variation is attributed to the ZTC point near V_{TH}. Moreover, as observed in Figure 7, I_{OFF} is significantly shifted with V_{TG}, which can be detrimental for memory blocks comprising switch transistors, placed at the top-tier above TG.
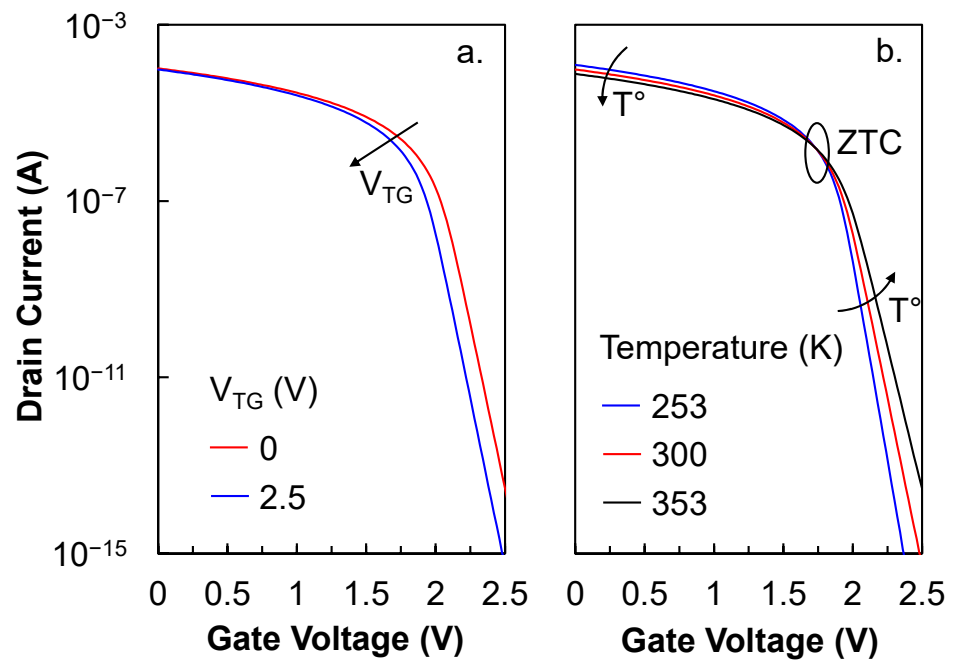
Figure 6. Impact of coupling (**a**) and temperature variation (**b**) on the top-tier SOI input characteristics.
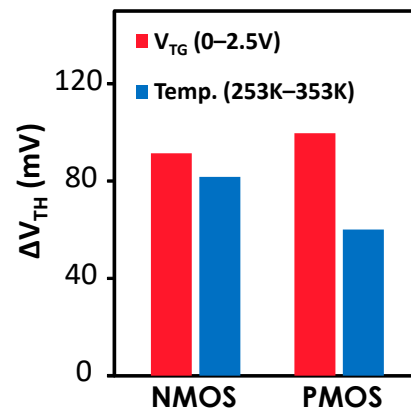

Figure 7. Comparison of the V_{TH} variation of the top-tier NMOS and PMOS due to TG coupling or due to a 100 K temperature increment.
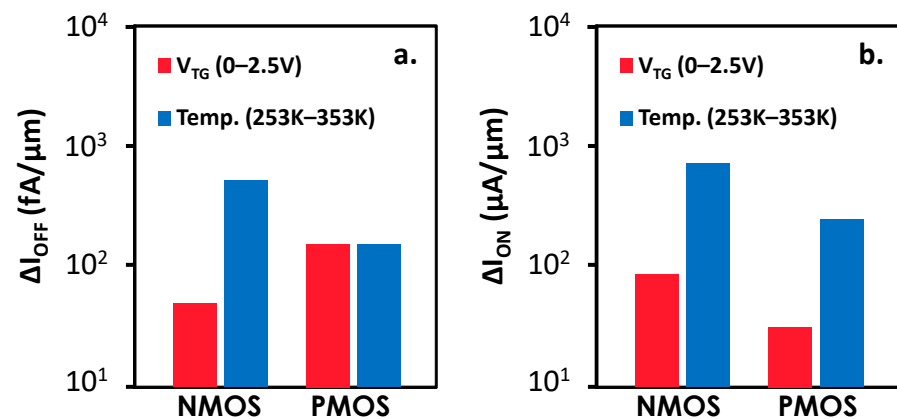

Figure 8. Comparison of the I_{OFF} (**a**) and I_{ON} (**b**) variation of the top-tier NMOS and PMOS due to TG coupling or due to a 100 K temperature increment.

3.2. Investigation at Pixel Level

3.2.1. Pixel Topology and Chronogram

In order to carry out our analysis at the pixel level, the 4T–APS topology was selected, which consisted of an NMOS–TG and the RST, SF and RS in a PMOS circuit configuration, as illustrated in Figure 9a. As shown from the chronogram of the 4T–APS pixel readout operation presented in Figure 9b, during the readout cycle, TG was switched ON following the SN reset, allowing the diffusion of photo-generated electrons, which in turn cause a voltage drop at the input of the SF. Due to the rough unity gain of SF, the voltage drop is transferred nearly at the same level at its output.
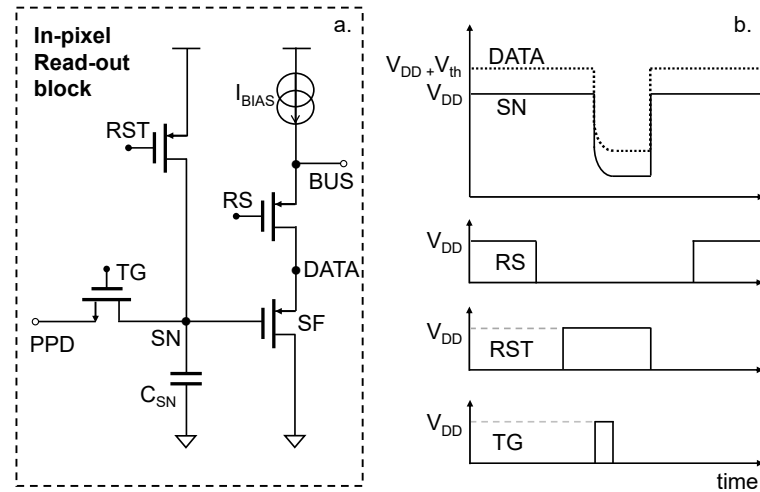

Figure 9. (**a**) 4T pixel readout circuit. (**b**) chronogram of a readout cycle.

The efficiency of the aforementioned operation is characterized by the CG in $\mu V/e^-$, given by the following [21]:

$$CG = \frac{q G_{SF}}{C_{SN} + C_{GD} + (1 - G_{SF})C_{GS}},$$
(2)

where q is the elementary charge, G_{SF} is the SF gain, C_{SN} is the sum of parasitic capacitances at the SN node and C_{GS} and C_{GD} are the gate to source and gate to drain capacitances of SF.

The gain G_{SF} of the SF, on the other hand, is expressed as follows:

$$G_{SF} = \frac{g_{m,SF}}{g_{ms,SF}} = \frac{1}{n},$$
(3)

where $g_{m,SF}$ and $g_{ms,SF}$ are the gate and source transconductances, respectively, and n is the body factor of SF. The gain is approximately equal to unity in the case where the BG of SF can be tied to the source or else it is process-dependent and is given by $n = 1 + \gamma$, where γ is the back-bias efficiency. With the increase in ILD thickness, n approaches unity. For the γ values extracted in the previous section, we have evaluated the gain G_{SF} of the NMOS and PMOS devices as 0.97 and 0.96, respectively.

The cutoff frequency (f_c) of the SF is given by the following [21]:

$$f_c = \frac{g_{m,SF}}{2\pi \cdot C_{out,SF} \cdot G_{SF} \cdot (C_{SN} + C_{GD} + C_{GS})},$$
(4)

where $C_{out,SF}$ is the capacitance observed at the source of the SF that is the column-level capacitance if there are no other stages in between.

3.2.2. Impact of TG Coupling on Pixel Electrical Parameters

In order to evaluate 3DSI impacts on the two critical parameters CG and f_c analyzed above, parasitic extraction was performed concerning a single- and a two-layer implementation of our pixel, as illustrated in Figure 10, and the results along with CG values are presented in Table 1. As observed, the sums of C_{SN} and C_{GD}, as well as C_{GS}, slightly increased by 48aF and 44aF, respectively, which may be attributed to the proximity of the top tier.
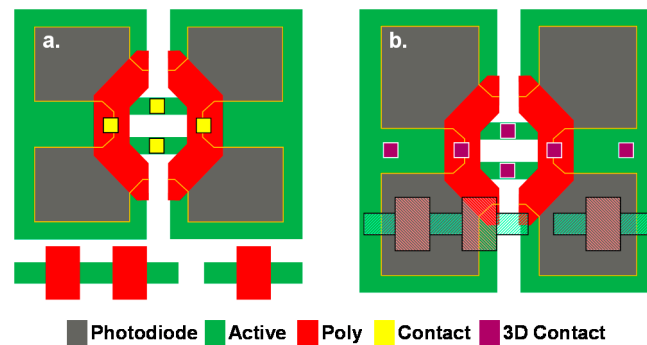

■ Photodiode ■ Active ■ Poly ■ Contact ■ 3D Contact

Figure 10. Shared pixels at photodiode layer: 2D (**a**) vs. 3D (**b**). Photodiode area (in grey) increased by 44% when the three readout transistors were placed at the top tier.

Table 1. Two-dimensional vs. three-dimensional parasitic capacitances and CG.

	$C_{SN} + C_{GD}$ (fF)	C_{GS} (fF)	$C_{out,SF}$ (pF)	CG (μV/e$^-$)
2D	4.432	1.093	2	34.319
3D	4.48	1.137	2	33.942

Furthermore, the column-level capacitance reveals an even smaller increase in 10aF, resulting in a minor difference in the conversion gain (ΔCG = 0.377 μV/e$^-$) and the AC response of the two-layer pixel (Δf_c = 0.244 Hz) compared to the single-layer one. The low 3DSI impact on the CG also suggests that noise performance will not be degraded.

The diagram of Figure 11 shows the output voltage of SF versus the number of photogenerated electrons at SN, where it is apparent that there is a constant vertical shift of the response without significant change in its slope (CG remains the same) while varying TG bias. The former can be considered as an offset that can be easily adjusted during the readout process.
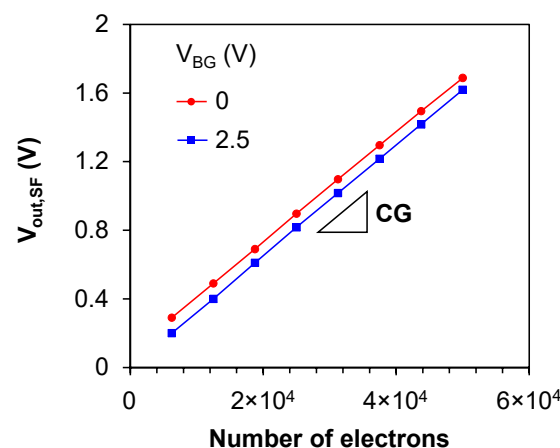

Figure 11. Output voltage of the in-pixel SF transistor versus the number of photo generated electrons at SN for the voltage bias limits of the bottom tier TG (0 V–2.5 V). The slope provides that CG was not altered with TG coupling.

Concerning the rest of pixel performance metrics, they are either related to the photodiode technology and size (similarly to FWC and FF) and, thus, are not affected by 3DSI layering, or directly related to the CG, such as the SNR and DR, which was found almost unchanged by parasitic coupling.

Continuing our analysis, in order to estimate the impact of the inter-tier coupling on the transient response of the top readout circuit, the two scenarios of Figure 12 were employed. The first is considered when SF is placed above a TG of the same pixel (Figure 12a). In that case, charge transfer occurs right at the time in which TG is enabled, as shown in the pixel readout cycle. Thus, sampling processes performed right before and after the charge transfer cannot result in an error.
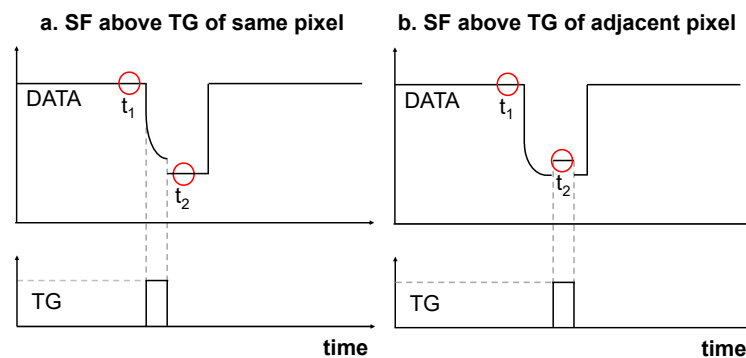

Figure 12. (**a**) For SF above a TG of the same pixel, TG switches ON during the transfer of e^- from PPD to the SN. Sampling is, thus, performed at t_1 and t_2 without readout errors. (**b**) In the scenario of an SF placed above a TG of an adjacent pixel, sampling can contain erroneous value due to TG coupling.

On the contrary, our second scenario considers an SF placed above the TG of an adjacent pixel (Figure 12b). In this case, TG is not synchronized with the pixel readout; hence, sampling can contain erroneous information. This sampling error $\Delta V_{out,SF}$ has been extracted versus the number of the photogenerated electrons at the SN and for various bias currents of the SF, with the results shown in Figure 13a. In order to evaluate the strength of this error, a comparison was made with the readout error resulting in temperature variations (253 K–353 K), which is presented in Figure 13b. It is evident that the coupling-induced readout error is significant compared to the temperature-induced one, especially for low light conditions and low bias current.
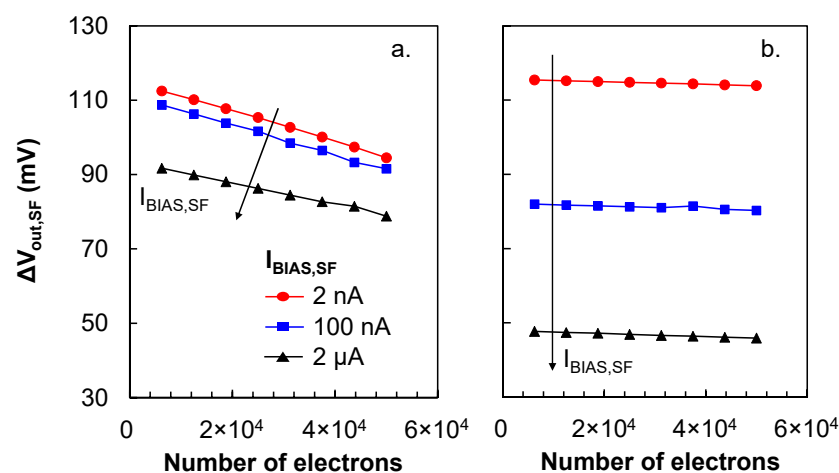

Figure 13. Readout error of the in-pixel SF transistor versus the number of photo generated electrons at SN resulting from (**a**) SF–TG coupling of Figure 7b and (**b**) sensor temperature variations.

3.2.3. Inter-Tier Ground Plane Necessity

Recent studies [22,23] have demonstrated efficient decoupling solutions between sensitive tiers in 3DSI via the process integration of a conductive layer, i.e., an inter-tier Ground Plane (GP).

Depending on each application's sensitivity and functionality, an inter-tier Ground Plane integration must be considered, taking severely into account process complexity. Nevertheless, in cases where an effective isolation between tiers in 3DSI is required, studies show that the integration of an inter-tier GP made of polysilicon can offer a reduction in vertical static coupling by five orders of magnitude [23].

Concerning the example of the two-layer 3DSI pixel studied in this work, in a typical rolling readout operation, sequential pixel activation implies that there is no probability for a readout error due to TG coupling. Consequently, TG will be enabled outside the readout cycle of this pixel and, thus, does not interfere. Furthermore, the Correlated Double Sampling (CDS) stage that exists commonly after the readout circuit eliminates possible readout errors. Therefore, the direct stacking of the readout tier upon the photodiode area is safe without the necessity for electrical isolation in a 3DSI CIS. However, an inter-tier GP is mandatory in cases where sensitive blocks are considered to be placed above the photodiode area, such as in-pixel frame memory for which the leakage current is a critical parameter.

4. Conclusions

To summarize, we have presented an investigation of coupling-induced effects in a 3DSI PMOS pixel with the aid of TCAD simulations. Our results show that coupling from TG can cause an electrical parameter variation as important as the one induced by a 100 degrees temperature variation. For switch transistors, where the leakage is a critical parameter, this could be a very limiting effect. However, for the in-pixel SF transistor, we demonstrated that the impact of inter-tier electrical coupling on the CG and the AC performance is negligible. Concerning the rest of the indicators presented in Section 2.3, none of them should be affected (especially QE and FWC since they only depend on the photodiode technology). Hence, in addition to the very slight increase in CG, pixel performance should be maintained.

We have further shown that SF–TG coupling may cause a readout error if SF is placed above the TG of a nearby pixel, i.e., in the case that it is not synchronized with the pixel readout. This is not necessarily a limitation for the CIS performance, because if the readout is performed following the rolling shutter scheme, pixel activation is sequential. Therefore, despite strong electrical coupling and high threshold voltage shifts (~100 mV) for top-tier devices, we demonstrated that a sequentially integrated 3D CIS can have an inherent immunity to inter-tier coupling, with zero readout errors.

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