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# A Design of Wide-Range and Low Phase Noise Linear Transconductance VCO with 193.76 dBc/Hz FoM<sub>T</sub> for mm-Wave 5G Transceivers

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**Abstract:** This paper presents a wide-range and low phase noise mm-Wave Voltage Controlled Oscillator (VCO) based on the transconductance linearization technique. The proposed technique eliminates the deep triode region of the active part of the VCO, and lowers the noise introduced by the  $g_m$ -cell. The switch sizes inside the switched capacitor bank of the VCO are optimized to minimize the resistance of the switches while keeping the wide tuning range. A new layout technique shortens the routing of the VCO outputs, and lowers the parasitic inductance and resistance of the VCO routing. The presented method prevents the reduction of the quality factor of the tank due to the long routing. The proposed VCO achieves a discrete frequency tuning range, of 14 GHz to 18 GHz, through a linear coarse and middle switched capacitor array, and offers superior phase noise performance compared to recent state-of-the-art VCO architectures. The design is implemented in a 45 nm CMOS process and occupies a layout area (including output buffers) of 0.14 mm<sup>2</sup>. The power consumption of the VCO achieves the phase noise performances of -87.2 dBc/Hz and -113 dBc/Hz, at 100 kHz and 1 MHz offset frequencies from the carrier frequency of 14 GHz, respectively. In an 18 GHz carrier frequency, the results are -87.4 dBc/Hz and -110 dBc/Hz, accordingly.

Keywords: linearized transconductance; VCO; low phase noise; wide-range; mm-Wave; 5G

## 1. Introduction

Nowadays, the frequency band of fourth Generation wireless systems (4G) is almost saturated. As shown in Figure 1, the fifth Generation of wireless systems (5G) offers a high data-rate communication, and the operating frequency has been extended to the mm-Wave band, due to its large bandwidth. Therefore, the design of mm-Wave integrated circuits has become popular in the last decade.



Figure 1. Frequency spectrum of the 5G.

Phase-Locked Loops (PLL) and frequency multipliers are widely used for the generation of a high-frequency clock from a low-frequency clock, to ensure the synchronized operation of different

blocks [1]. Alternatively, in a Radio Frequency (RF) and mm-Wave transceiver [2], PLL provides the local oscillator signals (LO) for the up- and down-conversion of the RF signals.

Figure 2 shows the well-known top block diagram of an analog PLL. As an essential building block of an analog PLL inside the transceiver architecture, a wide tuning range and low phase noise Voltage Controlled Oscillator (VCO), operating at a higher frequency, is highly demanded. The phase noise of the VCO results in leakage of power into adjacent channels, as well as interference, and also enhances the bit error rate in digital communication. On the other hand, a low phase noise design cannot satisfy the error vector magnitude (EVM). Therefore, a wide tuning range with low phase noise is a trending demand of such applications. Recently, to achieve a wide range and low phase noise at the same time, several techniques, such as capacitive and inductive tunings, have been reported. By using a combination of the switched capacitor bank for coarse tuning and the Metal Oxide Semiconductor (MOS) varactor for fine-tuning, a wide tuning range can be obtained [3,4]. However, in the mm-Wave frequency band, due to the capacitor and varactor, the quality factor of the Inductor and Capacitor (LC) tank decreases.



Figure 2. Top block diagram of an analog Phase-Locked Loops (PLL).

Another work [5] employs the inductive tuning technique and uses switches at different locations in the secondary coil to increase the number of sub-bands and the resulting wide tuning range. A large number of switches on the coil path introduces more parasitic capacitance, and the parasitic capacitance of switches highly affects the overall performance.

The work proposed in [6] utilizes a topology based on triple-coupled inductors, which are used to couple three pairs of varactors and compensates for the tuning nonlinearities of the LC tank, while achieving a tuning range of 15.8%, with the center frequency of 20.85 GHz. Simulation and measurement results show the phase noise performance has not been improved sufficiently. In contrast, the design of a wide-range and low phase noise VCO would be difficult, considering the trade-offs between the tuning range, phase noise and power consumption. On the other hand, the design process at higher frequencies becomes more complicated when the layout parasitic effects come into play.

In this brief, a wide tuning range and low phase noise VCO is proposed. Since in a CMOS VCO the phase noise is limited by the oscillation amplitude and device noise, the transconductance linearization technique is employed to provide sufficient signal swing and low device noise. Coarse and middle switched capacitor arrays are provided to cover the whole frequency range, of 14 GHz to 18 GHz, while the varactor offers continuous fine-tuning. The switch sizes inside the switch capacitor array are optimized to lower the introduced flicker and channel noise, while keeping the frequency range wide. A new layout technique is employed to shrink the VCO output routing and resistance, which prevents the reduction of the quality factor of the Inductor and Capacitor (LC) tank.

The rest of this paper is organized as follows: Section 2 describes VCO implementation, with the transconductance linearization technique and capacitive tuning method. Post-layout simulation results are presented in Section 3. The conclusion of the paper is summarized in Section 4.

#### 2. VCO Implementation with Linearized Transconductance and Capacitive Tuning

Figure 3 indicates the schematic of the proposed VCO with the linearized transconductance technique. The oscillation condition of an LC-based VCO can be represented as (1):

$$g_m \ge 1/R_{tank} \tag{1}$$

where  $g_m$  and  $R_{tank}$  are the transconductance of the active part and equivalent resistance of the passive part, respectively.



Figure 3. Top block diagram of the proposed linear transconductance voltage controlled oscillator (VCO).

In an LC-VCO, considering the noise produced by the parasitic resistance and cross-coupled pair as presented in [7], the output noise can be driven as in Equation (2):

$$dV_{out}^{2}[\omega] = KTR_{par}[1+A] \left(\frac{\omega_{0}}{\omega}\right)^{2} df$$
<sup>(2)</sup>

where *K*, *T*,  $R_{par}$ , and *A* are Boltamann's constant, temperature, parasitic resistance, and multiple noise factor of the cross-coupled pair, respectively. Therefore, the ratio of the output noise and signal power is equal to (3):

$$\frac{dV_{out}^2[\omega]}{P_{sig}} = \frac{KTR_{par}[1+A]\left(\frac{\omega_0}{\omega}\right)^2 df}{\frac{V_{amp}^2}{2}}$$
(3)

As can be easily observed, increasing the oscillation amplitude improves the phase noise performance of the VCO effectively. For a given current, the class-C VCO provides high oscillation amplitude characteristics. In the proposed architecture, the maximum achievable oscillation amplitude, through the famous saturation condition  $V_D > V_G - V_{th}$ , can be obtained, wherein  $V_D$ ,  $V_G$ , and  $V_{th}$  are the Drain, Gate and threshold voltages, respectively. When the Drain voltage is minimum, the Gate

voltage is maximum, and A represents the voltage gain from Gate to Drain of the feedback path, Equations (4) and (5) can be realized.

$$VDD - V_{amp} > V_{bias,Gate} + AV_{amp} - V_{th}$$

$$\tag{4}$$

$$V_{amp} < \frac{VDD - V_{bias,Gate} + V_{th}}{1 + A}$$
(5)

As can be seen, if the gate of the cross-coupled pair is biased at lower voltages, the proposed architecture provides a larger oscillation amplitude. According to Equation (5), if the gate of the cross-coupled pair is directly connected to the LC tank, to keep the transistors out of the triode region, the oscillation amplitude should be small. In this case, the amplitude is not allowed to be more than  $V_{th}/2$ . As shown in Figure 4, the DC isolation of the Gate and Drain through the coupling capacitance lets the Gate be biased lower than the Drain, thereby reducing the nonlinearity of the active part. Besides, this provides a high efficiency of DC current conversion into class-C current waveforms, and minimizes the generation of effective noise. The  $g_m$  drops with increasing oscillation amplitude, and cross-coupled pairs become nonlinear when entering the deep triode region. The  $g_m$  determines the active part noise power at the zero-crossing point, where the sensitivity of the phase noise is high [8]. Therefore, the proposed technique shrinks the operation of the LC-VCO in the triode region by extending the saturation region.



Figure 4. Swing of the Gate voltage in a conventional VCO and linear transconductance VCO.

In contrast, the transconductance linearization approach optimizes the design by eliminating the deep triode region, introducing larger amplitude, lowering noise generation, and improving the quality factor of the tank compared to conventional LC-VCOs.

The sizes of the cross-coupled pairs are chosen to be large enough to provide almost ideal switch characteristics. Since the topology provides high swing, the VDD is 0.8 V, and considering the tank load, its safe operation, which avoids Gate-breakdown inside the frequency tuning range, is guaranteed.

The trade-off between the quality factor of the switched capacitor bank and VCO's tuning range is an unavoidable issue in wide tuning range VCOs. The MOS switches introduce on-resistance in the signal path, which lowers the quality factor of the tank. To lower the on-resistance of the switch, a MOS transistor with a large size is required, considering the reduction of phase noise. The large sized MOS transistor introduces parasitic capacitance, and limits the tuning range of the VCO. Hence, for a wide tuning range, small size transistors are preferred.

As shown in Figure 5, the switched capacitor quality factor ( $Q_C$ ), when the switch is on, is proportional to Equation (6):

$$Q_C \propto 1/R_{sw} \tag{6}$$

where the value of  $R_{sw}$  can be calculated through Equation (7).

$$R_{sw} = \frac{1}{\mu_n C_{ox} \left(\frac{W}{L}\right) (V_{GS} - V_{th})}$$

where  $\mu_n$ ,  $C_{ox}$ , W, L,  $V_{GS}$ , and  $V_{th}$  are the mobility of the carrier, oxide capacitance, width, length, and the threshold voltage of the NMOS switch, respectively.



Figure 5. Switch capacitor equivalent circuit in off and on cases of switch.

Also, in the off state, the equivalent capacitance  $C_{off}$  is equal to Equation (7):

$$C_{off} = C \times Csw / [2 \times (C + Csw)]$$
<sup>(7)</sup>

Therefore, the switch size and the value of *C* should be chosen carefully to minimize the on-resistance of the switch, while keeping the frequency range wide. Since the frequency steps and the fixed unit capacitor of the coarse stage are large, the switch sizes in this stage are selected to be large enough to minimize the on-resistance. Besides, the switch sizes for the middle capacitor array are optimized through noise analysis, to make their noise contribution less than 2%.

As shown in Figure 3, the discrete frequency tuning of the VCO is realized by using 3-bits coarse and 6-bits middle tunings. The varactor offers a continuous frequency tuning range of 160 MHz/V at the center frequency of 16 GHz. Higher VCO gain (KVCO) needs a larger fixed capacitor inside the varactor, and introduces large AM (Amplitude modulation) to FM (Frequency modulation) noise. Therefore, the size of the capacitance of the varactor, or the value of KVCO, can be relaxed, while this capacitance can be compensated by increasing the size of the switches in both coarse and middle tuning stages. The middle capacitor bank and varactor are located at the Drain since the variation of the capacitance is less than that of the Gate. Two resistors inside the switched capacitor are provided to isolate the AC of the VCO nodes. To lower the thermal noise of the resistor inside the switched capacitor, its size is optimized to make the noise contribution less than 1%.

The tail inductor resonates with the parasitic capacitance of the tail node  $(2w_0)$ , and prevents the loading of the tank when one of the cross-coupled transistors enters the triode region, thereby improving phase noise. This method also enhances the linearity of the cross-couple transistors and lowers the current harmonics.

Figure 6 shows the schematic and simulated environment of the designed inductive buffer. In a transceiver, the buffer isolates the VCO from the other signal path of the transceiver. At both inputs of the buffer, AC coupling capacitors are provided to block the DC components of the AC waveform, so that the buffer remains correctly biased through the provided resistors R1 and R2. The switched capacitor adjusts the output swing of the buffer, with consideration of the carrier frequency and Process, Voltage, and Temperature (PVT) variations.



Figure 6. Schematic and simulated environment of the proposed inductive buffer.

As shown in Figure 7a, the VCO routing introduces parasitic inductance and resistance, which lower the quality factor of the tank. In order to shrink the output routing, the input transistors of the VCO buffer are located as close as possible to the VCO output's routing, as seen in Figure 7b. Thus, utilizing this technique keeps VCO output routings short, and enhances the phase noise performance of the VCO by around 1 dBc/Hz at 1 MHz offset frequency. To suppress the parasitic resistance and inductance, the routing of VCO outputs is stacked through the wide metal 7 and 8. Via and wide metal lines tie the parasitic inductance in parallel. Therefore, the introduced parasitic inductance can be lowered effectively, and the VCO offers linear VCO frequency steps. The simplified pattern of the layout is shown in Figure 7c.



**Figure 7.** (**a**) Layout of VCO core and buffer are separated, (**b**) the utilized technique for shrinking the routing and improving phase noise performance, (**c**) simplified layout pattern of the VCO routing.

#### 3. Experimental Result

Figure 8 shows the top layout of the proposed VCO. It consists of VCO core, tail inductor, VCO buffer and test buffer, and occupies a layout area of 0.14 mm<sup>2</sup>. The circuit is implemented in a 40-nm CMOS process. The VCO core consumes 24 mW from the power supply of 0.8 V, while inductive buffers consume 21 mW from the power supply of 1.1 V. The VCO operation is verified through the Electro-Magnetic (EM) based post-layout simulation. The proposed VCO satisfies the frequency range of 13 GHz to 19 GHz in all corner cases and temperatures, while the target frequency range is from 14 GHz to 18 GHz. The additional 2 GHz frequency range is considered for variation of the capacitors inside the switch capacitor bank during the fabrication process. The tuning range of the VCO can be calculated through Equation (8):

$$F_{TR}(\%) = (F_{max} - F_{min}) \times 100 / F_{center}$$
(8)



Figure 8. Top layout pattern of the proposed VCO.

Therefore, the proposed VCO offers the tuning range of 37.5%.

Figure 9 demonstrates the linearity and discrete tuning of the coarse and middle switched capacitor banks of the proposed VCO. In this simulation, the binary controlling bits of the coarse bank are changed from 001 to 100 (1 to 4 decimal), while the 6 bits of the middle capacitor array are adjusted from all "0" to all "1", within each code of the coarse bank. The maximum frequency resolution of the middle capacitor bank at 18 GHz is 100 MHz, while with a decreasing frequency this frequency step decreases. To avoid any blind zones inside the frequency range, there are overlapped frequencies between the coarse and middle tunings. The weights of the capacitors inside the middle stage are 1, 2, 3, 4, 8 and 16. One redundant bit with the weight of 3 is considered to avoid any blind zones inside the middle-frequency range.

Figure 10 indicates the continuous tuning of the VCO through controlling the voltage of VC. As the simulation results show, the VCO gain is 120 MHz/V, 180 MHz/V and 300 MHz/V, at 14 GHz, 16 GHz and 18 GHz, respectively.



Figure 9. Linearity of the discrete tuning of VCO by coarse and middle capacitor banks.



Figure 10. Continuous tuning of the VCO (KVCO).

Figure 11 shows the phase noise performance of the linear transconductance VCO at 14 GHz and 18 GHz carrier frequencies. The post-layout simulation results of phase noise at 14 GHz are –87.2 dBc/Hz, –113 dBc/Hz and –134 dBc/Hz at 10 kHz, 1 MHz and 10 MHz offset frequencies, respectively. The VCO offers phase noise performance of –87.4 dBc/Hz, –110 dBc/Hz and –130 dBc/Hz for 10 kHz, 1 MHz and 10 MHz offset frequencies at 18 GHz carrier frequency.



Figure 11. Phase noise performance of the VCO at 14 GHz and 18 GHz carrier frequencies.

Figure 12 shows the transient simulation result and output swing of the VCO with output buffers at 14 GHz and 18 GHz, respectively. In this simulation, the load condition for the test buffer is the

coupling capacitance and a 50-ohm load, and the VCO buffer is simulated considering the input load of the divider.



Figure 12. Transient simulation of the proposed VCO.

Table 1 summarizes the performance of the proposed VCO in different corners and temperatures. The results show that the variation of the phase noise in all corner conditions is less than 3 dBc/Hz, at the start and end of the frequency.

Table 1. Performance summary of the proposed VCO.

Corner, Temp (C)	14 GHz	18 GHz	Frequency Range
SS, -40	PN = -113.2  dBc/Hz	PN = -110.1  dBc/Hz	12.2 GHz~19.3 GHz
TT, 27	PN = -113  dBc/Hz	PN = -110  dBc/Hz	12.5 GHz~19.5 GHz
FF, 125	PN = 110.05 dBc/Hz	PN = -108.6  dBc/Hz	13 GHz~20 GHz

Table 2 features the proposed VCO as well as the recent works. It should be noted that the comparison with the fabricated works is not fair. However, the phase noise is calculated in the presence of the Low Dropout regulator (LDO) noise, considering the loading effect of the coupling capacitance, 50-ohm load, and the input load of the divider inside the PLL. Further, the frequency range of the VCO is optimized using the EM-based post-layout simulation results. Therefore, the provided simulation environment provides a fairer evaluation compared to the practical conditions.

To evaluate the performance of the VCO, the Figure of Merit ( $FoM_T$ ) is presented in Equation (9).

$$FoM_T = |PN| + 20\log_{10}\left(\left(\frac{f_0}{f}\right)\left(\frac{F_{TR}(\%)}{10}\right)\right) - 10\log_{10}\left(\frac{P_{DC}}{1mW}\right)$$
(9)

where the *PN*,  $f_0$ , f, *FTR*,  $P_{DC}$  are the phase noise, center frequency, offset frequency from the carrier frequency, frequency tuning range and power consumption, respectively. The proposed VCO indicates superior performance to those of previous works for wide range applications.

Parameter	[6]	[9]	<b>[10]</b>	[11]	[12]	This Work
Technology	90 nm CMOS	180 nm SiGE	130 nm CMOS	180 nm CMOS	130 nm SiGE BiCMOS	40 nm CMOS
Center Frequency	20.85 GHz	24.1	22.8	24	25.5	16 GHz
Tuning range	15.8%	15.3%	7.018%	25%	43%	37.5%
Phase noise @ 1 MHz (dBc/Hz)	-100.7 @ 20 GHz (Meas.) -102 dB (Sim.)	–107.7 @ 24 GHz –105.8 @ 22.5 GHz (Meas.)	–115 @ 22.8 GHz (Meas.)	–101.3 @ 24 GHz (Meas.)	–96 @ 25.5 GHz (Meas.)	-113 @ 14 GHz -110 @ 18 GHz (Sim.)
P <sub>DC</sub> (mW) FoM <sub>T</sub>	8.1 161.97	8.2 189.9	1.4 197.62	25 182.88	12 186	24 193.76

Table 2. Comparison of the proposed VCO with the other architectures.

### 4. Conclusions

In this paper, a wide-range and low phase noise VCO is designed with the linear transconductance technique. The presented architecture is implemented in a 40-nm CMOS process, and the VCO core consumes 24 mW power from the power supply of 0.8 V. The proposed VCO achieves a wide range, of 13 GHz to 19 GHz, and offers 37.5% frequency tuning range. The noise of the active part of the VCO is lowered through the transconductance linearization technique, and the passive part noise is reduced by optimizing the switched capacitor array. Besides this, the utilized layout techniques reduce the parasitic resistance and inductance of the VCO routings, thereby improving the phase noise performance. The circuit shows a FoM<sub>T</sub> performance of 193.76 dBc/Hz, and superior performance compared to recent works. The main application of the proposed VCO is in the structure of Phase-Locked Loops for mm-Wave 5G transceivers.

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