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On-Chip Terahertz Detector Designed with Inset-Feed Rectangular Patch Antenna and Catadioptric Lens

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Abstract: This study proposes an on-chip terahertz (THz) detector designed with on-chip inset-feed rectangular patch antenna and catadioptric lens. The detector incorporates a dual antenna and dual NMOSFET structure. Radiation efficiency of the antenna reached 89.4% with 6.89 dB gain by optimizing the antenna inset-feed and micro-strip line sizes. Simulated impedance was $85.55 - j19.81 \Omega$, and the impedance of the antenna with the ZEONEX horn-like catadioptric lens was $117.03 - j20.28 \Omega$. Maximum analyzed gain of two on-chip antennas with catadioptric lens was 17.14 dB resonating at 267 GHz. Maximum experimental gain of two on-chip patch antennas was 4.5 dB at 260 GHz, increasing to 10.67 dB at 250 GHz with the catadioptric lens. The proposed on-chip rectangular inset-feed patch antenna has a simple structure, compatible with CMOS processing and easily implemented. The horn-like catadioptric lens was integrated into the front end of the detector chip and hence is easily molded and manufactured, and it effectively reduced terahertz power absorption by the chip substrate. This greatly improved the detector responsivity and provided very high gain. Corresponding detector voltage responsivity with and without the lens was 95.67 kV/W with $NEP = 12.8 \text{ pW/Hz}^{0.5}$ at 250 GHz, and 19.2 kV/W with $NEP = 67.2 \text{ pW/Hz}^{0.5}$ at 260 GHz, respectively.

Keywords: THz detector; rectangular inset-feed patch antenna; catadioptric horn-like lens; CMOS process

1. Introduction

Terahertz (THz) detectors have been recently employed to assist security aspects for high-speed data communication, spectroscopy, concealed weapon detection, short-range radar, aviation assistance, cancer detection, and many more applications [1–4]. The THz spectrum region is in the middle of the microwave and infrared spectra and is sometimes known as sub-millimeter waves. Terahertz radiation ranges from 3 mm to 30 μ m with corresponding frequencies of 0.1–10 THz [5–9], which penetrate plastics, paper, and wood. The THz region is sometimes called the "THz Gap" [10–12] because optical and microwave theory do not fully apply for this frequency range.

Specific terahertz antennas are required to radiate and receive terahertz waves, acting as transducers to convert high-frequency current or waveguide energy into spatial electromagnetic wave energy, and directional radiation for transmission or the reverse conversion for receiving. However, designing an on-chip antenna in the terahertz band is somewhat difficult, partly because the system's dynamic range and transmission distance between the THz wave source and detector are influenced by antenna gain. Dielectric layers between the CMOS top and bottom metal layers are too thin to construct a



high gain antenna [13,14], and lossy silicon substrates significantly reduce on-chip patch antenna performance. However, problems can be solved with reasonable on-chip antenna design considering antenna gain and bandwidth.

Annular on-chip single-ended slot antennas can achieve approximately 4.5 dB gain with 50% radiation efficiency [15]. Although directional front-end antennas are unsuitable for THz detectors [16,17], Taeguk log periodic dipole antennas (LPDAs) can achieve a maximum 7.8 dBi gain at 73 GHz and circular LPDA antennas can achieve a maximum 9.25 dBi gain at 85 GHz [17,18]. The total size of these two antennas is $4.5 \times 10 \text{ mm}^2$ and they have complicated structures. Rectangular antennas are the most common on-chip design, leveraging simple structure and being compatible with standard CMOS processing [18,19]. The proposed rectangular antenna from [20] was 237.5 × 317 μ m² and operated at 300 GHz, but only achieved –2.1 dB gain. In contrast, the proposed THz dielectric resonator antenna (DRA) [21] employed a 500 μ m resonator to greatly enhance antenna gain. The DRA was 290–310 μ m wide and 390–410 μ m long, considerably larger than the traditional rectangular patch antenna, and provided measured 6.7 dB maximum gain at 327 GHz. Thus, there is considerable ongoing research to improve THz detector antenna gain.

This study proposes an on-chip terahertz detector with on-chip rectangular inset-feed patch antennas that was implemented using a United Microelectronics Corporation (UMC) 0.18 µm standard CMOS process and ZEONEX RS420 (ZEON Corporation, Tokyo, Japan) horn-like catadioptric lens. Section 2 discusses the antenna design and Section 3 introduces the detector structure, combining plasma wave-based terahertz detection in NMOSFETs (TeraFETs). Section 4 describes the horn-like catadioptric lens and Section 5 details testing for the prototype proposed THz detector antenna and lens. Conclusions are presented in Section 6.

2. On-Chip THz Antenna

The UMC 0.18 µm CMOS process provides six metal layers with intermediate dielectric layers (SiO₂) between them. The CMOS process can be used to design not only digital and analog circuits, but also optoelectronic devices [22–24]. The major advantage is that signals detected by the detector can be amplified and processed on the chip. However, silicon is lossy in the THz frequency range due to the short wavelength. Therefore, we implemented the antenna inset-feed patch in the Metal 6 (top metal) layer, using the Metal 1 (bottom metal) layer as a ground plane to reflect radiated power back to the NMOSFETs, hence reducing THz signal penetration into the lossy silicon substrate [20,21]. Metal 6 is 2.06 μ m thick and the SiO₂ CMOS process layer is 6.32 μ m thick. Radiation efficiency was low because these layers were too thin to emit an EM field, e.g., a similar antenna design achieved only approximately 20% radiation efficiency in simulation [14,21], with -1.6 and 0.1 dB gains, respectively. In contrast, the proposed antenna achieved 89.4% simulated radiation efficiency and 6.89 dB simulated gain. Figure 1 shows a cross-section of the proposed CMOS structure and Figure 2 shows a suitable patch antenna design using UMC 0.18 µm CMOS technology. Patch height, dielectric substrate properties, and patch conductor thickness are fixed depending on the specific UMC technology employed. We adopted substrate thinning and increased the ground plane size to increase antenna gain, with a micro-strip feed line.

Rectangular patch antennas can fully meet CMOS process design rules, in contrast with circle, ring, and other irregularly shaped antennas. Harrington [25,26] provided analytical expressions to explain the relationship between antenna performance and this separation. The empirical relationships for rectangular patches can be expressed as follows [13,14]:

$$W = \frac{c}{2f_0} \sqrt{\frac{2}{\varepsilon_{SiO_2}}} \tag{1}$$

$$\varepsilon_{\rm eff} = \frac{\varepsilon_{SiO_2} + 1}{2} + \frac{\varepsilon_{SiO_2} - 1}{2} \left(1 + 12 \frac{h}{W} \right)^{-1/2} \tag{2}$$

$$\Delta L = 0.412h \frac{(\varepsilon_{\rm eff} + 0.3)(W/h + 0.264)}{(\varepsilon_{\rm eff} - 0.258)(W/h + 0.8)}$$
(3)

and

$$L = \frac{c}{2f_0 \sqrt{\varepsilon_{\text{eff}}}} - 2\Delta L \tag{4}$$

where *W* is the radiation patch width, *c* is the speed of light in free space, f_0 is the operating frequency, ε_{eff} is the effective dielectric constant, $h = 6.32 \,\mu\text{m}$ (for the UMC 0.18 μm CMOS process) is the dielectric thickness between the patch and ground, ε_{SiO_2} is the SiO₂ dielectric coefficient, and *L* is the patch length.



Figure 1. Cross-sectional view for the proposed United Microelectronics Corporation (UMC) $0.18 \,\mu m$ CMOS design.



Figure 2. Structures for the proposed on-chip patch antenna.

Figure 2 shows the patch antenna structure, where *Wg* is the ground plane width, *Lg* is the ground plane length, *Win* is the insertion width, *Lin* is the insertion distance, *W1* is the micro-strip line width, and *L1* is the micro-strip line length.

Micro-strip and impedance matching networks were used to increase the input impedance. Table 1 shows the dimensions and performances of the patch antennas. Resonance is approximately 270 GHz and bandwidth is the region where S11 < -10 dB. Bandwidth for the patch antenna = 1.5 GHz with 271 GHz center frequency, and gain = 6.89 dB. Patch antenna (without lens) gain was higher than for other antennas, but still insufficient to provide a practical detector.

To ensure maximum power transmission, half the NMOSFET (TeraFET) channel impedance should be conjugated with the antenna output impedance. NMOSFET channel impedance depends on the gate voltage, hence the NMOSFETs should operate below the sub-threshold to obtain high impedance, forming a two-dimensional electronic fluid. The NMOSFET gate was powered by the antenna and matching network comprising a microstrip line and open stub line to achieve maximum power transmission. Performance comparison of terahertz antenna and lens are shown in Table 2, and without a lens or DRA, the patch antenna proposed in this study gets the highest gain of all.

Parameter	Patch
<i>Wg</i> (μm)	500
Lg (µm)	500
Ŵ (μm)	275
<i>L</i> (μm)	275
Win (µm)	90
<i>Lin</i> (µm)	65
<i>W1</i> (μm)	5.5
<i>L1</i> (μm)	122
Gain (dB)	6.89
Bandwidth (GHz)	1.5
Central frequency (GHz)	271
Radiation efficiency	89.4%

Table 1. Proposed on-chip rectangular inset-feed patch antenna dimensions and performances [14].

Tab	le	2.]	Perf	ormance	com	parison.
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Ref.	Process	Antenna	Center Frequency (GHz)	Gain (dB)	Bandwidth (GHz)
[27]	TSMC 65 nm CMOS	Ring	296	4.2	-
[28]	45 nm CMOS SOI	Slot ring	375	1.6	3
[21]	0.18 µm CMOS	Rectangle + DRA	327	7.9	2.5
		Rectangle	300	-2.1	4.1
[20]	TSMC 0.18 μm CMOS	Circular	300	5.30	11.3
		Diamond	300	5.94	9.6
[14]	0.18 µm CMOS	Rectangle	284	-1	7
[22]	65 nm CMOS	Ring with silicon lens	288	18.3	-
This work	UMC 0.18 µm CMOS	Rectangle	271	6.89	1.5

Antenna radiation efficiency η_{rad} is defined as the ratio of desired output power to supplied input power:

$$\eta_{rad} = \frac{P_{rad}}{P_{in}} = \frac{P_{in} - P_{loss}}{P_{in}} = 1 - \frac{P_{loss}}{P_{in}}$$
(5)

where P_{rad} is power radiated by the antenna, P_{in} is power supplied to the antenna input, and P_{loss} is power lost in the antenna. Other factors could also contribute to effective transmitted power loss, including impedance mismatch at antenna input, or receiving antenna polarization mismatch. However, these losses are external to the antenna and could be eliminated by proper matching networks, or proper receiving antenna choice and positioning. Therefore, these losses are not usually attributed to the antenna, compared with dissipative losses due to metal conductivity or dielectric loss within the antenna.

3. Terahertz Detector Circuit

Figure 3a shows the proposed detector structure. The antenna output port is connected to the matching network, and the network is connected to an NMOSFET (TeraFET) for improved power transfer efficiency. DC photoresponse ΔU of the on-chip amplifier output terminal was measured with an SR830 (Standard Research System, INC, Sunnyvale, CA, USA) lock-in amplifier which measured the ΔU amplitude submerged by noise at a determined frequency. Thus, the detector is thermal noise limited, and the detector also includes a dual antenna and dual NMOSFET (TeraFET) structure, which provides degree of noise suppression.



Figure 3. (a) MOSFET detector structure and (b) matching network between on-chip antenna and NMOSFET.

Antenna impedance is the ratio of input voltage to input current at the antenna feed. The best-case scenario is that antenna impedance is purely resistive and equal to half of the characteristic NMOSFET (TeraFET) impedance. There is no power reflection at the feeder terminal and no standing wave at the feed line, and antenna impedance changes slowly with frequency. Ideal matching will eliminate reactance. The NMOSFET's characteristic resistive impedance can be adjusted by increasing the applied voltage for better performance. Impedance matching between the antenna and NMOSFET (TeraFET) was achieved using an L-type matching network comprising a microstrip open-stub and microstrip line section to reduce the imaginary part magnitude as much as possible through the matching network, as shown in Figure 3b. Selected section dimensions were $L2 = 105 \,\mu\text{m}$, $W2 = 13.6 \,\mu\text{m}$, $L3 = 222 \,\mu\text{m}$, and $W3 = 13.36 \,\mu\text{m}$.

Figure 4 shows the circuit diagram for the proposed readout amplifier, comprising two stages. Stage 1 uses a common-source structure with large differential NMOS input pair (M1 and M2), since increased size can reduce input-referred flicker noise. M3 and M4 are also large to similarly reduce any contribution to flicker noise. M5 and M6 operate in their linear region, acting as resistors to provide common-mode feedback. C0 is a 10 pF capacitor with larger equivalent resistance at low frequency. M8 must operate in the sub-threshold region to provide direct current bias for M1 and M2 to ensure that the alternating current signal passes through the capacitor to M2 and M7 gate.



Figure 4. Proposed low-noise amplifier (LNA).

Stage 2 uses a PMOS input device with a common-source single-ended structure. The R and C provide Miller compensation for circuit stability when operated as a closed loop.

The proposed on-chip low-noise amplifier (LNA) shown in Figure 4 compensates for low-gain antennas. Two key issues must be solved during circuit design, namely low-noise performance and amplification ability under low frequency. The amplifier, fabricated in the standard 0.18 µm CMOS

process, provides 42 dB voltage gain and 4 MHz 3 dB bandwidth with capacitor feedback. Simulated input-referred noise is $17 \text{ nV/Hz}^{1/2}$ at 10 kHz and $113 \text{ nV/Hz}^{1/2}$ at 310 Hz. Amplifier power consumption is 3.5 mW with 1.8 V supply voltage. Figure 5 shows the input-referred noise curve.



Figure 5. Low-noise amplifier (LNA)'s input-referred noise.

4. Catadioptric Horn-Like Lens

Traditional catadioptric optical systems are commonly used for optical telescopes, telephoto lenses, early lighthouse focusing systems, searchlights, etc., with refraction achieved by lenses and reflection by curved mirrors. This lens can be easily integrated with THz detectors in contrast with conventional quasi-optical components, as shown in Figure 6. Terahertz detector front-end antennas have been physically coupled to back-end silicon lens previously to yield a compact system [10]. Therefore, this study proposes a THz detector with front-end antenna and lens symmetric about the z-axis to reduce signal loss in the substrate.



Figure 6. Cross-sectional view for the proposed catadioptric lens with inset 3D view of the lens.

Figure 7 shows a simulated lens, where the lens' out-radius R1 = 3 mm and in-radius R2 = 0.6 mm (R1 is about $\epsilon\lambda_0$, where λ_0 is the free-space wavelength [29]). Catadioptric lens length L4 = 6 mm, corresponding to $2\epsilon\lambda_0$ at 270 GHz. Length between out-radius and in-radius L5 = 2 mm, approximately λ_0 . When A1, A2, and A3 rays radiate from the source, they are totally reflected at the reflection plane (B1, B2, and B3, respectively), which are then refracted at the refraction plane (C1, C2, and C3, respectively).



Figure 7. Simulated gain at 280 GHz (**a**,**b**) individual patch antenna, (**c**,**d**) two patch antennas working together, and (**e**,**f**) two patch antennas with catadioptric lens. Red and brown lines represent 2D simulated radiation pattern along Phi = 0° and 90° planes, respectively.

The THz wave power received by the antenna is proportional to the antenna area, hence the two antennas receive approximately twice the power as a single antenna. The signal is converted to a direct voltage signal by the detector. Although the two NMOSFETs (TeraFETs) are connected in parallel, the output voltage does not increase but the output current doubles. Since the equivalent impedance

for the low-noise amplifier input is large, the output current is converted into a voltage, hence doubling the voltage signal after passing through the low-noise amplifier.

Figures 6 and 7 show that the refracted rays are distributed and converged to the z-axis, and the distribution provides up to 17.14 dB total gain, considerably higher than that achieved without the lens. The catadioptric dielectric lens is easily fabricated and illuminated compared with a silicon lens [10]. Figure 8 shows *S11*, gain, and efficiency with respect to frequency, where Port 1 is shown in Figure 2. Figure 9b shows that the catadioptric dielectric lens also increases antenna impedance.



Figure 8. Simulation results for (a) S11, (b) gain, and (c) efficiency.



Figure 9. Output impedance: (a) patch antenna and (b) two patch antennas with catadioptric lens.

5. Terahertz Chip Measurements

The THz detector performance was modelled using Dyakonov–Shur plasma wave theory. Plasma waves at the insulator–metal interface can not only achieve THz wave detection but also achieve power amplification [11,30], where ΔU is the measured voltage from the SR830 at the amplifier output terminal, as shown in Figure 3a [31], and there is a positive correlation between ΔU and received power. Plasma waves are usually overdamped in CMOS structures [32,33], hence we propose a non-resonant broadband detector [34].

The method in [31] was used to determine voltage responsivity R_V for a detector as follows:

$$R_V = \frac{\Delta U}{P_{det}} = \frac{\int_0^L E(x)dx}{L_{THZ}A_{det}}$$
(6)

where P_{det} is the THz power received by antennas, *L* is the length of the NMOSFET (TeraFET); *E* is the electric field intensity caused by terahertz waves, L_{THz} is the THz power density on the antennas measured with a large aperture THz power meter [31,33,35,36], as shown in Table 3, and $A_{det} \approx 0.075$ mm² is the rectangular inset-feed patch antenna size:

$$G_A = \frac{\Delta U}{G_T \left(\frac{\lambda}{4\pi R}\right)^2 R_V P_{BWO}} \tag{7}$$

following [21], where *GT* is the total gain due to the first and second lenses, and on-chip and lock-in amplifiers, as shown in Figure 10b, R = 40 cm is the distance between the backward wave oscillator (BWO) and detector, *PBWO* is the power of the BWO wave source [21], as shown in Table 3, and λ is the wavelength. By adjusting the position of the lenses and the THz power meter, the THz power meter position of maximum L_{THz} is recorded, then the THz power meter is replaced with detector chip.



Figure 10. (a) Measurement setup for the detectors, (b) micro-photo of the chip, (c) detector test platform, (d) R_V and *NEP*, and (e) gain.

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Frequency (GHz)	PBWO (mW)	L _{THz} (mW/mm ²)	Δ <i>U</i> without Lens (μV)	Δ <i>U</i> with Lens (μV)
200	12	213	46.6	540.8
210	14	240	57.1	707.4
220	6	133	92.3	402
230	2	26	96.7	93.1
240	4	67	8.6	246.85
250	10	160	141.3	1148.04
260	16	267	144.3	1338
270	10	187	105.4	749

Table 3. NMOSFET test results.

The gain of the horn-like lens is as follows:

$$G_L = \frac{R_{Vwith \ lens}}{R_{Vwithout \ lens}} \tag{8}$$

NMOSFET channel thermal noise is the dominant noise source for a non-current biased NMOSFET detector. Noise equivalent power (NEP) determines the detector noise component with respect to the particular wavelength and measurement bandwidth, and represents the minimum optical power required for output signal-to-noise ratio = 1 [37]. Since the on-chip amplifier and detector are integrated on the same chip, low-noise amplifier noise cannot be measured separately. However, simulation shows low-noise amplifier *NEP* to be very small, hence amplifier flicker noise was negligible and need not be considered. Therefore, we estimated the detector *NEP* as follows:

$$NEP = \sqrt{4kTR_{ds}/R_V} \tag{9}$$

where *k* is the Boltzmann constant, *T* is the measurement environment temperature (nominally 300 K), and R_{ds} is half of the drain-source resistance.

The NMOSFET threshold voltage was approximately 0.45 V. The detectors were tested with gate voltages from 0.15 V to 0.36 V and bias voltage = 0.238 V for maximum R_V . The NMOSFET is most suitable to operate in the sub-threshold region, forming a two-dimensional electronic fluid, increasing channel resistance sufficiently, and most likely to obtain maximum R_V .

Figure 10e shows that the detector with catadioptric dielectric lens achieved $R_V = 95.67 \text{ kV/W}$ with $NEP = 12.8 \text{ pW/Hz}^{0.5}$ at 250 GHz, whereas it achieved $R_V = 19.2 \text{ kV/W}$ with $NEP = 67.2 \text{ pW/Hz}^{0.5}$ at 260 GHz without the lens. Comparing Figure 10d with Figure 8, simulated frequencies for maximum R_V differed from the measured case. The most likely cause was fabrication error. Figure 10e shows patch antenna gain with and without catadioptric lens calculated from Equations (6)–(8). G_A is relatively meaningless due to the on-chip and lock-in amplifiers, but G_L is accurate. Patch antenna gain with a catadioptric lens was slightly lower than the simulation result.

6. Conclusions

This study proposed a THz rectangular inset-feed patch antenna that can be easily achieved in CMOS technology and can be integrated perfectly with a low-noise amplifier. However, the antenna has narrow bandwidth and is sensitive to dielectric constant and shape. The dielectric constant cannot be changed by the circuit and antenna designer for standard CMOS processing, but antenna impedances and operating frequency can be controlled by reasonable on-chip antenna design considering antenna gain and bandwidth. A front-end ZEONEX RS420 catadioptric horn-like lens greatly improved voltage responsivity of the THz detector.

Two patch antennas with lens achieved 17.14 dB maximum simulated gain at 267 GHz, while the gain of two patch antennas is 4.5 dB at 260 GHz and the gain of two antennas with catadioptric lens is 10.67 dB at 250 GHz.

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