

Article

A K_u -Band RF Front-End Employing Broadband Impedance Matching with 3.5 dB NF and 21 dB Conversion Gain in 45-nm CMOS Technology

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Abstract: This paper presents a K_u -band RF receiver front-end with broadband impedance matching and amplification. The major building blocks of the proposed receiver front-end include a wideband low-noise amplifier (LNA) employing a cascade of resistive feedback inverter (RFI) and transformer-loaded common source amplifier, a down-conversion mixer with push-pull transconductor and complementary LO switching stage, and an output buffer. Push-pull architecture is employed extensively to maximize the power efficiency, bandwidth, and linearity. The proposed two-stage LNA employs the stagger-tuned frequency response in order to extend the RF bandwidth coverage. The input impedance of RFI is carefully analyzed, and a wideband input matching circuit incorporating only a single inductor is presented along with useful equivalent impedance matching models and detailed design analysis. The prototype chip was fabricated in 45-nm CMOS technology and dissipates 78 mW from a 1.2-V supply while occupying chip area of 0.29 mm². The proposed receiver front-end provides 21 dB conversion gain with 7 GHz IF bandwidth, 3.5 dB NF, −15.7 dBm IIP₃ while satisfying < −10 dB input matching over the whole input band.

Keywords: complementary; push-pull; resistive feedback inverter; stagger tuning; wideband matching; wideband LNA

1. Introduction

Many wireless communication standards have evolved, and continue to do so, in the millimeter-wave regime to accommodate an ever-increasing demand for various applications such as 5G communications, corresponding to which the number of devices is increasing, resulting in communication under heavily congested spectrum. Heavily congested spectrum entails the use of broadband spectrum sensing receiver for efficient and maximum utilization of the desired frequency spectrum.

The implementation of broadband sensing device is a difficult task with the major hurdles being the design of broadband amplifier and local oscillator (LO) signal synthesizer. All these parameters entail harsh design requirements with strict trade-offs, which are hard to meet simultaneously. At the system level, therefore, an architecture is required that can process broadband signals with less stringent design requirements.

RF channelization is an alluring method to achieve broadband spectrum sensing where the channelized receiver bifurcates the incoming RF band into multiple channels [1]. Ref. [2] presented the design challenges and requirements of channelized receiver operating from DC-40 GHz, where

both series and parallel channelization concepts have been adopted to ease-off the requirements on RF front-end design for agile spectrum analysis.

Some of the previously reported works have proposed wideband receivers with good system performances. [3] reported a low-noise block (LNB) which down-converts the Ku-band (10.5–13 GHz) to the L-band (0.75–2.25 GHz). The system uses two-stage, narrow band cascode LNA topology, which requires a large number of inductors to achieve good input match along with high gain. The intense use of inductors in LNA and mixer in [3] renders the architecture unappealing in terms of area occupation. Similarly, [4] presented yet another LNB with system specifications similar to those in [3]. However, this work only provides amplification in a limited band, where the gain contribution from the LNA is the lowest. Moreover, the use of two-stage, inductor degenerated IF amplifier (used to compensate for the gain contribution from LNA) requires large area and high power consumption. L. Jia et al. [5] described a 10.7–12.75 GHz RF band front-end, implemented in 65-nm CMOS technology with the LNA using capacitive feedback to achieve wideband matching. However, as the results suggest, the proposed LNB fails to achieve < -10 dB input and output matching over the complete input RF band. Moreover, an external HEMT device with low noise figure (NF) of 0.45 dB and conversion gain of 10 dB has been employed to meet the NF requirements in [5]. It is worth mentioning that most of the earlier reported works have been designed for input RF bands with relatively narrow signal bandwidths (less than 3 GHz in most of the cases). This work, as the core building block of RF channelization receiver in [2], aims at the design and implementation of an extremely wideband RF front-end covering 10–20 GHz broad input bandwidth (which includes the whole K_u -band) driven by 10 GHz local oscillator (LO) signal to downconvert the input RF band to IF (intermediate frequency) with good dynamic range performance.

The paper is organized as follows. Section 2 reviews the receiver architecture for the 10–20 GHz band reception. Section 3 describes detailed analysis for designing the building blocks of the proposed receiver to achieve desired performance while maintaining adequate power efficiency. Section 4 provides the simulation and measurement results followed by the conclusion in Section 5.

2. Receiver Architecture

Figure 1 shows the complete architecture of the implemented receiver front-end. The proposed system consists of an LNA with both wideband input matching and signal amplification, an on-chip passive BALUN for single-ended to differential signal conversion along with action as a load of LNA, and down-conversion mixer. The 10 GHz LO signal is applied externally through two-stage inverter-based buffers. The down-converted IF signal in DC–10 GHz band is interfaced to off-chip 50Ω termination through an output buffer.

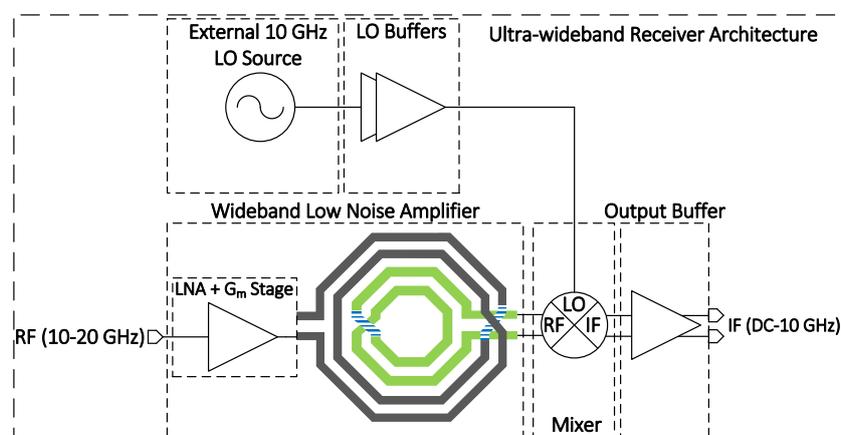


Figure 1. Proposed receiver architecture.

The major considerations for 10–20 GHz receiver front-end include the NF, bandwidth, and conversion gain. With the broadband signal amplification required in the first stage of a receiver, LNA topology with minimum NF, large bandwidth, and maximum possible amplification are required. Moreover, mixing of LO and RF signal with minimum LO-IF and LO-RF feed-through is critical for zero-IF signal reception when this front-end is utilized for the channelization receiver [1,2].

3. Proposed Receiver Front-End

A description of the major building blocks, including wideband LNA and mixer, is given in the following sections.

3.1. Low Noise Amplifier (LNA)

Low-Noise Amplifier (LNA) with wide bandwidth is one of the most crucial components in designing receivers for instrumentation systems, optical communications, and software defined radios (SDR) [6]. Distributed Amplifiers (DA) were extensively used in the past to achieve high gain and broadband input matching. Several low power DA architectures have been proposed [7,8]; however, their main downside was occupation of large chip area. Hence, DAs have been deemed as an unsuitable choice for fully integrated receivers. The common source amplifier with inductive degeneration has been the most widely used topology to implement LNA [9], because of its high gain, good noise performance, and ability to match to the source impedance. However, inductor degenerated LNA is an inherently narrowband circuit topology with series RLC resonator as an input matching network [10]. Such an implementation provides high gain over a narrow band, and hence is not suitable for the broadband signal reception. Such a scheme can be adopted for wideband signaling provided that the power budget available for the whole system is high.

Resistive-feedback LNA provides high gain and broadband characteristics, along with good input matching, lower NF, and occupy small chip area [11]. Figure 2a shows the architecture and design philosophy of the proposed two-stage wideband LNA. The two-stage topology ensures wideband signal reception by enhancing the LNA bandwidth using lowpass type first stage, and bandpass type second stage. The first stage enhances the low frequency content around the lower end of resonant frequency of the second stage, and combined together with the bandpass type second stage, guarantees wideband RF input signal reception and amplification. Figure 2b shows the schematic of proposed on-chip LNA. It consists of RFI as the first stage of LNA and a transformer-loaded common source amplifier as a second stage. The RFI can be thought of as an extension of resistive feedback common source amplifier, and can provide high linearity and good power efficiency as compared to its conventional counterpart, i.e., resistive feedback common source amplifier. As for the input matching to 50 Ω source, a single matching inductor, $L_{matching}$, has been employed. According to the Friis NF equation [12], the NF of the overall system depends on the NF of the first stage, given that the gain of the first stage is adequately high. The DC gain of the RFI is given by:

$$A_v = \frac{[\frac{1}{R_F} - G_m][r_{on} || r_{op}]}{1 + \frac{r_{on} || r_{op}}{R_F}} \quad (1)$$

In Equation (1), $G_m = g_{mn} + g_{mp}$, where g_{mn} and g_{mp} are the transconductances of the NMOS and PMOS devices in the RFI. Equation (1) states that the gain of the LNA can be increased by increasing the transconductance of both NMOS and PMOS devices. This is possible only if the output resistances of both NMOS and PMOS devices stay constant over device size variation. However, in short channel devices, by increasing the size of transistors to obtain high G_m at the same DC current, the corresponding output resistances decrease and, hence, the intrinsic gain of the RFI stays relatively constant. The NF of the RFI is given by [13]:

$$NF = 1 + \gamma \left[\frac{1}{G_m R_S} + G_m R_S \left(\frac{r_{on} || r_{op}}{R_F + r_{on} || r_{op}} \right)^2 + \frac{2(r_{on} || r_{op})}{R_F + r_{on} || r_{op}} \right] \quad (2)$$

where R_S is the source resistance and γ is the thermal noise coefficient for the NMOS and PMOS devices with values ranging from 1 to 2 in saturation condition. In short channel MOSFETs, the value of $r_{on} || r_{op}$ is usually very small, if the size of the transistors is chosen very large to increase the transconductance of the MOSFETs, and, hence, this value can drop below 100 Ω . Therefore, in Equation (2), if $R_F \gg r_{on} || r_{op}$, then only the first term in the bracket will dominate. Accordingly, increasing the G_m and satisfying $R_F \gg r_{on} || r_{op}$ condition simultaneously not only makes the gain of first stage LNA to approach its intrinsic gain, i.e., $G_m(r_{on} || r_{op})$, but also reduces the NF of the overall system. It is important to note that Equation (2) only models the thermal noise effect of RFI and does not include $1/f$ noise, and, hence, Equation (2) is constant for all frequencies. Figure 3 shows the calculated and simulated NF of the RFI based on the parameters given in Table 1. A good correlation between post-layout simulated NF of RFI and calculated NF can be seen from approximately 1 to 12 GHz based on the given NF model. Given that the circuit is properly designed, the RFI can provide a gain almost twice that of a conventional resistive feedback common source amplifier. This also indicates that the g_m/I_D efficiency of the RFI is better as compared to simple resistive feedback common source configuration owing to the utilization of current reuse technique. From a more rigorous analysis, it can be proven that, if $R_F \gg R_{in}$, then the amplifier is biased near $V_{DD}/2$, which makes the amplifier linear and stable.

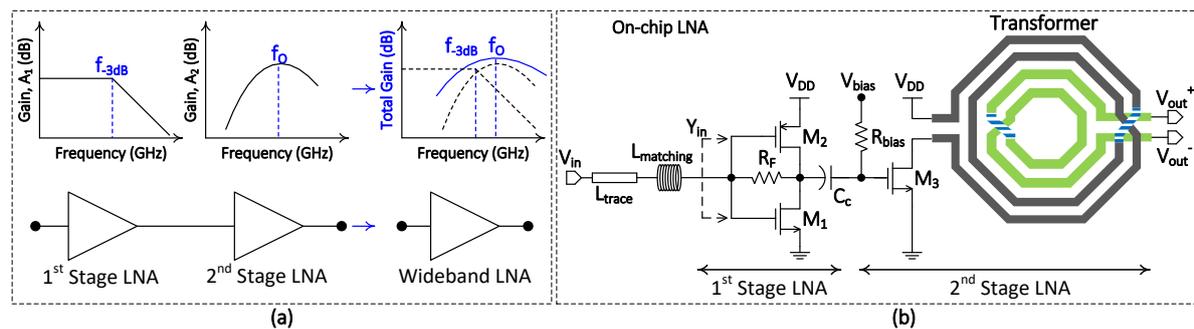


Figure 2. (a) LNA architecture and design philosophy; and (b) schematic of two-stage LNA with resistive feedback inverter (RFI) as first stage, and transformer-loaded common source configuration as second stage.

Table 1. LNA transistor sizing and component values (top), and DC operating parameters (bottom).

Component	Value
M_1 (L/W) (μm)	54/0.04
M_2 (L/W) (μm)	108/0.04
M_3 (L/W) (μm)	48/0.04
L_{matching} (pH)	390
L_{trace} (pH)	≈ 120
R_F (k Ω)	0.42
C_C (pF)	0.9
R_{bias} (k Ω)	44
Parameter	Value
G_m (mS)	155
C_{GS} (fF)	65
C_{GD} (fF)	39
$r_{on} r_{op}$ (Ω)	39
C_{in} (pF)	0.260–0.256 *
R_{in} (Ω)	60–49 *

* Only within 10–20 GHz band.

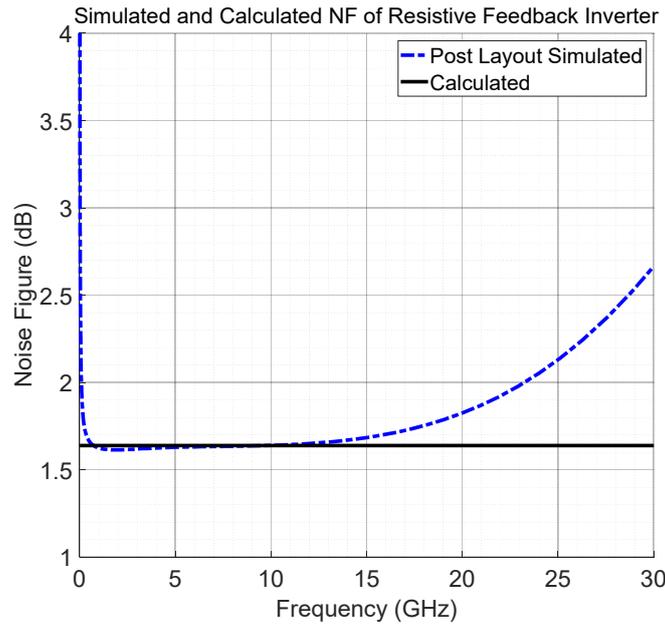


Figure 3. Calculated and simulated NF of RFI.

With the input signal having a 10 GHz bandwidth in this work, it is necessary that not only wideband amplification is achieved, but also the input of the LNA is matched to the source resistance over this whole frequency band to allow maximum power of the signal to be transferred to the LNA input. Hence, a wideband matching circuit needs to be designed as opposed to commonly employed narrowband matching techniques. Ref. [14] proposed a three-section bandpass Chebyshev filter to achieve ultrawideband input matching ranging 3.1–10.6 GHz RF input band. However, the proposed three-section filter employs three on-chip inductors to achieve wideband matching. It can be easily seen in [14] that the majority of the on-chip area has been occupied by the input matching network. One of the major focuses of this work is to alleviate this issue and achieve input matching with as few passive components as possible, provided that a slight compromise on the NF of whole system can be made.

$$G_{in} = \frac{1}{R_{in}} = \frac{(1 + G_m(r_{on} || r_{op})) (R_F + r_{on} || r_{op} + \omega^2 C_{GD}^2 R_F^2 (r_{on} || r_{op}))}{(R_F + r_{on} || r_{op})^2 + \omega^2 C_{GD}^2 R_F^2 (r_{on} || r_{op})^2} \tag{3}$$

$$B_{in} = \omega C_{in} = \frac{\omega C_{GS} (R_F^2 + (r_{on} || r_{op})^2) + 2\omega C_{GS} R_F (r_{on} || r_{op}) + \omega C_{GD} R_F^2 G_m (r_{on} || r_{op}) + \omega^3 C_{GS} C_{GD}^2 R_F^2 (r_{on} || r_{op})^2}{(R_F + r_{on} || r_{op})^2 + \omega^2 C_{GD}^2 R_F^2 (r_{on} || r_{op})^2} \tag{4}$$

With only first-order approximations taken into account by ignoring the parasitic capacitances and gate resistance, the input admittance, $Y_{in} = G_{in} + jB_{in}$, of the RFI can be given by Equations (3) and (4), where $C_{GS} = C_{gsn} + C_{gsp}$ and $C_{GD} = C_{gdn} + C_{gdp}$. It can be observed from Equation (3) that the real part of input impedance is dependent on the frequency. Hence, the transistors in RFI should be sized so that not only desirable gain and NF is achieved, but also an input conductance of around 20 mS is obtained within the input band of interest, i.e., from 10–20 GHz. Based on MATLAB simulations, Equations (3) and (4) are plotted in Figure 4. Based on the parameters given in Table 1, the input conductance, G_{in} , falls in the range of 16.6–20 mS in the desired input frequency band. Moreover, the input susceptance, B_{in} , increases almost linearly with frequency, which implies that the input admittance of the RFI can be modelled by a resistor in parallel with a capacitor. In Figure 4, the input resistance, R_{in} , and input capacitance, C_{in} , fall in the range from 60 to 49 Ω , and from 0.260 to 0.256 pF, respectively, based on the parameters chosen for transistor and other passive components in LNA. Combining this model of input admittance with the input matching inductor and a small pad

capacitance results in a π -network. Figure 5 shows the equivalent model of the input matching circuit, i.e., $L_{matching}$, along with the input admittance, Y_{in} , of RFI and the pad capacitance, C_{pad} . The input trace inductance, L_{trace} , connecting the input pad and the matching inductor has been ignored here for simplicity, and hence the value of $L_{matching}$ are evaluated at higher resonant frequencies relative to desired RF input band. Eventually, L_{trace} will shift the resonant band from higher end to the desired input band of 10–20 GHz. In the following, it is theoretically demonstrated that the proposed network can achieve wideband input matching with only a single matching inductor.

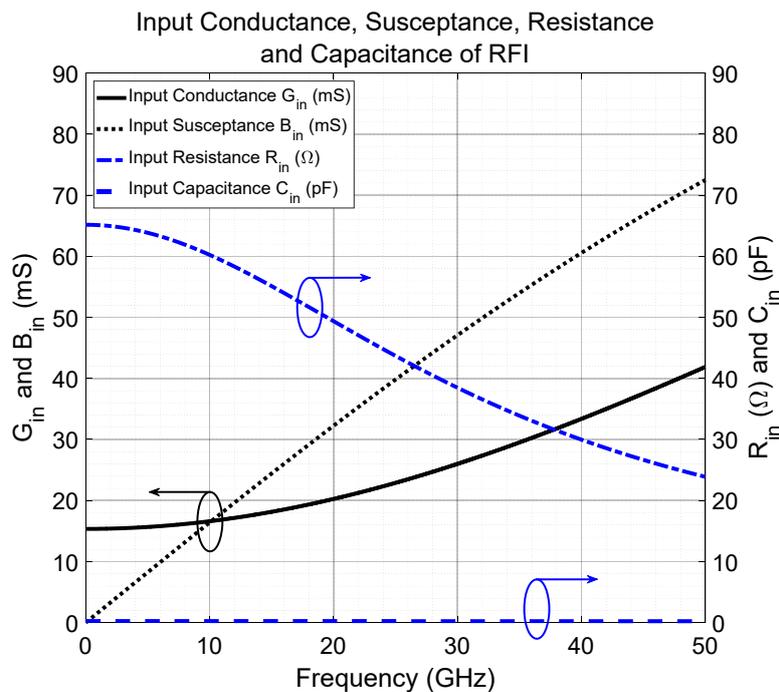


Figure 4. Input conductance (G_{in}) and susceptance (B_{in}) of the RFI.

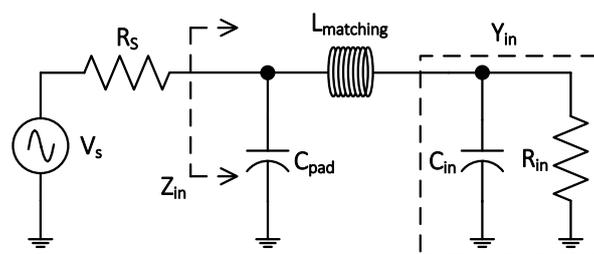


Figure 5. Equivalent model of input matching circuit accounting for the parallel input resistance and capacitance, R_{in} and C_{in} , respectively, along with pad capacitance, C_{pad} .

It is desired that the impedance, Z_{in} (or equivalently Y_{in}), being seen at the input pad should be equal to R_s (or equivalently $1/R_s$ if talking in terms of admittance parameters) over the whole input frequency band. The π -matching network can be designed by considering it as two cascaded L -section matching circuits, as described in Figure 6. It is important to note that R_1 and R_2 are the series resistances of their respective inductors. The 1st L -section matching network tunes out C_{in} at a lower frequency, while the 2nd L -section matching network tunes out C_{pad} at a higher frequency, since the value of pad capacitance is quite small. To tune out C_{in} at 15 GHz (which is the midpoint frequency of interest of the input band, and is hence called $f_{o,low}$), it is important to evaluate the value of the inductor L_1 along with its series resistance, R_1 , that can achieve such a task, and that value can be evaluated as per the following expression:

$$L_1 = \frac{R_{in}^2 C_{in}}{1 + \omega^2 R_{in}^2 C_{in}^2} \tag{5}$$

$$R_1 = \frac{\omega L_1}{Q_{L1}} \tag{6}$$

where $Q_{L1} = 15$ is chosen as the quality factor of inductor L_1 . Having plotted Equations (5) and (6) in Figure 7, the desired value of L_1 to tune out C_{in} at 15 GHz is roughly equal to 280 pH. It is interesting to note, however, that the value of L_1 is frequency dependent and that Equation (5) provides freedom in choosing the value of L_1 which can tune out C_{in} at any desired frequency of interest. For instance, to tune out the C_{in} at 10 GHz, the required value of inductor would roughly be equal to 478 pH. The value of equivalent series resistance, R_1 , can be chosen based on Equation (6). In Figure 7, the value of R_1 is approximately equal to 1.76 Ω at $f_{o,low} = 15$ GHz. The input admittance and impedance at the intermediate node, $Y_{in,1}$, plotted in Figure 8, can be theoretically derived as:

$$Y_{in,1} = \frac{1}{Z_{in,1}} = \frac{1 + j\omega R_{in} C_{in}}{R_{in} + (R_1 + j\omega L_1)(1 + j\omega R_{in} C_{in})} \tag{7}$$

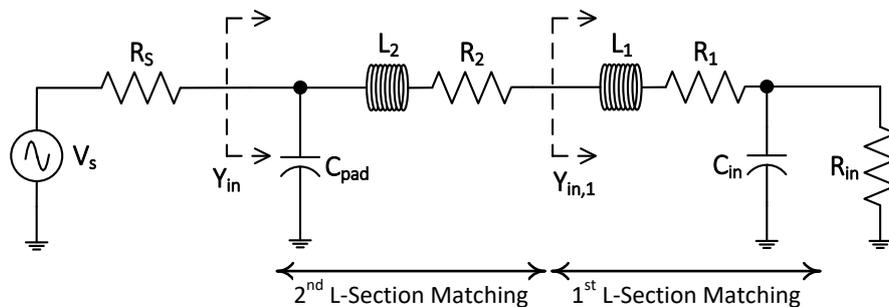


Figure 6. π -matching network thought of as cascaded L-section matching networks.

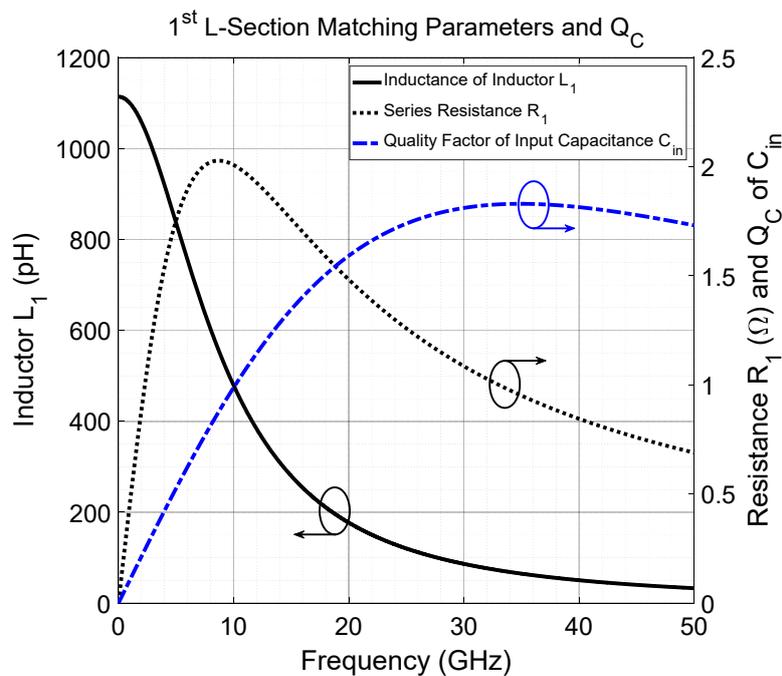


Figure 7. Inductor L_1 and resistance R_1 vs. frequency.

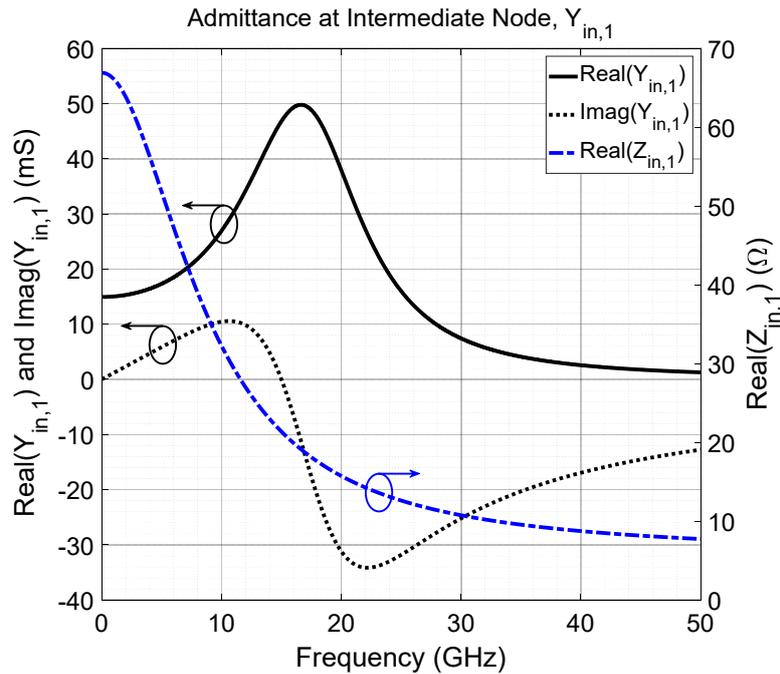


Figure 8. Admittance and resistance at intermediate node, $Y_{in,1}$.

As evident in Figure 8, the chosen value for L_1 indeed tunes out C_{in} at desired resonant frequency, $f_{o,low}$, which suggests that the input impedance at the intermediate node is composed purely of the resistive portion at $f_{o,low}$, and is given by:

$$R_{in,1} = \frac{R_{in}}{1 + Q_C^2} + R_1 \tag{8}$$

where Q_C is the quality factor of C_{in} , also plotted in Figure 7. Equation (8) marks a reduction in series resistance being seen at the intermediate node at $f_{o,low}$. With $Q_C = \omega R_{in} C_{in} = 1.3$ at $f_{o,low}$, the value of input resistance is approximately halved as compared to R_{in} of RFI, where the input resistance varies from approximately 32 to 16 Ω at the intermediate node within the band of interest. However, the reactive part is zero only at $f_{o,low}$ and non-zero over rest of the frequency band, which illustrates that the total impedance being incorporated into the 2nd L -section matching network is $Z_{in,1}$, where the value of $Z_{in,1}$ at $f_{o,low}$ is given by Equation (8).

To ensure a good, wideband power match, it is vital that C_{pad} is also tuned out at $f_{o,high}$, and, to achieve it, the value of the inductor, L_2 , in the 2nd L -section matching network must be sorted out. To tune out the C_{pad} , it is important that the total impedance, $Z_{in,1}$, being incorporated in 2nd L -section matching network given by Equation (7), is purely resistive at $f_{o,high}$. As mentioned above, Figure 7 provides freedom in choosing the value of inductor L_1 to tune out C_{in} at any desired higher resonant frequency. At a frequency of 25 GHz (which is referred to as $f_{o,high}$), the value of L_1 obtained in Figure 7 is roughly equal to 119 pH with the value of R_1 being equal to 1.25 Ω . This implies that at $f_{o,high}$, only resistive part will be incorporated into 2nd L -section matching network, and the circuit at $f_{o,high}$ would resemble the one in Figure 9. It is important to note that, at $f_{o,high}$, the total series resistance for L_2 has now increased from mere R_2 to $R'_2 = R_2 + R_{in,1@f_{o,high}}$. With the multiple unknowns being encountered, an initial assumption is required to evaluate the value of L_2 . As a starting point, it assumed that $R_2 = aR_1$, where a is a multiplication factor ranging from as low as 1 to as high as required. By transforming the series RL circuit into parallel RL circuit in Figure 9, the values of equivalent components can be found by the subsequent equations:

$$R'_{2,parallel} = (R_2 + R_1 + \frac{R_{in}}{1 + Q_C^2})(1 + Q_{L2}^2) \tag{9}$$

where R_1 , R_{in} , and Q_C can be evaluated at $f_{o,high}$ in Figures 4 and 7. In this design, C_{pad} has been modeled by a 100 fF capacitance. The equivalent parallel inductance, $L_{2,parallel}$, can be found by:

$$L_{2,parallel} = \frac{1}{\omega_{o,high}^2 C_{pad}} \tag{10}$$

$$(R_1 + R_2 + \frac{R_{in}}{1 + Q_C^2})Q_{L2}^2 - (\omega_{o,high}L_{2,parallel})Q_{L2} + (R_1 + R_2 + \frac{R_{in}}{1 + Q_C^2}) = 0 \tag{11}$$

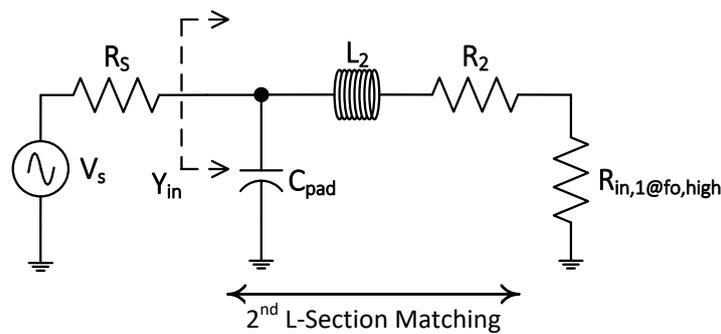


Figure 9. Desired circuit configuration at $f_{o,high}$.

The quality factor of the equivalent parallel inductor can be evaluated through $Q_{L2} = R'_{2,parallel} / (\omega_{o,high}L_{2,parallel})$, and by substituting the values of Equation (9) in the aforementioned equation, a quadratic equation is obtained as mentioned in Equation (11). Solving Equation (11) yields two different values of Q_{L2} from which the larger one would be employed in subsequent calculations. Having known the values of R'_2 and Q_{L2} , the required value of 2nd L -section series matching inductor, L_2 , can be figured out through the following equation:

$$L_2 = \frac{Q_{L2}R'_2}{\omega_{o,high}} \tag{12}$$

In the current design, having arbitrarily chosen the value of $a = 10$ along with the values of R_1 , R_{in} , and Q_C at $f_{o,high}$, and $L_{2,parallel}$ being obtained from Equation (10), Q_{L2} is evaluated equal to 2.15 and from Equation (12), the value of L_2 is found equal to 333 pH. With the values of all the components evaluated, the input impedance, Z_{in} , at the source can be described by the following equation:

$$Z_{in} = \frac{1}{Y_{in}} = \frac{j\omega L_2 + R_2 + Z_{in,1}}{1 + j\omega C_{pad}(j\omega L_2 + R_2 + Z_{in,1})} \tag{13}$$

Figure 10 shows the MATLAB simulation plot of the input impedance, Z_{in} , and input matching, S_{11} . In Figure 10, the input resistance seen by the source ranges from 40 to 63 Ω over the entire frequency band of 10–20 GHz, while the reactive portion ranges from -13 to 22 Ω . It can also be observed that the reactive portion of Z_{in} is zero at the desired resonant frequencies of 15 and 25 GHz. The effect of L_{trace} has been ignored in the aforementioned calculations. If the inductance of L_{trace} is taken into account, then the resonant frequency shifts towards the lower end of the input RF band, as shown in Figure 11. It can also be seen that the input matching no longer remains < -10 dB above 18 GHz. Hence, to compensate for this, the value of L_2 is reduced to 270 pH in the second iteration, which provides a perfect < -10 dB matching over whole input band. Having found the values of both the inductors at $f_{o,high}$, the value of an equivalent, single matching inductor can be found as follows:

$$L_{matching} = L_{1,f_{o,high}} + L_{2,f_{o,high}} \tag{14}$$

From Equation (14), the value of an ideal, single equivalent matching inductor, $L_{matching}$, is equal to 389 pH, which is equal to the one used in the actual design (value mentioned in Table 1). It must

be noted that the value of L_1 evaluated previously was 280 pH. However, to resonate both C_{in} and C_{pad} , the total matching inductance value must satisfy Equation (14). In that case, if the value of L_1 was chosen to be 280 pH, then that of L_2 must be 109 pH as opposed to 270 pH. The quality factor of an equivalent, single matching inductor, $L_{matching}$, can be calculated by:

$$Q_{matching} = 2\pi f_{o,high} \left(\frac{L_{1,f_{o,high}}}{R_1} + \frac{L_{2,f_{o,high}}}{R_2} \right) \tag{15}$$

Therefore, apart from the input trace inductance (which is fixed because of the fixed length of the input signal line in the current design, but can be changed by laying out the chip in more efficient way so as to reduce L_{trace}), a theoretical $L_{matching}$ value of 389 pH with a quality factor of approximately 18 is required to tune out both C_{in} and C_{pad} over a wide bandwidth of 10 GHz. A minor difference was observed in Z_{in} between the MATLAB simulation and actual design, which can be attributed to the unaccounted parasitics and first-order approximations made in evaluating the input admittance of RFI mentioned in Equations (3) and (4).

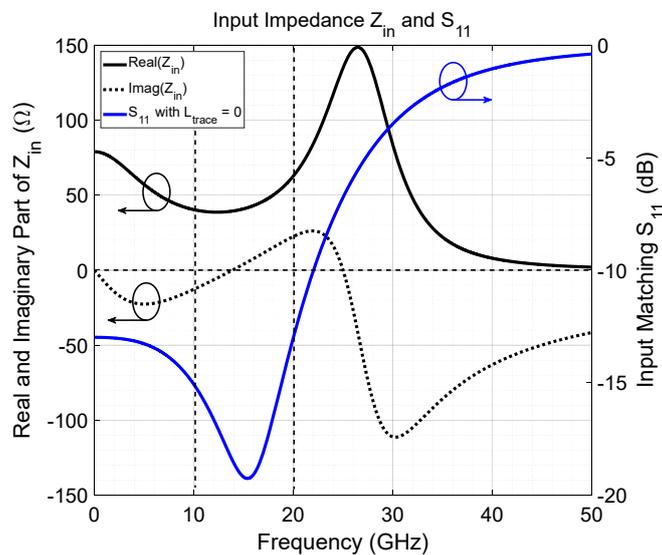


Figure 10. Input impedance and matching at the source.

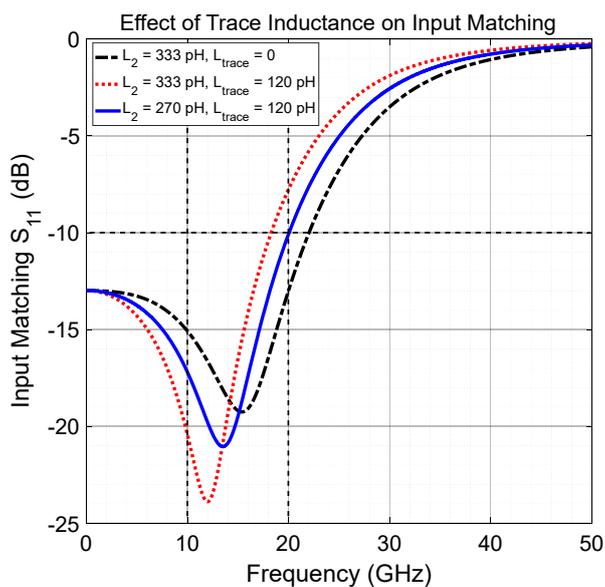


Figure 11. Effect of L_{trace} on input matching.

With implementation of the aforementioned input matching network and considering that the maximum signal power has been transferred to the input of the LNA, this whole band requires amplification. The first-stage LNA, i.e., RFI, cannot provide such a wideband signal amplification alone as it depicts a lowpass nature. In this work, the input signal is a bandpass type and, hence, an amplifier with bandpass characteristics is desired. The transformer-loaded common source amplifier has been adopted as the second stage, which is AC coupled with the previous stage and has its own biasing through the bias resistor, R_{bias} , as shown in Figure 2. This configuration provides high gain in a narrow band (with its bandwidth dependent upon the quality factor of the transformer) around the resonant frequency, f_o , which in this work is tuned towards the upper end of the input band. The proposed signaling method combining the lowpass and bandpass characteristics of first and second stage LNA, respectively, can thereby provide wideband signal amplification. The LNA gain plot has been shown in the Figure 12. The 3-dB cutoff frequency of the first-stage LNA is 16.5 GHz (relative to 10 GHz), while the second-stage LNA is resonant at 18 GHz. The total LNA gain has been shown as a sum of gain from both stages where LNA provides a gain flatness of less than 4 dB. The transformer load also achieves single-to-differential conversion. Without the transformer load, high gain due to the front-end along with the parasitic ground inductance incurs unwanted oscillations. Another reason to convert the amplified signal from single-ended to differential is that the differential signaling in the mixer reduces the second-order distortions and improves robustness to power supply and substrate noise while also improving stability.

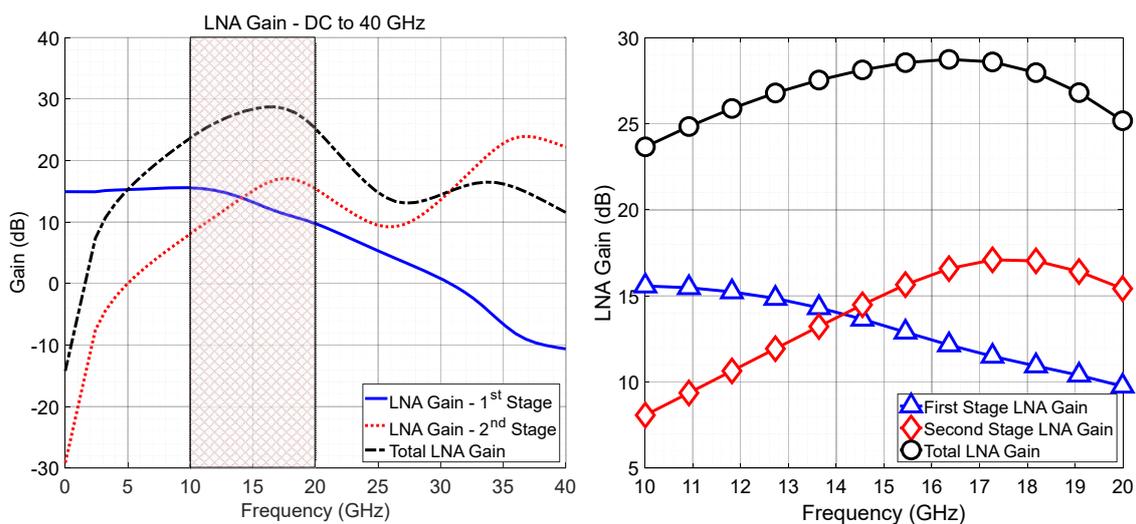


Figure 12. Simulated LNA gain with individual contribution from first and second stages: extending from DC to 40 GHz (left); and zoomed-in version from 10 to 20 GHz (right).

3.2. Mixer

Figure 13 shows the schematic diagram of a double balanced mixer where it has been implemented using a complementary switching and g_m -stage [15]. The push–pull architecture improves both the g_m -efficiency and noise performance, whereby also improving the linearity due to complementary input stage by eliminating the second order distortions [16]. This structure also improves the LO feedthrough to the output, which is extremely critical in this receiver front-end because the high-end frequency of the band coincides with the LO signal. Even though the push–pull single-balanced mixer architecture inherently performs single-to-differential conversion, transformer load for the LNA is utilized to perform single-to-differential conversion to utilize double-balanced mixer configuration. The double balanced mixer operation ensures stability by mitigating the effect of parasitic ground loops. Current-efficiency is maintained due to the complementary g_m -stage even with the double-balanced mixer structure. Table 2 presents the mixer sizing parameters along with the values of passive components employed.

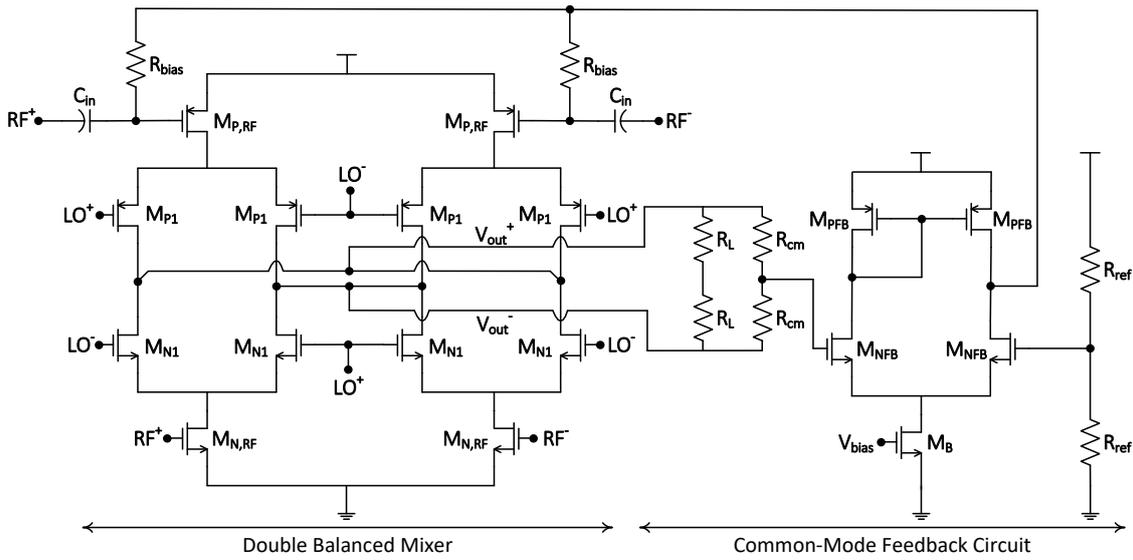


Figure 13. Double balanced mixer with complementary LO switching and g_m -stage (left); and common-mode feedback circuit (right).

Table 2. Mixer transistor sizing and component values.

Component	Value
M_{N1} (L/W) (μm)	48/0.04
M_{P1} (L/W) (μm)	48/0.04
$M_{N,RF}$ (L/W) (μm)	64/0.04
$M_{P,RF}$ (L/W) (μm)	48/0.04
M_{NFB} (L/W) (μm)	6/0.1
M_{PFB} (L/W) (μm)	12/0.1
M_B (L/W) (μm)	20/0.04
C_{in} (pF)	0.3
R_{bias} (k Ω)	55
R_{cm} (k Ω)	9
R_{ref} (k Ω)	14
R_L (k Ω)	0.085

Along with its inherent ability to reduce the LO feedthrough to the output, the common-mode feedback (CMFB) circuit further reduces the LO-IF feedthrough by mitigating the mismatch between the complementary g_m , i.e., g_{mn} and g_{mp} . The overall conversion gain of the implemented mixer can be derived as follows:

$$A_{CG} = \frac{2 (g_{mn} + g_{mp}) R_L}{\pi (1 + s R_L C_{eq})} \tag{16}$$

where R_L is the load resistance connected at the output terminal, C_{eq} is the total load capacitance, and g_{mn} and g_{mp} are the transconductances of the RF input voltage to current converters.

Considering that the input to the mixer is of bandpass type, ideally, a wideband mixer is desired so that it can downconvert the whole band to the desired IF band with minimum conversion loss. However, the RC time constant of the mixer appears as the main limitation in achieving wideband downconversion, as shown in Figure 14, where the mixer demonstrates a lowpass nature. The 3-dB IF bandwidth of the mixer is approximately equal to 4.66 GHz, and, above 7 GHz, the mixer shows conversion loss. This loss will manifest itself as overall gain loss of the system at frequencies above 7 GHz, as discussed below.

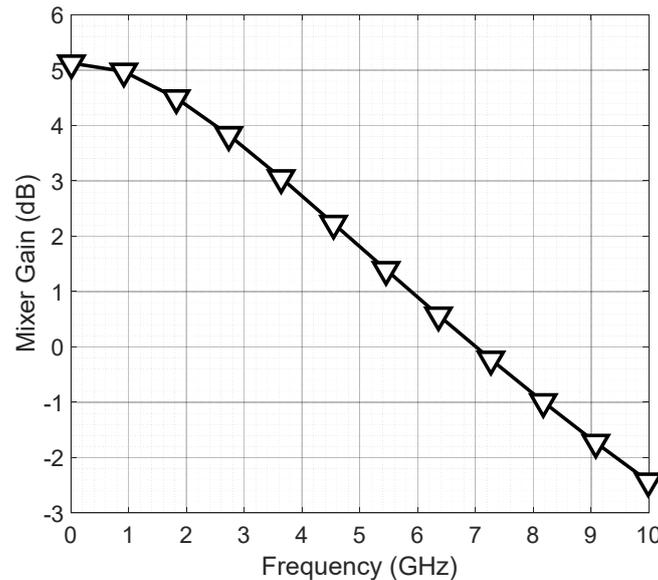


Figure 14. Simulated conversion gain of the implemented mixer.

Assuming that the transconductances of the RF input NMOS and PMOS devices are same, the implemented mixer provides twice the conversion gain as compared to the conventional mixer topologies. The gain-bandwidth (GBW) product of the mixer can be derived as follows:

$$GBW = \frac{2}{\pi} \frac{g_{mn} + g_{mp}}{C_{eq}} \quad (17)$$

where the equation implies that the GBW of the double balanced mixer with complementary LO and g_m stages is better as compared to the conventional double-balanced mixer. The g_m / I_D efficiency of the mixer is also better as compared to its conventional counterparts, since the effective g_m of the mixer is almost twice that of the normal mixer.

4. Measurement Results

The proposed ultra-wideband 10–20 GHz receiver front-end has been implemented in standard 45-nm CMOS technology. Figure 15 shows the fabricated chip micrograph having an occupied area of 0.29 mm². For measurement purpose, IF output and DC pads are wire bonded to PCB with a FR4 substrate while RF and LO signals are applied using on-wafer probing to minimize the losses and mismatches. The final measurement results are presented after de-embedding the PCB trace loss and the loss of cables from source to DUT and DUT to spectrum analyzer. The entire circuit consumes 78 mW from a 1.2-V power supply.

Figure 16 shows the post-layout simulation results of the proposed receiver over PVT variations. Figure 16a shows the variation in receiver gain, NF, and S_{11} over the global process corners (FF, TT, and SS). From the simulation results, the receiver gain is degraded at lower frequencies in FF corner relative to TT, while the degradation effect in the receiver gain is pronounced more at higher end of the IF band in SS corner as compared to the TT corner. The NF of the receiver degrades as one moves from TT to SS corner. However, the NF degradation is not severe over the global corner variations with the NF_{min} staying below 4 dB. The S_{11} plot indicates that the resonant frequency shifts towards higher frequency at SS corner in comparison to other corners but provides better matching. At the FF corner, the resonance frequency stays approximately the same as that in TT corner, but the amount of matching is relatively reduced. It is, however, encouraging to note that, within the band of interest (10–20 GHz), the input matching is still < -10 dB over all the corners. Figure 16b shows the receiver performance parameters over power supply variations. The power supply was varied from 1 to 1.2 V. As evident, reducing V_{DD} not only reduces receiver gain over the whole band, but also degrades

the NF. Similarly, input matching variations are shown, and, again, the input matching stays below -10 dB over the supply variations within the band of interest. Figure 16c shows the performance parameters against temperature variations, where the gain, NF, and S_{11} were measured at -20 , 30 , and 80 °C. Evidently, a rise in temperature degrades the performance of receiver in terms of gain and NF. However, the input matching is considerably tolerant to the temperature changes.

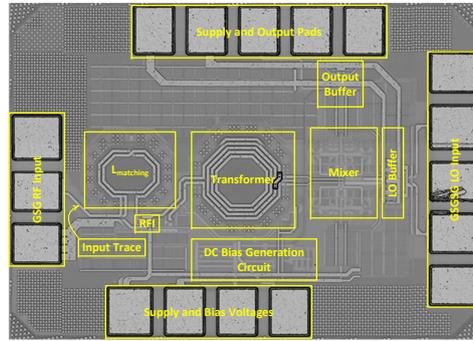


Figure 15. Chip micrograph.

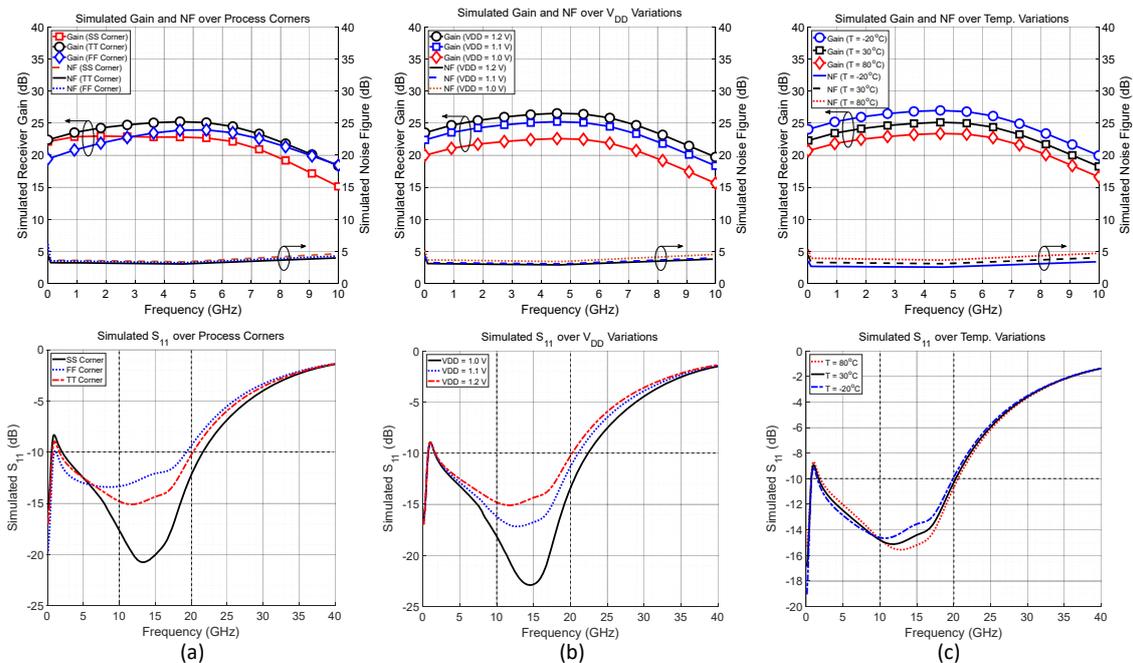


Figure 16. (a) Simulated receiver gain, NF, and S_{11} over global process corner variation; (b) simulated receiver gain, NF, and S_{11} over power supply variation; and (c) simulated receiver gain, NF, and S_{11} over temperature variation.

Figure 17 shows the simulated and measured conversion gain and NF results, respectively. The measurement results show a low frequency conversion gain of 21 dB as opposed to 24 dB obtained from the simulation, whereby the gain drops in an approximately linear fashion. Moreover, from the measured conversion gain, it was observed that the bandpass characteristic of the front-end has changed to lowpass characteristic. This indicates a shift in the resonant frequency of second stage LNA towards the lower end. The major reasons for the gain drop can be attributed to the IF output taken through SMA connector. From the electromagnetic simulation of a $50\text{-}\Omega$ transmission line (TL) mounted on FR4 substrate, it was observed that the TL shows good impedance characteristics up to 5 GHz, after which the impedance of the TL deviates from the ideal behavior and does not provide characteristic impedance of $50\ \Omega$ from thereon. The NF results show that the integrated NF over

whole IF band, i.e., 0–10 GHz, is 3.2 and 4.3 dB for simulation and measurement, respectively, with a minimum measured NF of 3.5 dB.

Figure 18 shows the input reflection coefficient, S_{11} . The measurement results show that input of the receiver is matched ($S_{11} < -10$ dB) to the source over a wide band of 10–20 GHz, with a little discrepancy observed at the higher end from around 18 to 20 GHz.

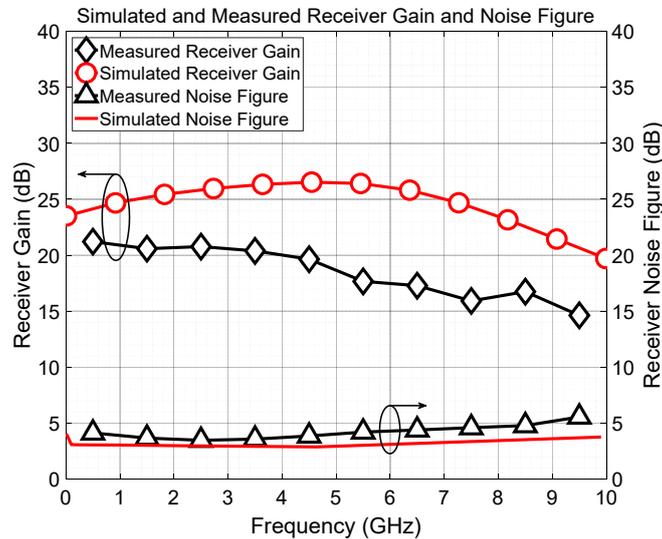


Figure 17. Simulated and measured receiver gain and NF.

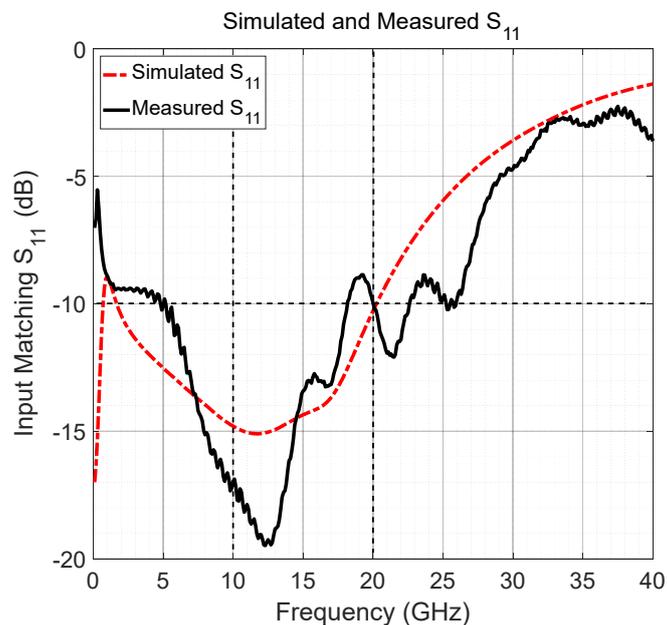


Figure 18. Simulated and measured input matching.

Figure 19 shows the linearity performance of the front-end. The measured IIP_3 is -15.7 dBm based on two-tone signal injected at 15.1 and 15.2 GHz, with the LO power set at 0 dBm and RF power swept from -45 to -15 dBm. Clearly, IIP_3 of the receiver shows poor linearity with the significant IIP_3 degradation occurring because of the active mixer. The cascaded NF and IIP_3 equation indicates a trade-off between the linearity and NF. To achieve a relatively higher linearity, a passive mixer could be implemented, which would effectively degrade the system NF, a totally undesired effect in the proposed receiver. Figure 20 shows the measured 1-dB compression point. The implemented front-end

shows a 1-dB compression point of approximately -26 dBm, 10.3 dB lower as compared to IIP_3 , which is quite close to the theoretical difference of 9.6 dB [17].

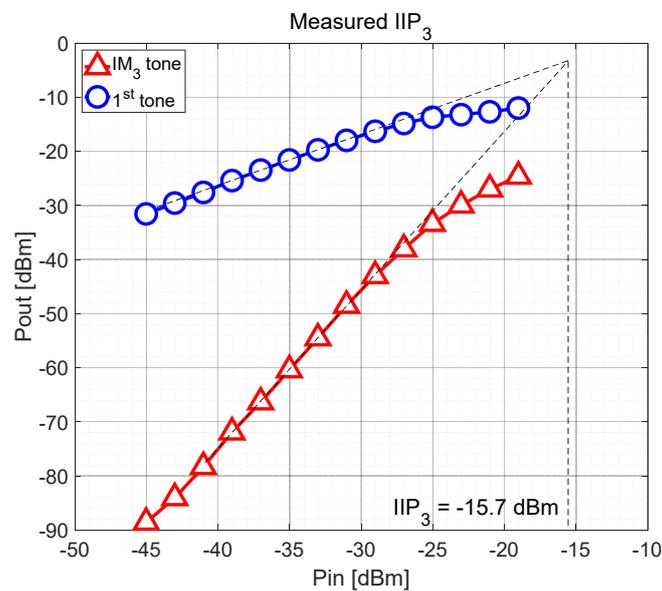


Figure 19. Measure third-order input intercept point.

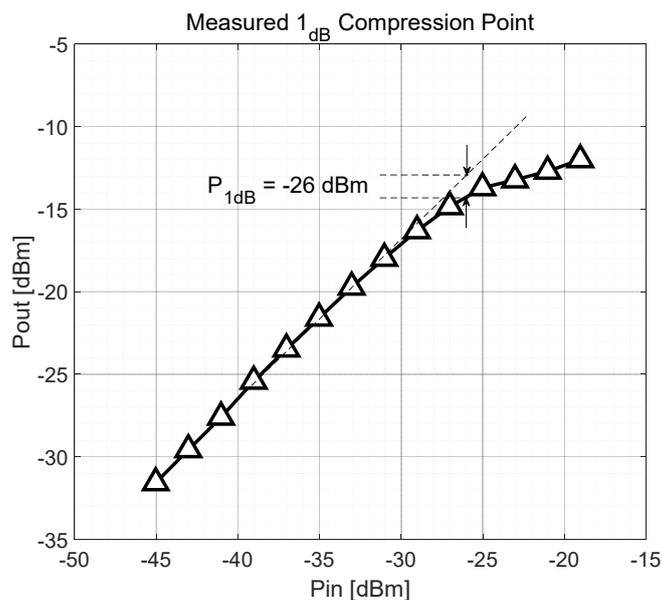


Figure 20. Measured IP_{1dB} .

Table 3 presents the performance summary of this work in comparison to the related works. Considering that the input is a broadband 10 GHz signal as opposed to most of the referred work, in terms of NF, power consumption, bandwidth coverage, and area occupation, the proposed receiver provides competitive performance as compared to the cited works. The work in [18] has similar performance to the proposed receiver in terms of input matching, IIP_3 , and power consumption, but the input signal bandwidth is extremely small with the input band centered at 24 GHz. The NF is also almost double as compared to the proposed work. The 12–20 GHz receiver in [19] accomplishes good wideband reception and linearity with gain performance similar to the proposed work, but is inferior in terms of NF, input matching, and power consumption. Similarly, [20] proposed a receiver with superior power consumption and gain as compared to the proposed receiver, but it has a

relatively narrowband reception of 1.48 GHz and poor NF. Even though the gain of the receiver in [21] is 53 dB over the 10 GHz bandwidth, the actual gain from the front-end is still 21 dB, where rest of the gain is provided by a baseband VGA. It is important to note that gain in almost half of the referred works is around 50 dB, which is due to the narrow RF input band. It is relatively difficult to achieve such a high gain over a broadband RF signal. The works presented in [22,23] provide extremely competitive receiver architectures with high gain, low NF, and low DC power consumption. However, these receivers provide such performance parameters over a relatively narrow bandwidth of 2.7 GHz. Similarly, the works in [24,25] provide competitive LNA architectures over extremely wide RF bandwidths. However, based on the post-layout simulation results, the proposed LNA provides even better performance in terms of gain, NF, and input matching as compared to these works. Therefore, as mentioned above, the most important parameters to measure the relative performance of the receivers is NF and input matching over the whole RF input band, in which case the proposed receiver stands out as compared to related works.

Table 3. Performance summary and comparison.

	Frequency (GHz)	Gain Max/Min (dB)	Peak Gain (dB)	NF (dB)	NF _{min} (dB)	S ₁₁ (dB)	IIP ₃ (dBm)	Power (mW)	Area (mm ²)	Technology
This Work	10–20	21.2/14.7	21.2	3.5–5.5	3.5 ^[1]	<−10	−15.7	78	0.29	CMOS 45 nm
JSSC [22]	0.1–2.8	50/10	50	1.8–2.2	1.8	<−10	5	27–40	0.9	CMOS 40 nm
ISSCC [23]	0.08–2.7	70/N/A	70	1.5–2.4	1.5	<−10	13.5	15.6	1.2	CMOS 40 nm
ISIC [5]	10.7–12.75	50/40	50	3.6–4.7	3.6 ^[2]	<−6	N/A	88	1.44	CMOS 65 nm
TCAS-I [18]	24	31.5	31.5	6.7–8	6.7	<−10	−13	78	1.92	CMOS 65 nm
APMC [19]	12–20	12/8	12	5.5–7	5.5	<−5	−4.4 ^[3]	263	1.1	CMOS 65 nm
TMTT [20]	14.25–15.75	N/A	23.5	5.6–6.3	5.6	<−10	−23.4	27	0.45	CMOS 65 nm
TCAS-II ^[7] [24]	0.5–7	16.8/14	16.8	2.87–3.77	2.87	<−10	−4.5	11.3	0.044	CMOS 65 nm
TMTT ^[7] [25]	1–20	12.8/9.5	12.8	3.3–5.3	3.3	<−10	5.8	20.3	0.096	CMOS 65 nm
JSSC [21]	8–18	53/50	53 ^[4]	6.7–7.8	6.7	<−8.5	−0.4	180	1.81	SiGe BiCMOS 130 nm
RFIC-S [3]	10.5–13	19.4/14.5	19.4	2.42–3.55	2.42	<−10	18.6	135	1.62	CMOS 180 nm
MTT-S [26]	10.7–13.5	52/50	51	5–5.8	5	<−10	−33 ^[5]	135	0.6 ^[6]	SiGe 180 nm

^[1] NF integrated over 10 GHz IF bandwidth = 4.3 dB; ^[2] SSB NF reported; ^[3] estimated from P_{1dB} point of −14 dBm; ^[4] includes the gain from baseband VGA; ^[5] estimated from the given OIP₃ using IIP₃ = OIP₃ − Gain; ^[6] core area = 0.43 mm²; and ^[7] only LNA.

5. Conclusions

A 10–20 GHz band RF front-end has been implemented in a commercial 45-nm CMOS process. The prototype receiver front-end achieves broadband signal reception while maintaining good signal to noise ratio. The proposed architecture is suitable as the front-end solution of the broadband spectrum-sensing device. A complementary transistor scheme is applied to the LNA as well as the down-conversion mixer, which improves the power efficiency while maintaining the performance. Stagger-tuned two-stage LNA implementation ensures the broadband signal amplification. The proposed receiver achieves a maximum conversion gain of 21 dB; a minimum and integrated NF of 3.5 and 4.3 dB, respectively; −15.7 dBm IIP₃; and less than −10 dB input matching over the entire RF input band from 10 to 20 GHz. The whole chip occupies 0.29 mm² area while consuming 78 mW power from 1.2-V supply.

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