

Review

# An Extensive Review of Multilevel Inverters Based on Their Multifaceted Structural Configuration, Triggering Methods and Applications

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**Abstract:** Power electronic converters are used to transform one form of energy to another. They are classified into four types depending upon the nature of the input and output voltages. The inverter is one among those types; it converts direct electrical current into alternating electrical current at desired frequency. Conventional types of inverters are capable of producing voltage at the output terminal that can only switch between two levels. The range of output voltage generated at the output is low when they are used for high power applications. To improve the voltage profile and efficiency of the overall system, multilevel inverters (MLIs) are introduced. In multilevel inverters the voltage at the output terminal is generated from several DC voltage levels fed at its input. The generated output is more appropriate to a sine wave and the  $dv/dt$  rating is also less leading to the reduction in EMI. Though they possess many advantages compared to the conventional inverters, the structural complexity and triggering techniques involved in designing multilevel inverters are high. Many studies are being carried out in defining new topologies of MLI with reduced switch as well as with the implementation of different PWM techniques. This paper will provide an extensive review on variety of MLI configurations based on the parameters such as the number of switches, switching techniques, symmetric, asymmetric, hybrid topologies, configurations based on applications, THD and power quality.

**Keywords:** multilevel Inverter; THD; power quality; PWM techniques

## 1. Introduction

The term MLI (multilevel inverter) was introduced in the late 20th century with the advent of a three-level converter. With the invention of multilevel inverters, the power rating of the device was increased owing to the number of levels and the device count was reduced when compared to conventional models. In recent times, the market for MLIs is becoming high in industrial sectors as well as in the fields where there is a need for high-power and high-voltage rating devices. Another interesting factor in the case of multilevel inverter is that it can be easily interfaced with renewable energy sources, plug in electric vehicles, batteries and capacitors [1]. Apart from this, the MLI delivers a high quality waveform with reduced harmonic distortion, capable of operating under fundamental and high frequencies, high power quality and better electromagnetic compatibility. The different classifications of multilevel inverters are as follows: the cascaded H-bridge multilevel inverter (CHB-MLI), the diode clamped multilevel inverter (DC-MLI) and the flying capacitor multilevel inverter (FC-MLI). The classification is shown in Figure 1.

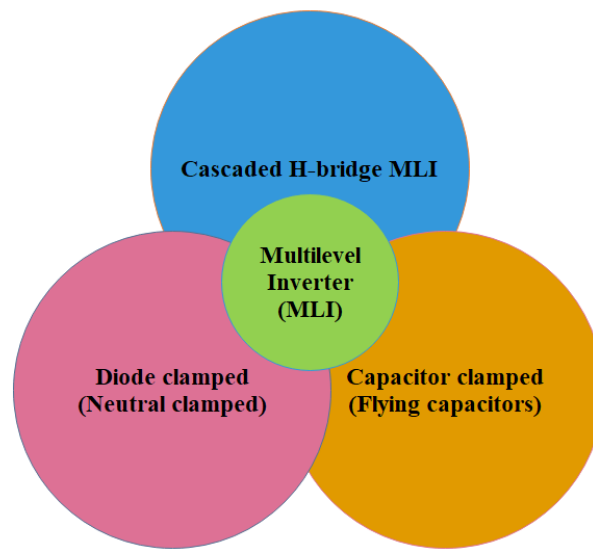


Figure 1. Basic classification of multilevel inverters (MLI).

In all the above-mentioned topologies, the quantity of electronic power switches required for designing the topology is high. The number of gate drives associated with these types is also high, which leads to a complex system. To reduce this complexity, several new topologies of MLI have been designed and tested by numerous researchers who are working in this field. The schematic of the newly derived topologies and techniques of MLI is shown in Figure 2.

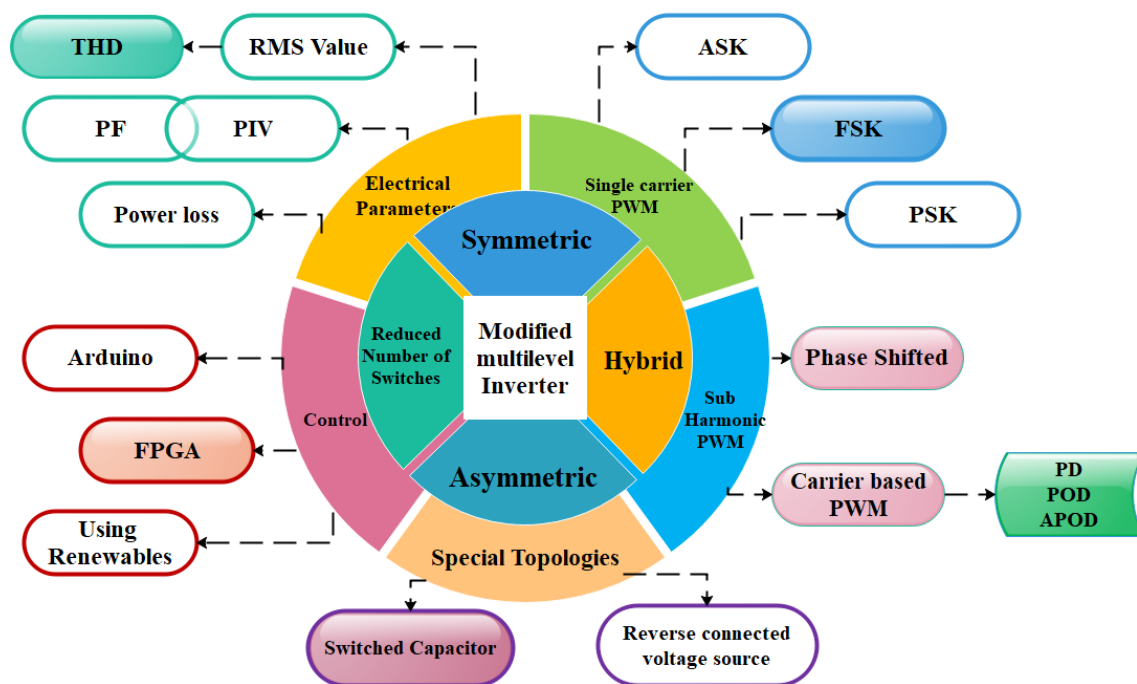


Figure 2. Classification of MLI types and techniques.

This paper discusses the different types of new topologies in MLI-based on structural configuration and also their applications, their switching techniques, THD reduction and power quality issues. The paper is organized in such a way that the structural configurations are discussed at first, followed by the switching techniques, then some special topologies, and finally the power quality and harmonic issues associated with the multilevel inverter.

## 2. Structural Configuration of Multilevel Inverters

Based on the structural configuration MLI is classified into three types namely symmetric, asymmetric and Hybrid MLIs.

### 2.1. Symmetric Multilevel Inverter

Conventional multilevel inverters such as CHB-MLIs, DC-MLIs and FC-MLIs fall under the symmetrical category, since the magnitude of the DC voltage sources employed in the system are equal [2]. A new power circuit topology for an 11-level output was designed and it is given in Figure 3.

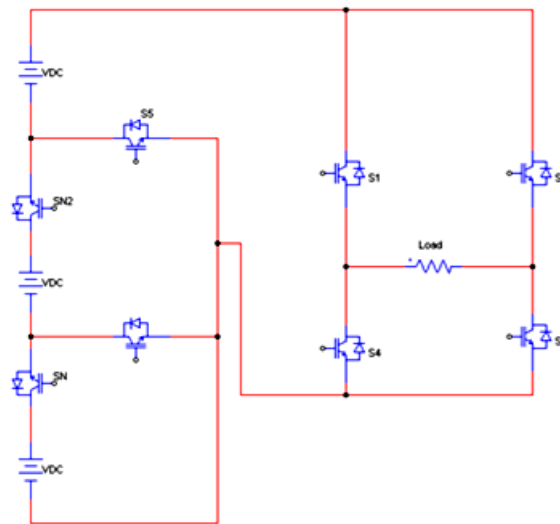


Figure 3. Circuit of 11-level inverter.

To increase the number of levels, two additional switches along with a DC voltage source was added to the existing configuration as given in [3]. But this configuration is different from the existing method due to the absence of a bidirectional switch in it. The desired voltage of the circuit configuration was derived from the following equation,

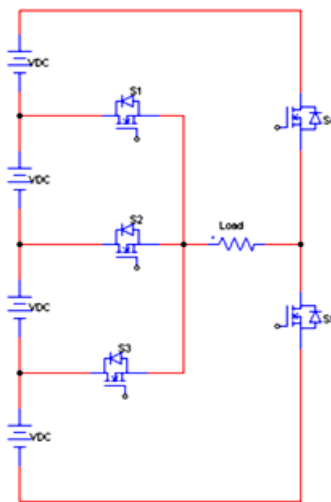
$$N_{\text{step}} = 2n + 1 \quad (1)$$

where  $n$  represents the number of dc voltage sources.

The maximum voltage at the output terminal ( $V_{\text{omax}}$ ) of this  $n$  cascaded multilevel inverter is:

$$V_{\text{omax}} = n \times V_{\text{dc}} \quad (2)$$

The voltage at the output end ( $V_o$ ) can be increased by connecting the 'N' number of basic circuits. Though the inverter topology explained in [4] delivers a maximum voltage output, the number of switches is high. This leads to increased switching losses in the system. To suppress this shortcoming, a seven-level MLI with four DC sources was proposed by the authors in [5]. The symmetric configuration works in a fashion based on a pulse pattern, which is unique in nature to trigger the switches at the proper instant. The reduction in switch count results in low switching losses even though the sources are less utilized. Instead of using an H-bridge, this topology employs two switches for reversing the polarity. The seven-level, five-switch MLI is given in Figure 4.



**Figure 4.** Circuit of seven-level five-switch inverter.

The output voltage levels for the investigated topology can be calculated as follows:

$$p = (2 * (S - 3)) \quad (3)$$

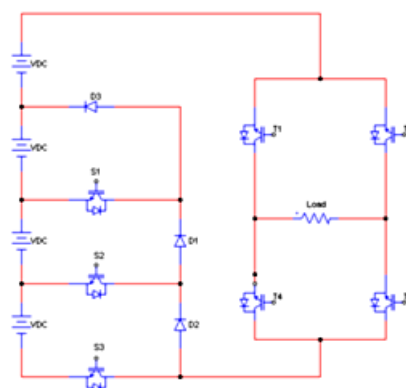
where,  $p$  = number of output voltage levels,

$S$  = number of switches

$$p = (2 * V_{dc} - 1) \quad (4)$$

where,  $V_{dc}$  = number of dc sources

One of the main advantages of the symmetrical multilevel inverter is that it possesses very high modularity, which is absent in case of the asymmetrical MLI. Several research works are being carried out in the field of multilevel inverters, especially in symmetric and asymmetric configurations due to their simplicity and efficiency compared to the conventional inverters. Such topologies are explained in a number of studies [6–10], where researches used a high number of power electronic semiconductor switches and gate drive circuits. Due to this, the circuit becomes complex and expensive. On account of this, a novel MLI with a reduced number of switching devices is suggested for producing a nine-level output. The circuit is shown in Figure 5.



**Figure 5.** MLI with reduced number of switches.

The overview of the symmetrical configuration for  $M$ -level output is given as:

The required number of controlled switches is given by

$$(M + 5)/2 \quad (5)$$



The number of driver circuits required

$$= (M + 5)/2 \quad (6)$$

The total number of diodes is given by

$$(M + 1) \quad (7)$$

The number of DC sources required can be determined as

$$(M - 1)/2 \quad (8)$$

Apart from this, the authors have also given a cascaded version of this nine-level topology [11], as shown in Figure 6.

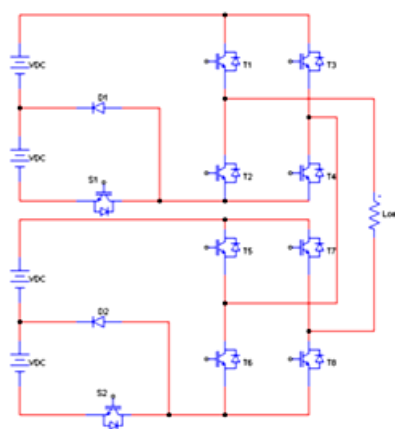


Figure 6. Cascaded MLI circuit.

The above configuration is designed in such a way that it has the ability to decrease the stress across the devices so that it can be employed in applications where there is a need for higher voltage. The H-bridge and the DC sources are switched with high switching frequency.

## 2.2. Asymmetric Multilevel Inverter

The only difference in the asymmetric multilevel inverter topology to that of symmetrical type is the rating of the DC input voltages and its control techniques. A cascaded H-bridge MLI with a lesser number of bridges is analyzed in [12]. This topology is capable of delivering maximum voltages at higher speeds even with minimum switching frequency. A seven-level asymmetric cascaded type inverter made up of two H-bridges for each phase is given in Figure 7. The DC source for the two H-bridges  $H_1$  and  $H_2$  is  $V_{dc}/2$  and  $V_{dc}$  respectively.

In the above figure, it is clearly shown that the asymmetrical inverter uses only two bridges (with eight switches) for generating seven levels of output. The inverter is also subjected to different PWM Techniques and the THD is found to be low. Another asymmetric configuration is proposed by the authors in [13] with a high frequency link as shown in Figure 8.

The high frequency link employed in the system is used to supply the supplementary bridge, which is made up of a series-resonant converter along with a ferrite core (torroid core) transformer and diode rectifiers. The transformer used in this topology is to provide galvanic isolation between the bridges. The operation of MLI is based on a control mechanism called nearest level control (NLC). The controller will match a voltage signal close to the reference signal value. The power delivered in this system is inversely proportional to the frequency.

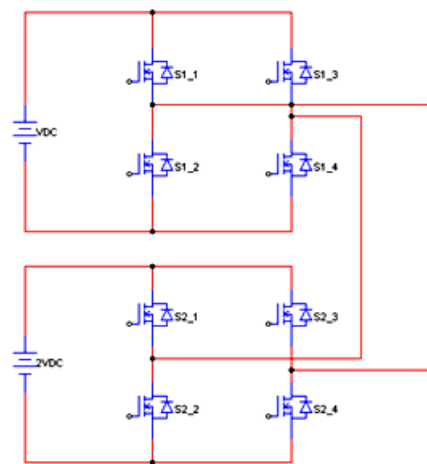


Figure 7. Seven-level cascaded type H-bridge MLI.

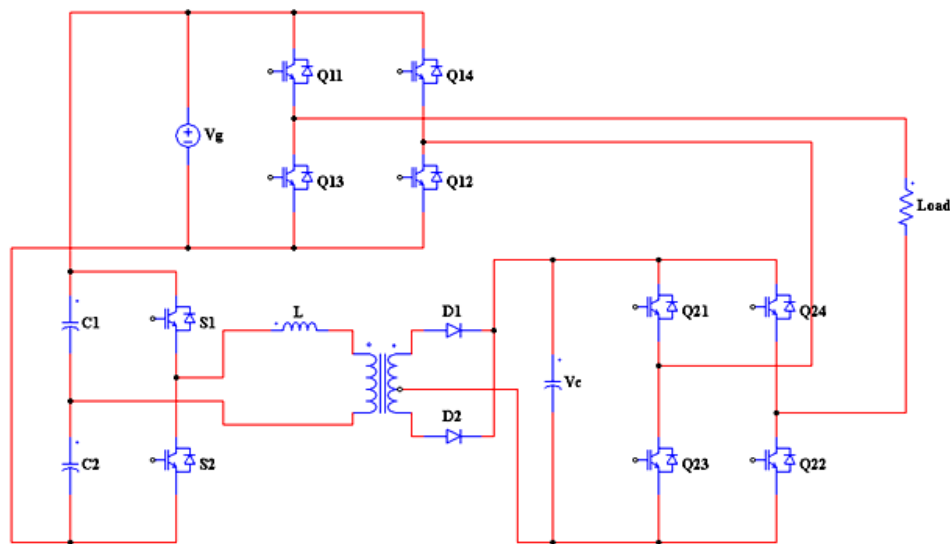


Figure 8. High frequency asymmetric MLI.

The controller is operated in such a way that the output voltage has to be varied whenever the source voltage is changed. This results in maintaining the voltage levels of the DC–AC converter and the total harmonic distortion.

One more cascaded H-bridge MLI is suggested by the researchers in [14] for a seven-level output. From the Figure 9, it is clearly understood that the number of switching devices gets reduced in this topology when compared to the conventional cascaded multilevel inverter configuration.

For the same seven-level output, a new MLI topology with switched capacitor (SC) technique is proposed and the circuit is given in Figure 10. It consists of a chopper and H-bridge inverter at the front and back, respectively.

A combination of switches is turned ON for producing a positive voltage and negative voltages [15].

The asymmetric topology is also capable of producing higher levels of voltage, as explained by the authors in [16]. The authors analyzed a 21-level MLI made up of a full bridge converter with semiconductor switches and different voltage sources. A set of switches was used to obtain the different levels of voltage. The circuit configuration is shown in Figure 11.

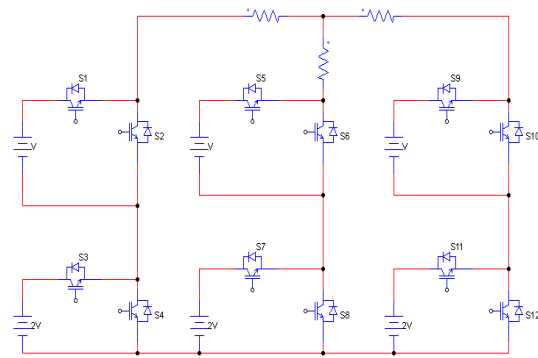


Figure 9. Circuit for seven-level cascaded MLI.

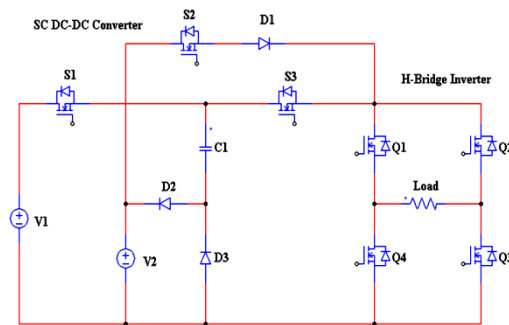


Figure 10. MLI based on switched capacitor.

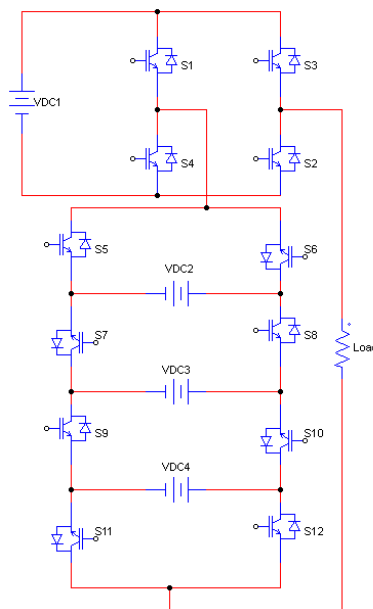
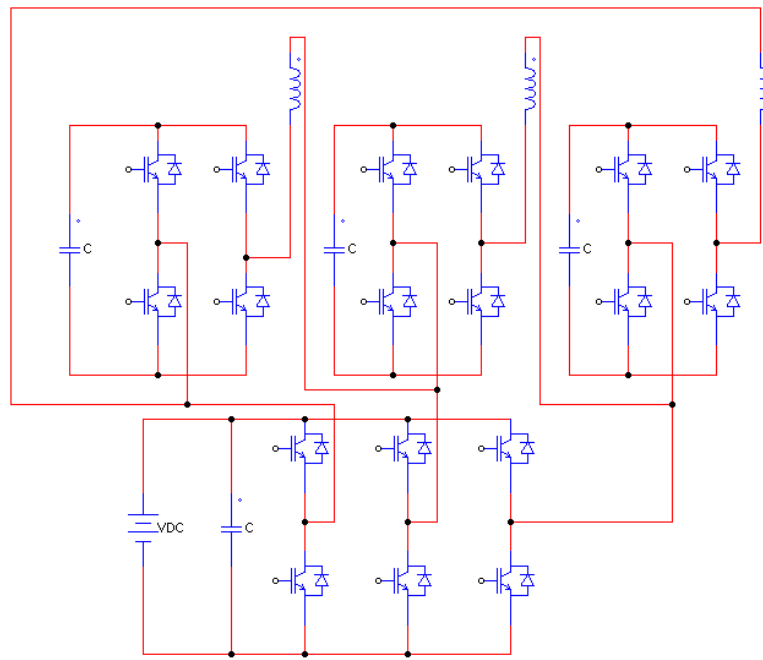


Figure 11. Equivalent circuit for full bridge MLI for 21 levels of output.

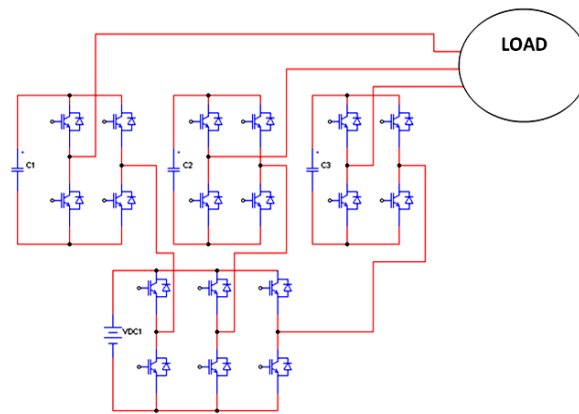
### 2.3. Hybrid Multilevel Inverter

The hybrid multilevel inverter is an amalgamation of symmetric and asymmetric inverter topologies. A novel hybrid MLI for drive applications was proposed in [17]. In this paper, the authors discussed a three-phase inverter in which each leg of inverter delivers two outputs for each single phase inverter and induction motor. This is capable of operating as three single-phase MLIs. The voltage levels are obtained by matching the capacitor voltages with that of  $V_{dc}$ . The circuit is given in Figure 12.



**Figure 12.** Hybrid three-phase multilevel inverter.

A similar topology was investigated by the researchers for a three-phase application [18,19]. In this topology, each leg is meant for a single phase and it was designed with an H-bridge in series with a DC voltage source. The circuit diagram for both the topologies is shown in Figures 13 and 14 respectively.



**Figure 13.** Circuit diagram for three-phase MLI.

An hybrid MLI based on switched capacitor technique is given in Figure 15. Here, a basic unit along with an H-bridge configuration is proposed for developing the positive, negative and zero voltages respectively. The magnitude of the voltage generated is given by

$$V_k = (5)V_1 \quad (9)$$

Due to the implementation of different voltage sources, it is 80 percent asymmetric in nature [20].

To overcome the drawbacks of utilizing more switches even for low-level inverters, a new hybrid cell technology was proposed by the authors in [21]. The high level of voltage was achieved with the

arrangement of multilevel VSIs (voltage source inverters). The number of DC voltage sources and switches required for the implementation of the topology are selected based on the following expression:

$$M = (P + 5)/2 \quad (10)$$

$$V_{ndc} = (P - 1)/2 \quad (11)$$

where P is the number of levels, M is the number of switches and  $V_{ndc}$  is the number of DC voltage sources. The circuit topology is as follows in Figure 16.

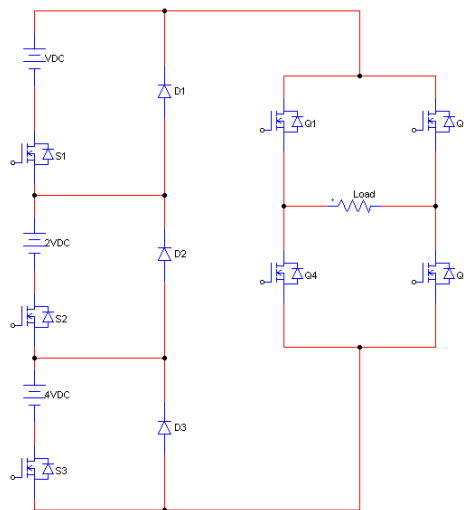


Figure 14. Circuit diagram for three-phase MLI.

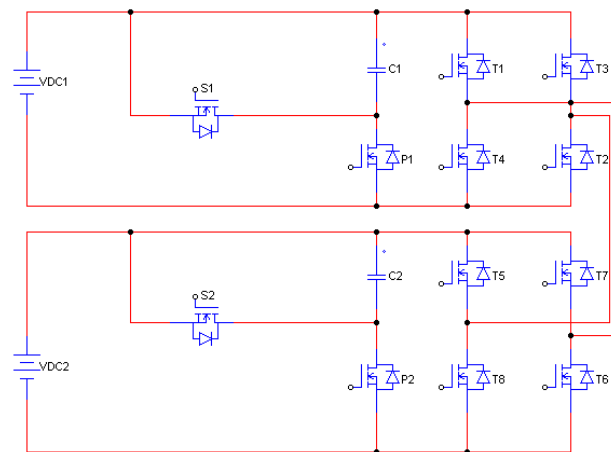


Figure 15. MLI based on switched capacitor.

A neutral-point clamp with floating capacitors capable of producing multilevel voltages is investigated in [22,23] and filed for patent (Efficiency and Dense Architecture: EDA5). The circuit configuration of the mentioned topology is shown in Figure 17.

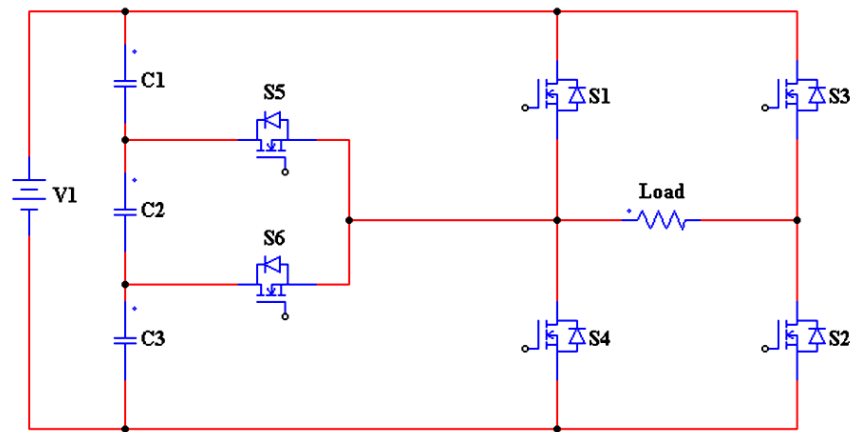


Figure 16. Circuit of hybrid cell technology for MLI.

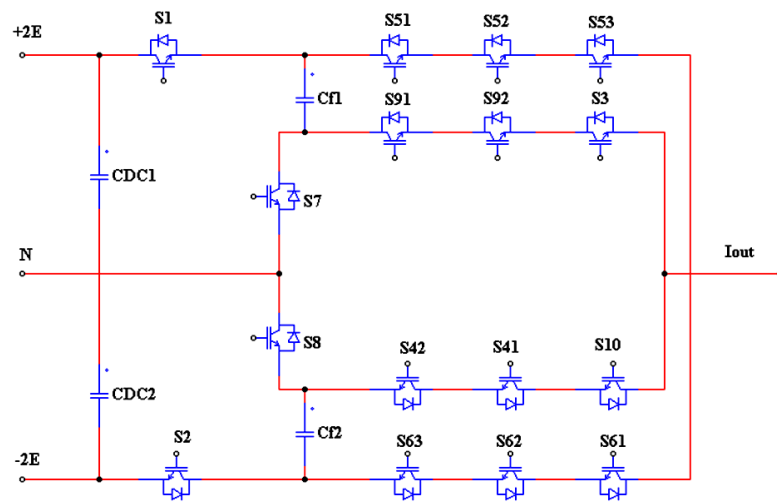


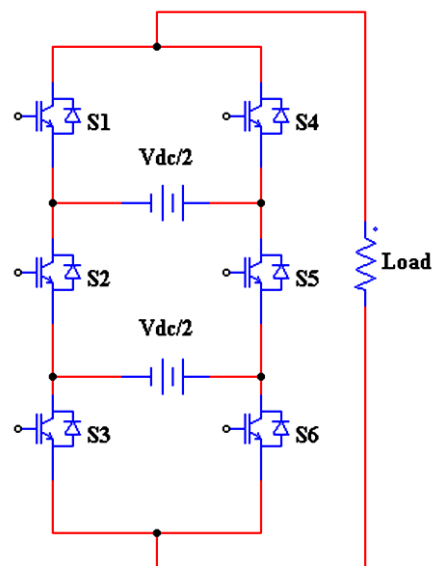
Figure 17. Circuit configuration for Neutral Point Clamped (NPC) type MLI.

### 3. Reduced number of Switches

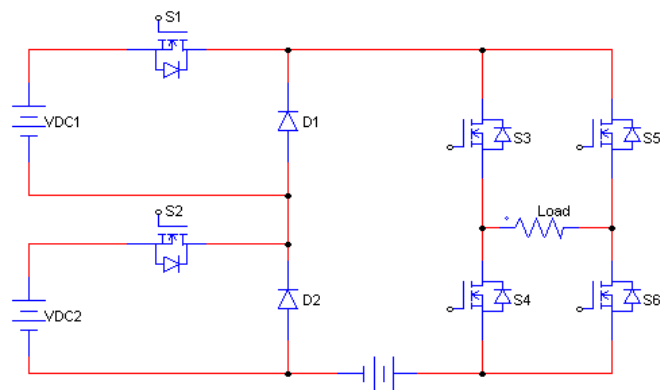
Some of the modified MLIs with minimum number of switches have also been discussed here in this literature. A new idea was proposed by the authors of [24] for producing very high levels of stepped voltage. This can act as a replacement for the conventional cascaded MLI with numerous switch counts. The suggested topology was tested for both symmetric and asymmetric configuration for a switch count of six, as shown in Figure 18.

A seven-level inverter made up of six power semiconductor devices is investigated by the authors of [25]. Both the performance and output rating of the inverter is maintained even though the switch count was reduced. The topology comprises of three DC voltage sources at the supply side and a full bridge circuit. It is a modification of the work implemented in [26], in which nine switches were used for obtaining a seven-level output. The circuit is given in Figure 19.

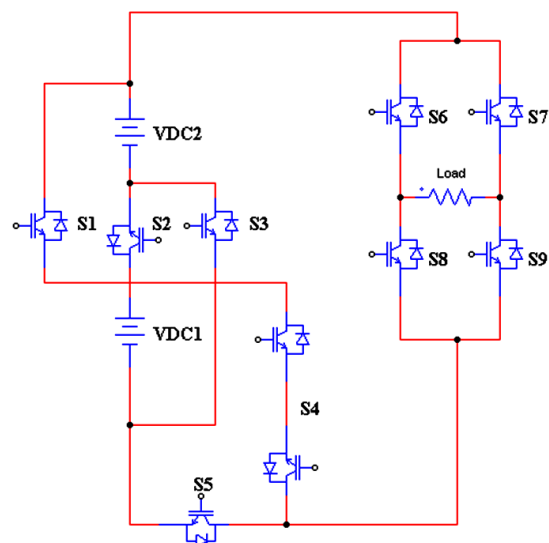
Apart from normal techniques, this paper has implemented a novel technique for MLI by combining the process of level generation and polarity generation. The general configuration consists of  $n$ -number of DC sources for generating  $3n$  levels of voltage at the output. The topology can be extended to higher levels of voltage by adding additional DC sources with the basic unit. The circuit for a nine-level inverter based on the above technique is shown in Figure 20.



**Figure 18.** Circuit for modified MLI with minimum number of switches.



**Figure 19.** Circuit for seven-level H-bridge inverter.



**Figure 20.** Nine-level inverter circuit.

The number of switches required for the inverter for a specific value of voltage can be determined using the following formula.

Number of switches:

$$(N_S) = 4m + 1 \quad (12)$$

where  $m$  is the number of DC sources [27].

Like the above-mentioned topology, another new technique has been discussed in [28] to eliminate the voltage imbalance and also to protect the false conduction. This is done by designing an MLI without any capacitors and diodes. The circuit topology given in Figure 21 proved to be the best in terms of switching losses and THD.

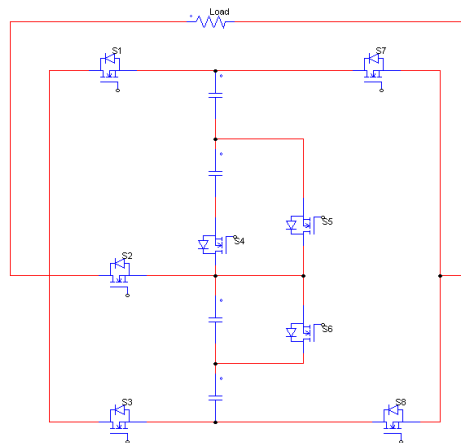


Figure 21. Multilevel inverter to reduce switching losses.

The switching losses can also be reduced by implementing a circuit configuration like that shown in [29]. It consists of nine switches and two DC voltage sources for generating a voltage signal at nine levels. Though the switch count is high when compared to the previous topologies, it is lesser in count than that of a conventional inverter for the same level of voltage. The circuit is given in Figure 22.

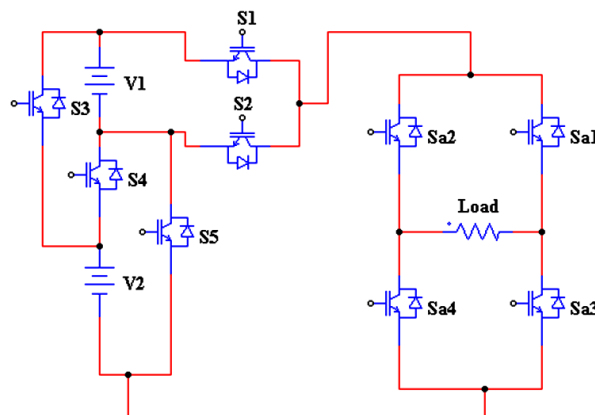


Figure 22. Reduced switch MLI circuit.

A symmetrical inverter with reduced switch count is implemented in [30]. This can be extended for higher voltage levels by adding the required number of voltages and switches.

The formula for calculating the number of switches is defined as follows:

$$N_S = m + 3 \quad (13)$$

$$N_L = 2N_S - 5 \quad (14)$$



where  $m$  is the number of DC sources in the symmetrical MLI.

The maximum value of voltage at the output end can be expressed as

$$V_o = nV_{dc} \quad (15)$$

The basic unit and the same topology for nine-level output voltage are given in Figures 23 and 24 respectively.

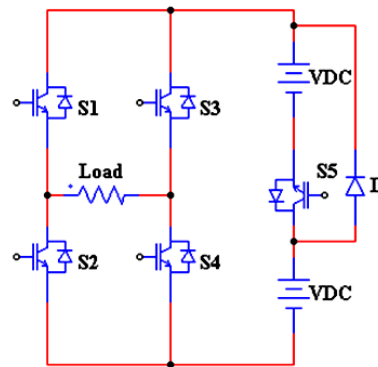


Figure 23. Basic unit and nine-level MLI.

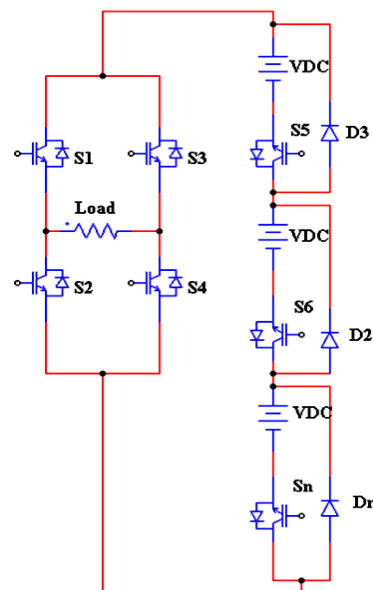


Figure 24. Basic unit and nine-level MLI.

Previously we have seen many topologies with reduced switch count and DC sources. In all the cases, as the number of level increases the switches and sources gets increased. This may lead to circuit complexity. To overcome this drawback, a novel design was implemented in [31], which generated the same number of voltage levels per phase with the help of only two batteries and eight switches. In this newly defined circuit, the number of devices and batteries reduced as the levels increased. The schematic is shown in Figure 25.

Similar to a neutral point clamp inverter discussed in the asymmetric section of this literature, a hybrid model combining a three-level NPC connected in series with a three-level H-bridge cells [32]. The general configuration of this topology is given in Figure 26. The bus voltage ratio is used to increase the voltage levels and also to optimize the switching losses of the device. The power distribution among the cells is improved with the hybridization technique. It also results in reduced switch count.

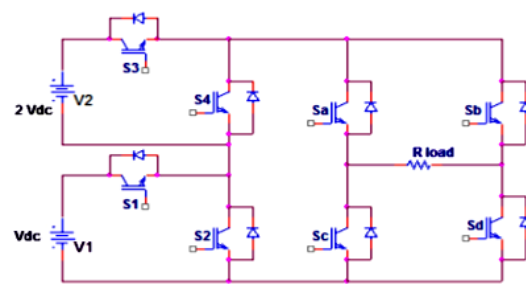


Figure 25. Novel reduced switch MLI.

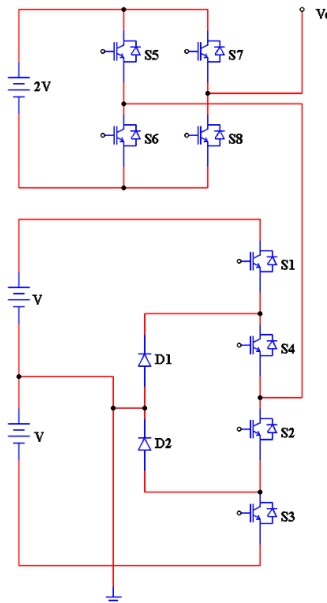


Figure 26. Generalized three-level NPC circuit.

Many research works have also been carried out in this area as discussed in [33,34]. The structure for both the topologies is shown in Figures 27 and 28 respectively.

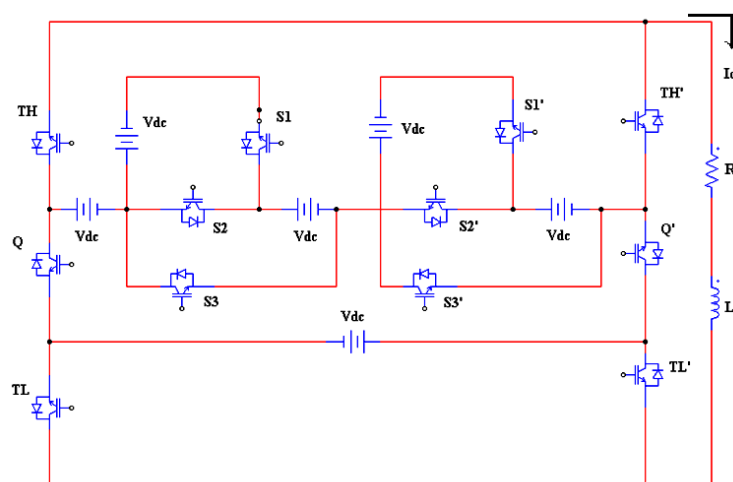


Figure 27. MLI circuit (symmetric mode).

One more configuration based on bidirectional and unidirectional switches is explained by the authors of [35,36]. In this paper, the authors used the CE (common emitter) configuration.

The unidirectional switches comprised one power device and one reverse diode which blocked the voltage in one polarity and makes the current flow through both paths. The same concept was applied for bidirectional switch configuration as well. The circuit configurations are shown in Figures 29 and 30 respectively.

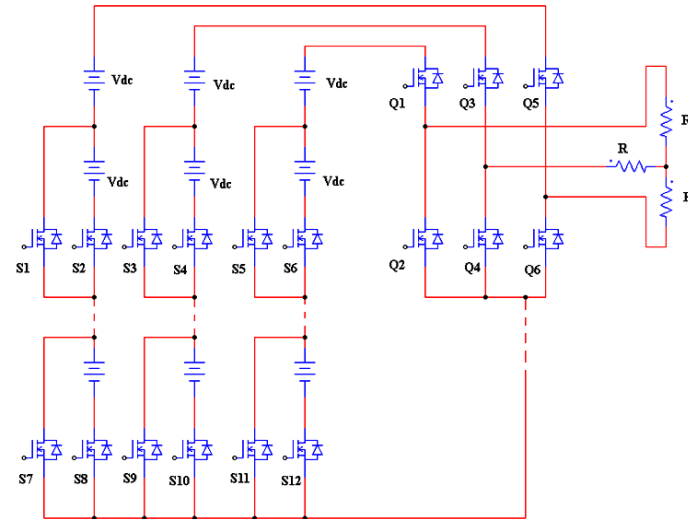


Figure 28. MLI circuit (asymmetric mode).

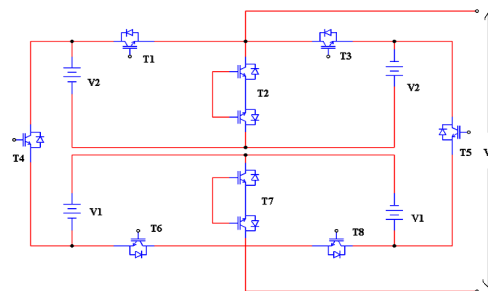


Figure 29. Bidirectional switch MLI circuit.

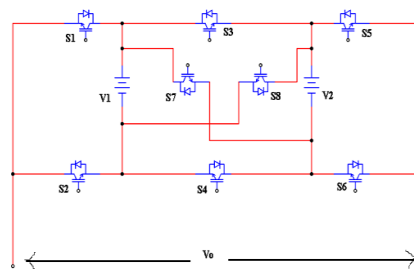


Figure 30. Bidirectional switch MLI circuit.

With the same concept, another paper proposed a structure based on the asymmetric structure which combined a reduced switch MLI and a cascaded MLI. The different levels of voltages were generated with a combination of unidirectional and bidirectional switches. The generated voltage had different paths since the sources were connected in different directions and it served as the major benefit of this topology [37]. The circuit topology is shown in Figure 31.

An overview of all the topologies discussed is given in the Table 1.

**Table 1.** Classification of MLI based on its number of elements and structure.

Paper Reference Number and Year	Type of Inverter	No. of DC Sources	No. of Switching Devices	Number of Diodes	No. of Voltage Levels	Voltage Gain and No. of Voltage Levels Formula	Switching Techniques	Limitations	Advantages
[4] & 2010	Symmetric	3	8	0	11	$V_{o,max} = n \cdot V_{dc}$	Carrier redistribution (CR) technique	-	A new algorithm has been proposed for the generation of maximum voltage without losing any level in output voltage waveform.
[5] & 2013	Symmetric	4	5	0	7	$\square = (2 \times * \square - 3)$	Carrier based PWM technique	Fails to determine suitable PWM technique	Lower THD level
[11] & 2016	Symmetric	4	7	3	9	-	Multicarrier PWM technique	It cannot be implemented for medium to high voltage application	Cost is very low for designing the same level of voltage when compared with conventional method
[11] & 2016	Symmetric(modified)	4	10	2	9	-	Multicarrier PWM technique	The values of dc sources get increased proportionally in the range of '5:1' for all 'k' number of cells.	It is applicable to wide range of voltage applications
[12] & 2013	Asymmetric	2	8	0	7	$V_{o, max} = (2N+1-1)V_{dc}$	Level Shifted PWM technique	Unique filter design is required to reduce harmonics	Lower THD level
[13] & 2016	Asymmetric	2	10	2	7	$(P1/P0) = (V1/Vo)$	On/OFF control	Proper PWM technique is not implemented	Suitable for medium power application such as PV, fuel cell, and battery application
[14] & 2016	Asymmetric cascaded MLI	6	12	0	7	$M = A_m/(A_c(k-1))$	Multicarrier PWM technique	Number of switches are high	It can be utilized in crucial industrial applications.
[16] & 2017	Asymmetric	4	12	0	21	-	Multicarrier PWM technique	Proper voltage balancing is required	Requires less number of devices
[17] & 2012	Hybrid	1 (along with 4 capacitors)	18	0	9	-	SPWM technique	Complex control strategy	The capacitor voltage of single phase inverters are regulated by a sliding mode control
[18] & 2012	Hybrid	1 (along with 4 capacitors)	18	0	9	$L_{ph} = 2N_{inv} + 1$	Fundamental switching scheme	No modification has been made in carrier or modulating signal	Need for large inductor is eliminated
[19]	Hybrid	3	7	3	9	$V = 2S - 1 \cdot V_{dc}$	Not defined	Proper PWM technique is not implemented	Produces high number of levels with less number of switches
[20] & 2015	Hybrid	2	12	0	25	$V_k = (5 \text{ ki}1) V_1$	Symmetrical Step Control Method & Fundamental Switching Frequency Scheme	Symmetrical step control does not give efficient results	THD is low while using fundamental frequency technique
[21] & 2016	Hybrid	1 (along with 3 capacitors)	6	0	7	$V_{ndc} = (N - 1)/2$	Hybrid Modulation	-	THD is 3.21%
[24] & 2017	Reduced Switch MLI	2	6	0	7	-	Not defined	Proper PWM technique is not implemented	The conversion efficiency of the converter increases because of less number of switches.
[26] & 2014	Reduced Switch MLI	3	9	0	7	-	Multicarrier APOD technique	-	Reduced switch count
[27] & 2019	Reduced Switch MLI	2	9	0	9	$kV_{dc}$	Phase disposition	Complex control strategy	Utilization of a novel converter using voltage multiplier concept reduces the DC source count.
[28]	Reduced Switch MLI	4	8	0	9	-	Phase Opposition Disposition	-	Minimized THD and Switching losses
[30]	Reduced Switch MLI	1	5	2	11	$V_o = nV_{dc}$	Multicarrier based level-shift PWM	-	Reduced Power loss
[31]	Reduced Switch MLI	2	8	0	9	$V = V_1 + V_2$	Not defined	Proper PWM technique is not implemented and filter design is required to reduce harmonics	Reduced switch count
[38] & 2016	Reduced Switch MLI	1	9	2	9	-	High Frequency Modulation	Complex control strategy	THD is low and the voltage stress on the power switches in the back-stage is relatively relieved

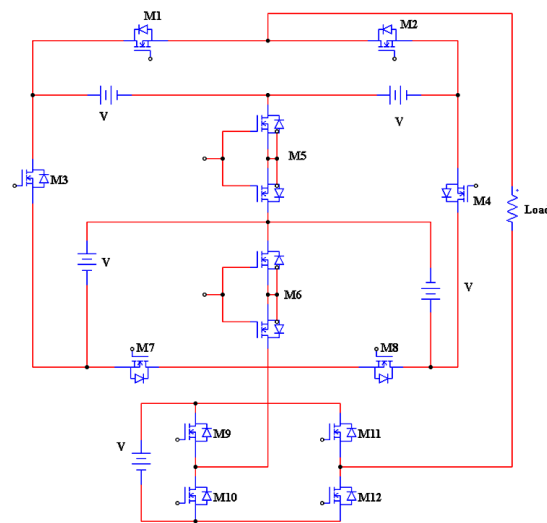


Figure 31. Circuit configuration for asymmetric MLI.

### 3.1. Multilevel Smart Inverter

A multilevel inverter (MLI) can act as a smart inverter by making some changes in the control system of the inverter topology. A modified hybrid multilevel inverter with less switches was proposed in [38]. In order to make the inverter a smart device, IoT was employed for its control. Initially, the parameters of the inverter were scrutinized with the help of IoT widgets and settling measures. The parameters that are not comparable (inactivity of packages) were combined together and separated from the IoT gadget and the rest of the parameters were given to the goal gadget. This helped to find the change probabilities for the associations. The overall system is given in Figure 32.

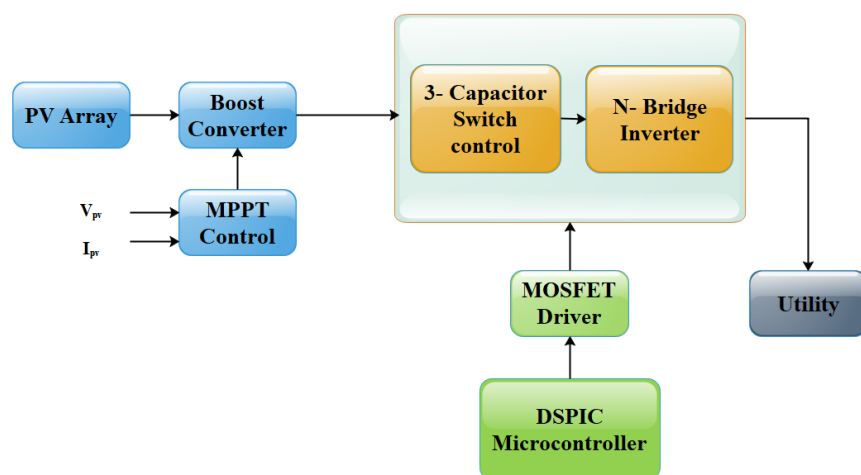


Figure 32. Block diagram for multilevel inverter circuit.

A novel MLI configuration was analyzed in [39–41]. It delivers a nine-step output voltage with high voltage gain. It consisted of a developed switched capacitor circuit (DSCC) at the source terminal of the inverter and another circuit was a conventional H-bridge circuit. The H-bridge circuit connected at the end terminal of the inverter produced the negative sequence of voltage levels at the output. The circuit of multilevel inverter is given in Figure 33.

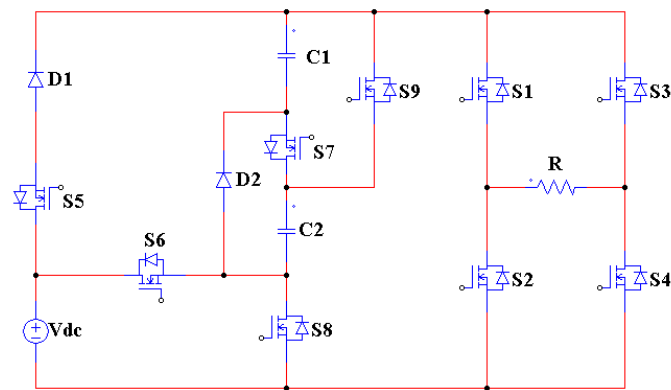


Figure 33. Circuit diagram for nine-level Inverter.

To maintain a high voltage profile, an intelligent control technique can be used to control the operations of the multilevel inverter. Another topology of MLI was discussed in [42]. In this paper, the authors have implemented a circuit by integrating a full bridge inverter and combination of switched DC sources [43]. The generalized circuit diagram of the above-mentioned hybrid MLI is shown in Figure 34.

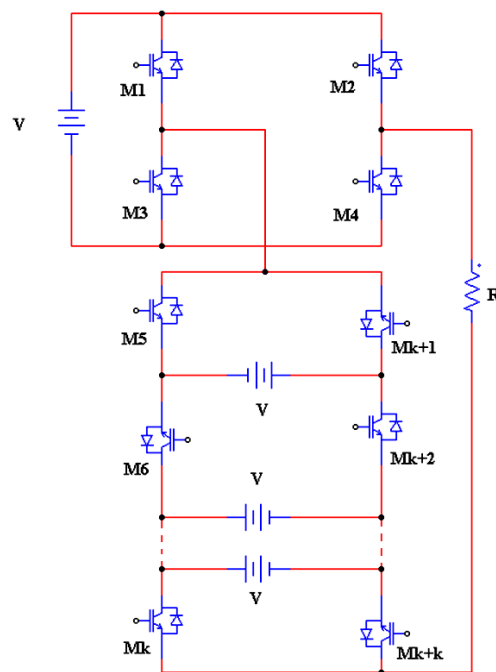


Figure 34. Circuit diagram for hybrid MLI.

This hybrid configuration can be extended to high number of output voltage levels by adding corresponding switches and DC sources. The SDCS design operates in asymmetric manner in order to increase the voltage level at output side.

### 3.2. PWM Techniques for MLI

Numerous research works are being carried out on multilevel inverters by several researchers in the field of power electronics. In order to switch these inverters, various modulation techniques are used. Among all those types, carrier based and space vector modulation techniques are most commonly used.

For a multilevel inverter, the modulation techniques such as single-carrier sinusoidal pulse width modulation (SCSPWM) and subharmonic PWM (SHPWM) can be used. Between the two categories, subharmonic PWM is an exclusive control strategy for multilevel inverters. The further classifications of SHPWM techniques are the phase-shifted carrier PWM method (PSPWM) and the carrier disposition PWM methods.

In the carrier disposition method, the multicarrier waveforms are obtained with the implementation of any one of techniques discussed below:

- phase disposition (PD);
- phase opposition disposition (POD);
- Alternative Phase Opposition Disposition (APOD).

For instance, an  $m$ -level MLI using a level-shifted multicarrier modulation scheme requires  $(m - 1)$  triangular carriers, all having the same frequency and amplitude [44,45].

### 3.3. Phase Disposition Method

In the phase disposition (PD) method, all carriers are selected within the same phase. With reference to the related research works in this field, this method results in low THD at higher modulation indices than the other schemes [46]. The simulated waveform in the MATLAB/Simulink software for carrier waves and reference signals is shown in Figure 35.

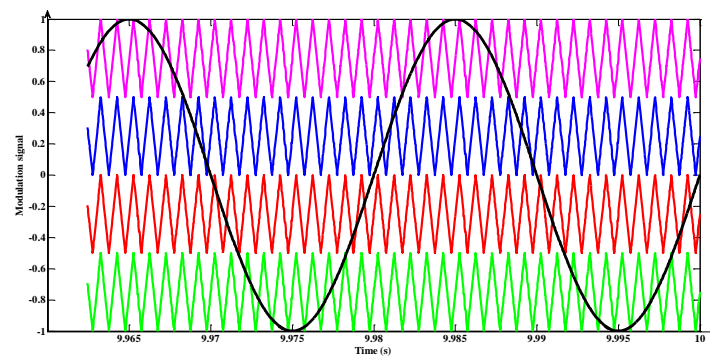


Figure 35. Waveform for phase disposition.

### 3.4. Phase Opposition Disposition

In this method, there is no harmonic at the carrier frequency and its multiples and the diffusion of harmonics occurs in that region [47]. The simulation of the POD technique was carried out in MATLAB/Simulink environment and waveform is shown in Figure 36.

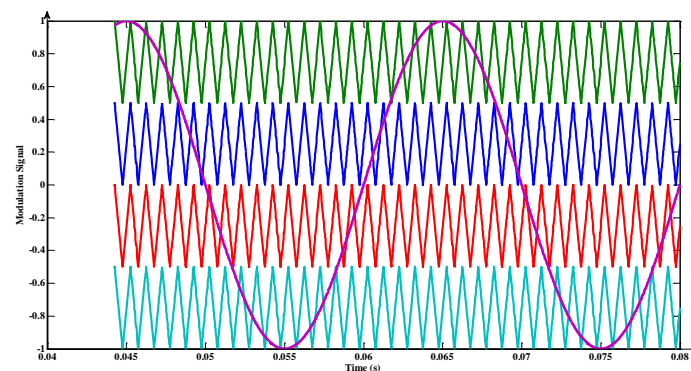


Figure 36. Waveform for phase opposition method.

### 3.5. Alternate Phase Opposition Disposition

In this method, each carrier signal is shifted by 180 degrees in phase from the other signal. This method gives almost the same results as the POD method but the only difference is that the triple-n harmonics are eliminated due to the cancellation of line voltages [48,49]. The simulation of the APOD technique was carried out in MATLAB/Simulink environment and waveform is given in Figure 37.

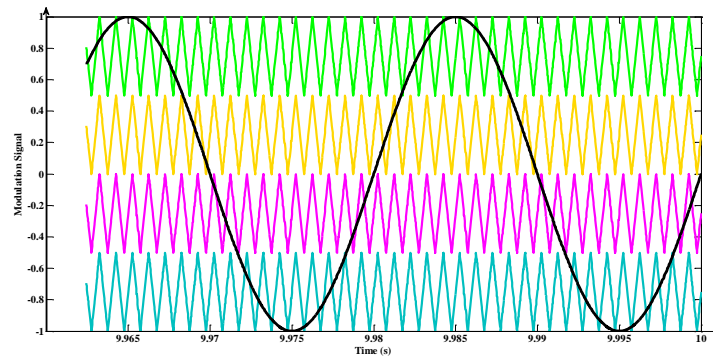


Figure 37. Waveform for alternate phase opposition method.

### 3.6. Multilevel Carrier PWM Technique

The conventional multilevel carrier PWM is capable of comparing several carrier wave signals with a single reference signal per phase. For a p-level inverter, p-1 carriers with the same frequency and amplitude are used. The authors have explained a novel PWM technique in which the carrier signals are disposed alternatively [50]. The waveforms for both conventional and modified multilevel PWM signals are shown in Figures 38 and 39 respectively.

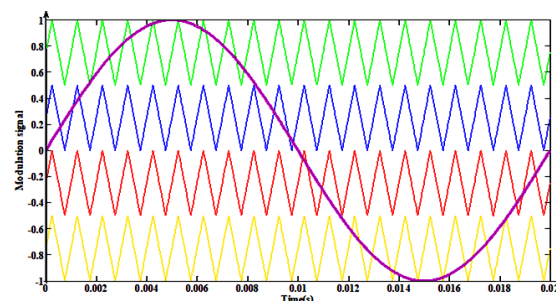


Figure 38. Conventional PWM signal.

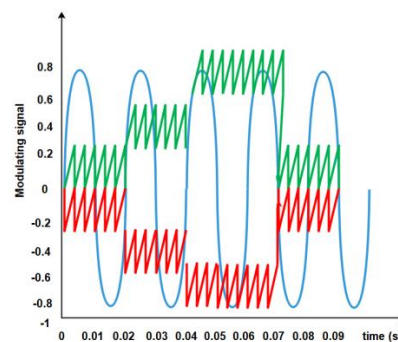


Figure 39. Modified PWM signal.

A hybrid-PWM technique was discussed in [51] using multiple carriers. This technique is a hybrid between the carrier-disposition PWM and the phase-shifted PWM. The carriers are shifted



both vertically and in phase in order to produce a pulse [52]. Thus, it includes the features of both the techniques. The waveform is shown in Figure 40.

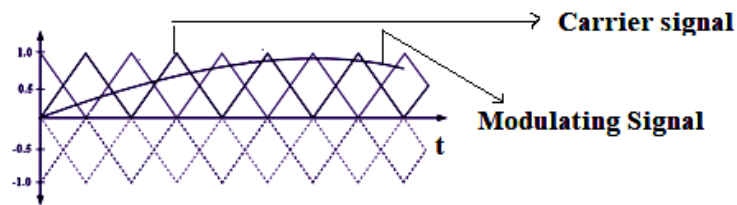


Figure 40. Waveform for hybrid PWM technique.

Another hybrid modulation technique is investigated in [53]. The authors have explained a PWM technique with the hybridization of the fundamental frequency modulation (FPWM) and multiple sinusoidal modulations (MSPWM) techniques. The generated wave has reduced switching loss as in the case of FPWM and also delivers as good harmonic characteristics as that of a MSPWM method. This hybrid modulation scheme is integrated with sequential switching and simple base PWM circulation scheme in order to balance the power dissipation among the power modules.

### 3.7. Depenbrock's Discontinuous PWM Technique (DPWM)

This is a discontinuous PWM technique in which a zero-sequence signal is injected to a sine wave [54,55]. This kind of signal is termed as Depenbrock's discontinuous PWM technique. The waveform for single-phase and three-phase Depenbrock's PWM is shown in Figures 41 and 42 respectively.

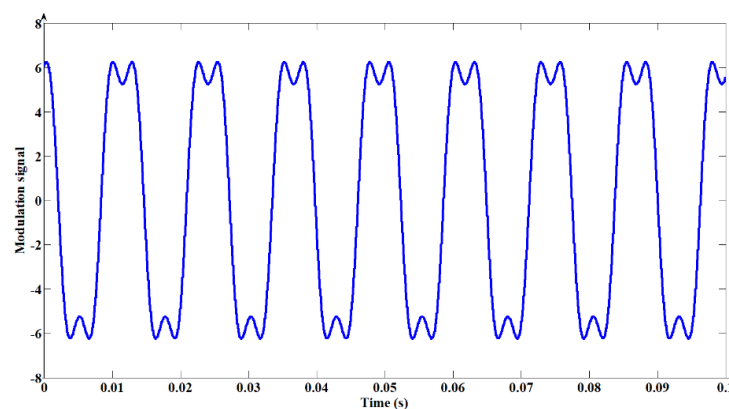


Figure 41. Depenbrock's PWM-1 phase waveform.

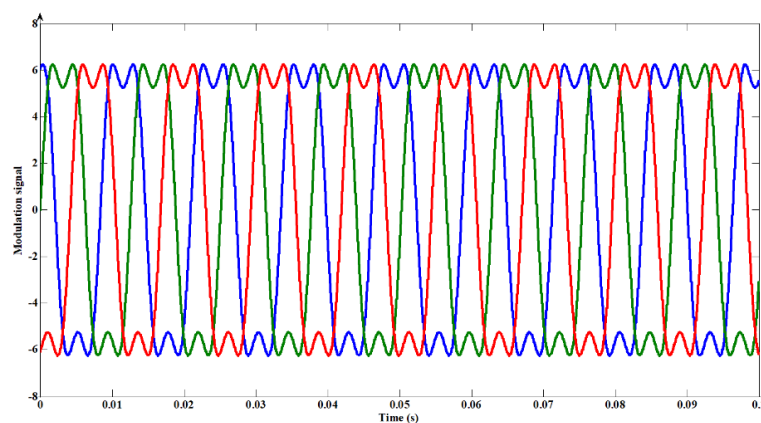


Figure 42. Depenbrock's PWM-3 phase waveform.

### 3.8. Selective Harmonic Elimination (SHE)

The purpose of the SHE-PWM technique is to get rid of certain lower order harmonics [56–59]. Other than triple-n harmonics (since they are getting eliminated naturally in three-phase applications), the remaining order of harmonics can be removed by means of proper filter. But the drawback in SHE is that it cannot obtain solutions for non-linear equations easily. Therefore, certain optimization techniques have to be implemented. The model waveform for the SHE method is shown in Figure 43.

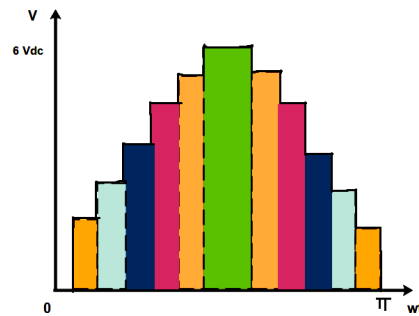


Figure 43. Model waveform for Selective Harmonic Elimination (SHE) method.

### 3.9. Space Vector PWM Technique

In the space vector modulation technique, the reference vector is approximated by switching among the nearest voltage space vectors [60–65]. The steps involved in the implementation of SVPWM are [66–68].

- Identification of each sector;
- Proper switching of voltage space vectors has to be determined;
- The duration of each voltage space vectors in the switching sequence should be identified;
- Determination of an optimum switching sequence.

To determine the operating sector a fractal-based technique was discussed by the authors in [69]. A fractal scheme based on a 60-degree-coordinate SVPWM was implemented in order to reduce the computational complexity. A multilevel inverter (five-level) in a  $60^\circ$  coordinate system is shown in Figure 44.

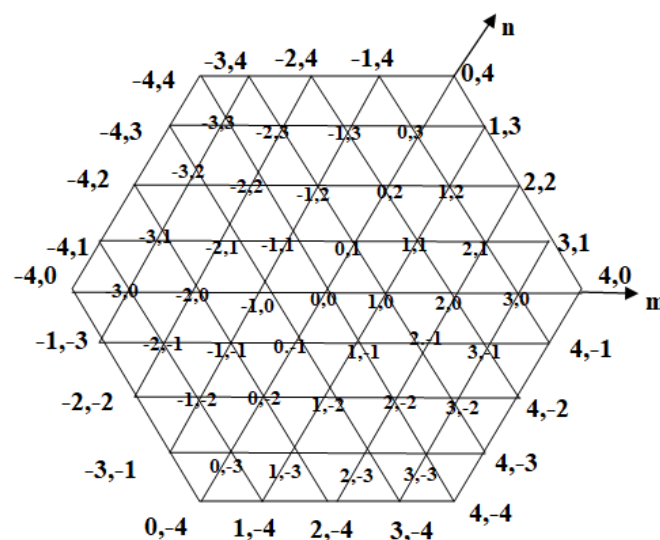


Figure 44. Sixty-degree coordinate system for five-level inverter.

A similar topology was discussed in [70] where the same two coordinate systems were implemented. The vector diagram for the 60-degree SVPWM of this topology is shown in Figure 45.

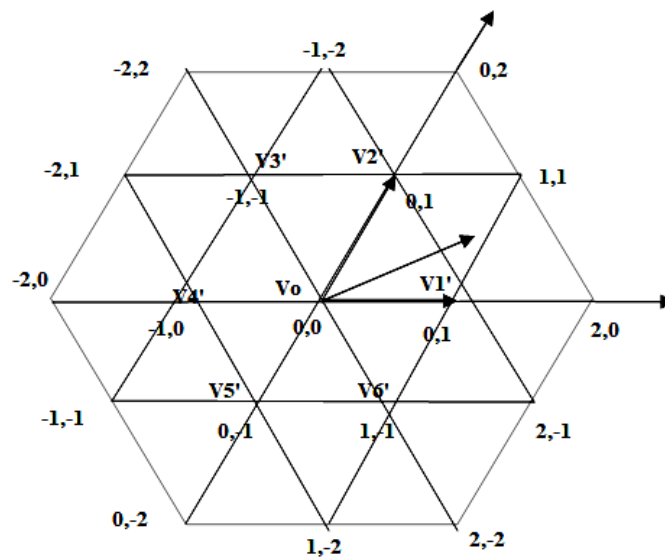


Figure 45. Sixty degree Space Vector Pulse Width Modulation (SVPWM) technique.

Several other SVPWM topologies were discussed [71–77] by the researchers for three-level inverters and higher levels.

### 3.10. FPGA Based Modulation Technique

A novel technique based on FPGA control was proposed in [78]. It proved to be the best in improving the modulation index range and also the power quality. The control block for PWM generation using FPGA is shown in Figure 46.

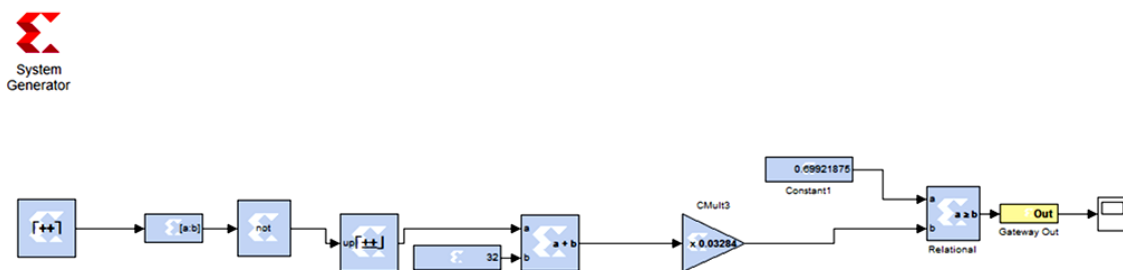


Figure 46. Control using FPGA.

### 3.11. Area Integration PWM Technique

This is a newer scheme explained by the authors in [79] for the generation of PWM pulses. It involves evolutionary programming (EP) for optimizing the pulse width [79]. The basic idea behind this technique is the integration of total area of the pulses with a sine region. Thus, it is named the area integration PWM (AIPWM) technique. The basic idea for a seven-level output with six pulses per half cycle using this AIPWM method is shown in Figure 47.

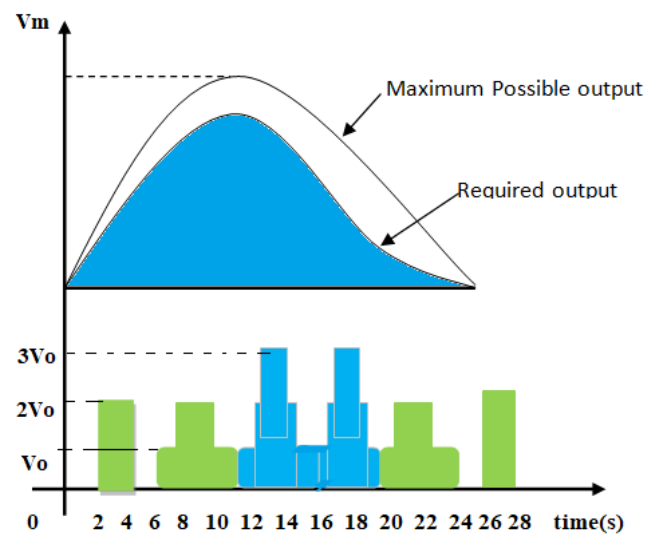


Figure 47. Basic schematic showing Area Integration Pulse Width Modulation (AIPWM) technique.

#### 4. Special Topologies of MLI

##### 4.1. Switched DC Source MLI

A new topology of MLI with alternate DC sources linked on the opposite polarities was designed by the authors in [80]. This kind of arrangement reduces the number of power semiconductors, which are responsible for generating multilevel output. This topology can be used in medium-voltage drive applications in order to provide isolated DC sources. It is mainly applicable to battery-powered applications (such as electric vehicles and submarine propulsion). The general structure is shown in Figure 48.

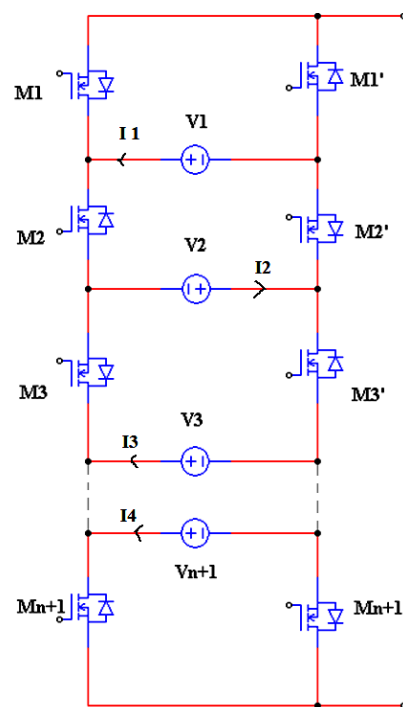


Figure 48. Circuit diagram for switched DC-source MLI.

#### 4.2. Reverse Connected Voltage Source MLI

The reverse connected topology was discussed by the authors for MLIs starting with five-level voltages in [81]. An H-bridge configuration with four main switches and a single voltage source acts as the main circuit. One leg of the main circuit had complementary switches and reverse-connected voltage sources. To extract N-level output voltage,  $N + 3$  switches had to be used. The circuit topology is shown in Figure 49.

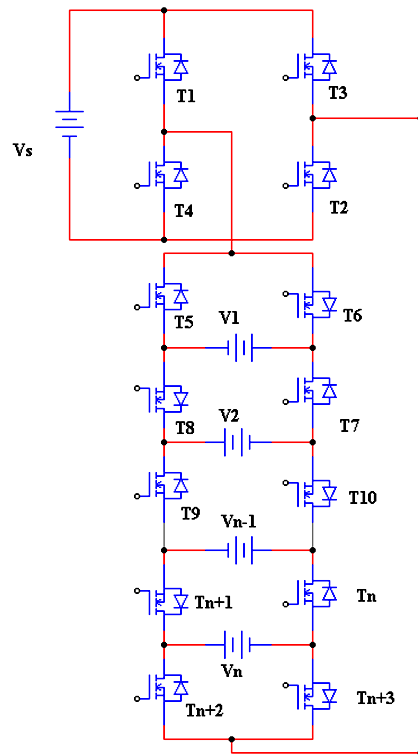


Figure 49. Reverse connected voltage source MLI.

#### 4.3. Implementation of MLI Using LM350 Voltage Regulator

A five-level inverter using an LM350 voltage regulator was implemented in [82] for low power applications, typically in the range of 30 W. With reference to the data sheet of LM350, the parameters were chosen for the design of inverter. The different values of output voltages were obtained by adjusting the terminals of the LM350 IC where the series biasing resistors were also connected. A microcontroller is employed for the proper selection of resistor. The desired values were generated by operating the inverter using a control program. The concept is explained with the help of a block diagram shown in Figure 50.

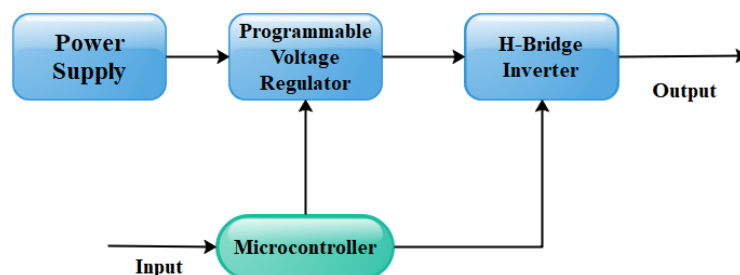


Figure 50. Block diagram for concept of MLI using LM350.

#### 4.4. Hardware Implementation of Cascaded Seven Level Inverter

The hardware prototype was implemented for a conventional cascaded seven-level inverter at R&D Power Electronics Laboratory of SEEE, at SASTRA Deemed University and the readings were noted. The overall circuit comprised several H-bridge inverters, which were connected in series to provide a sinusoidal output voltage. The inverter was divided into number of cells associated with an H-bridge in each cell and the voltage could be obtained by adding the values of voltage generated by each cell. For example, if there are  $k$  cells in an H-bridge multilevel inverter then the number of output voltage levels was  $2k + 1$ .

Cascaded inverters are more advantageous when compared to other two conventional types as they require fewer components than the other configurations. This results in weight and cost reduction of the overall system. Figure 51 shows a  $k$  level cascaded H-bridge inverter.

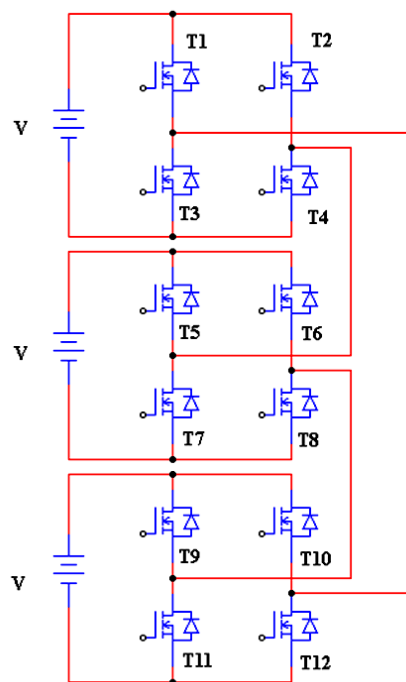


Figure 51. Circuit diagram for cascade H-bridge inverter.

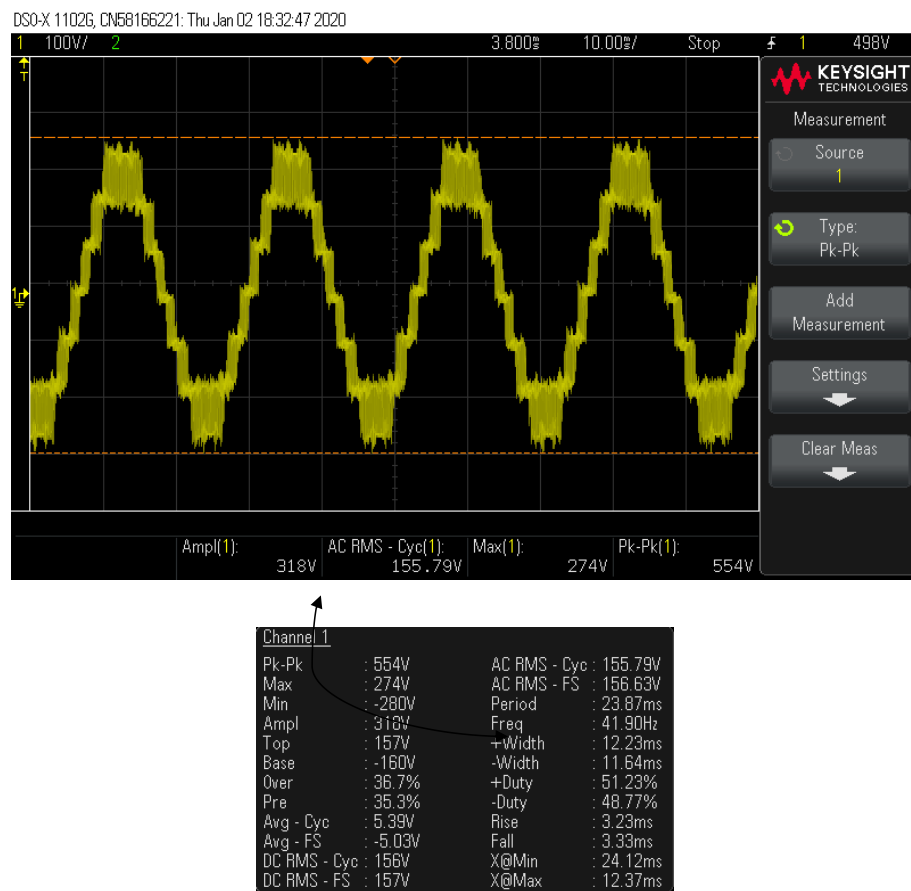
The cyclone IV FPGA controller was employed in the control unit of multilevel inverter. The hardware was set up and configured in the R&D lab at SASTRA Deemed University, India for the circuit topology shown in Figure 52.

The inverter operated under open-loop and closed-loop conditions with a motor load at the speed of 1300 rpm. In order to measure the voltage, a set of lamps was connected across a phase and the readings were noted. The generated waveforms for the output voltage under open-loop and closed-loop conditions were shown in Figures 53 and 54 respectively.

From Figures 53 and 54, it can be clearly observed that the inverter generated seven levels of output at a maximum of 274 V and 254 V respectively.



**Figure 52.** Hardware setup for seven-level cascade inverter at Shanmugha Arts, Science, Technology & Research Academy (SASTRA).



**Figure 53.** Output voltage waveform under open loop condition.

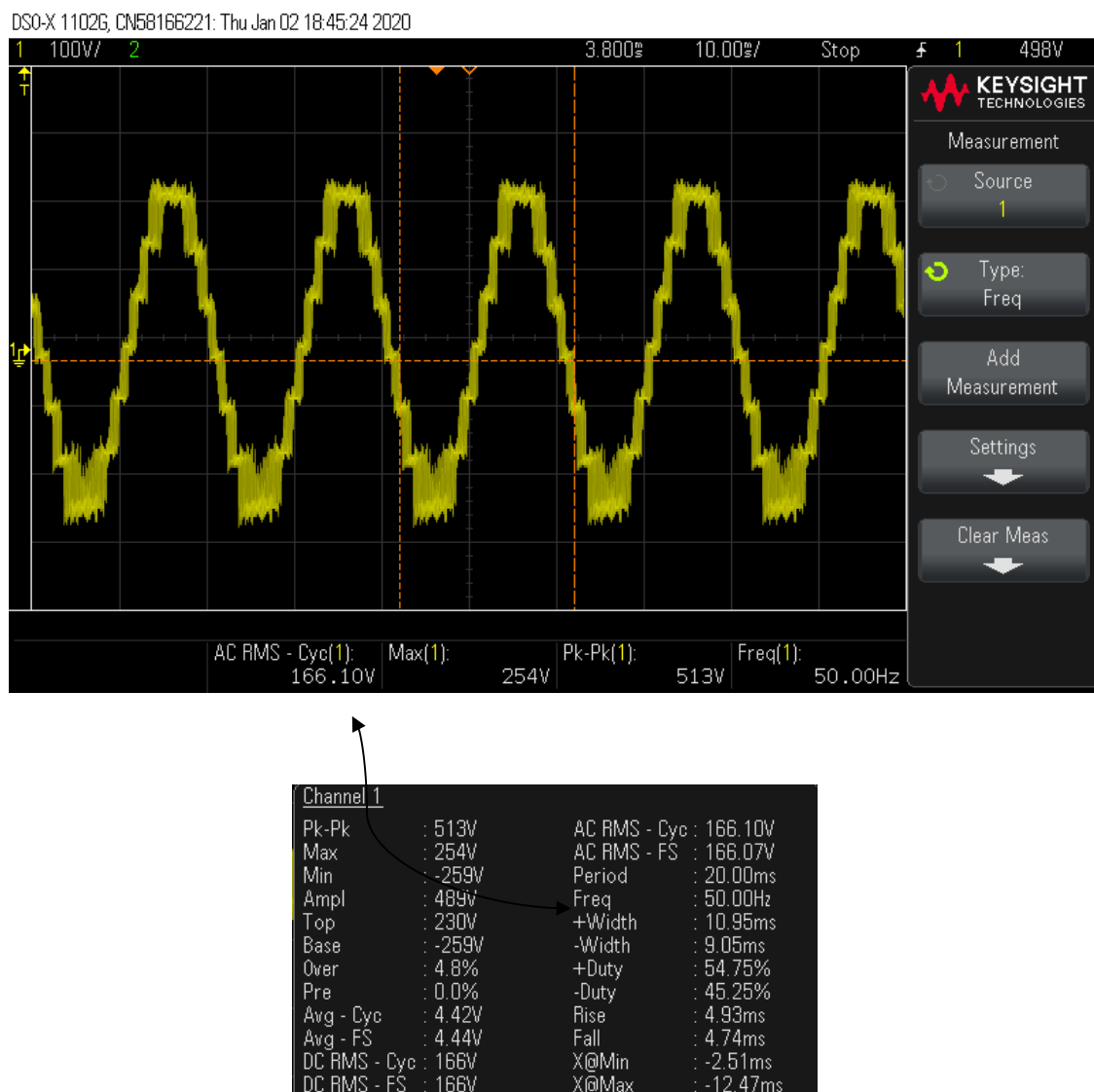


Figure 54. Output voltage waveform under closed loop condition.

## 5. Conclusions

Multilevel inverters have become one of the major devices in the field of power electronics since they can be used for both high-power and high-voltage applications. The multilevel inverter has more benefits too, such as high resolution, low modularity, reduced switch count for higher levels of voltage and in terms of its control mechanism. This work has been carried out in such a way that it covers the different configurations based on its structure and number of devices, the modulation techniques and some special methodologies for using MLI in a unique manner with certain modifications over the other versions. This review will serve as a point of reference for researchers those who are working in this field.

**Author Contributions:** S.P.S. performed the review under the guidance and direction of S.S.R. and S.N. who devised the idea. All three authors analyzed the data and contributed towards the review. S.P.S. wrote the paper and executed the experiments under the guidance and supervision of S.S.R. and S.N. All authors have read and agreed to the published version of the manuscript.

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**Conflicts of Interest:** The authors declare no conflict of interest.

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