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Study on Operational Characteristics of Protection Relay with Fault Current Limiters in an LVDC System

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Abstract: As the application of low-voltage-direct-current system increases, fault analysis in the low-voltage-direct-current system has essential because the fault response has different from the conventional AC distribution system. Especially, the fault current by the discharge current of the capacitor in the low-voltage-direct-current distribution system has very large compared with the conventional AC distribution system. Therefore, this paper proposed the application of the superconducting fault current limiter for limiting the fault current on the low-voltage-direct-current system. As one of the protected methods against fault current, the superconducting fault current limiter which could quickly limit the fault current has been noticed as an attractive method. However, the protection relay may malfunction such as over current relay, selective protection relay due to limiting fault current by applying superconducting fault current limiter. Therefore, in this paper proposed a solution to malfunction problem of the protection relay using the voltage components of the high temperature superconductivity. This paper verified the effect of the proposed method through test modelling and PSCAD/EMTDC .

Keywords: low voltage direct current (LVDC); micro-grid; superconducting fault current limiter (SFCL); protection relay; over current relay; selective protection relay

1. Introduction

Micro grid has been in the spotlight for the efficient operation of distribution generation such as photovoltaic (PV) and energy storage systems (ESS) and for improving the reliability of the system. The low voltage direct current (LVDC) system for the efficient topology of the micro-grid is being used to meet the lofty goal of sharing distribution generation [1,2].

As the LVDC system has a different configuration from the AC system, the analysis of fault response should be necessary for protecting the system component. In particular, the LVDC system has a fatal problem in which the fault current sharply increased due to the discharge current of the capacitor [3,4]. Therefore, many studies have been conducted to limit the fault current on the LVDC system.

First of all, to understand the fault characteristics of the LVDC system, many studies focus on the fault response [5–7]. Also, since the LVDC system did not exist zero crossings, other studies have been

conducted on the DC circuit breaker or insulated gate bipolar transistor (IGBT) isolation switches [3,8–10]. Reference [11] analysed the stability of applying a circuit breaker using a superconducting fault current limiter (SFCL) for protecting a DC system. However, for economic or bulky structure reasons, the DC circuit breaker was difficult to install on the LVDC system. Therefore, methods for limiting fault current have been studied. In order to limit the fault current, conventional methods were analysed by increasing the line impedance or changing the capacity of the capacitor on the DC-link [12–15]. However, these methods result in increased line losses or adversely affected the LVDC system. Reference [16] proposed a modular multi-level converter (MMC) based process for limiting fault current in DC systems. However, the MMC based method is not suitable for LVDC system. Reference [17] demonstrated to achieve the self-acting fault current limitation and protect the grid voltage using fault current limiting (FCL) and superconducting cable (SC). References [18–21] analysed the results of the positioning on the SFCL and its effects on limiting the fault current. The SFCL has more effective than other methods to protect the LVDC system against fault current. Reference [22,23] analysed the fault characteristics and protection of the DC distribution system with SFCL. Reference [24] proposed design method for limiting fault current which is weak point in the DC system. These studies confirmed that the SFCL is an effective method for limiting the fault current on the LVDC system. However, conventional studies only analysed the limiting effect of the fault current by applying SFCL. The problem caused by limiting fault current was not analysed. In order to effectively apply the SFCL to the LVDC system, a solution to solve the problem should be proposed.

This paper proposes the application of the SFCL to limit the fault current on the LVDC system. When the SFCL was applied to the LVDC system for limiting fault current, protection relay such as over current relay and selective protection relay was affected. The over current relay determines the timing of the trip signal according to the magnitude of the fault current. Therefore, as the fault current is limited, the timing of the trip signal on the over current relay is delayed [25,26]. In addition, the selective protection relay considered in this paper is affected because it detects the fault using the pole of the derivative on the fault current [27]. Therefore, this paper analysed the operational characteristics of the protection relay according to limiting the fault current. Also, this paper proposed a solution for the protection relays that have a problem with malfunction or timing delay of the trip signal. The method proposed in this paper solved the malfunction of the over current relay. Also, the selective protection relay improved the performance to detect the fault quickly by using the method proposed in this paper. The effect of the proposed method in this paper was verified by PSCAD/EMTDC .

Section 2 describes the modelling of the LVDC system and the SFCL respectively. Section 3.1 describes the fault response on the LVDC system. Section 3.2 verifies the effect of limiting fault current by applying the SFCL. Sections 3.3 and 3.4 is analysed the problem caused by limiting fault current and proposed a solution for properly operational characteristics on the protection relay. Section 4 is discuss about this paper. Section 5 is conclusion.

2. Simulation Modelling

2.1. Low Voltage Direct Current (LVDC) System

Section 2.1 describes the modelling of the LVDC system. As shown in Figure 1, the LVDC system has connected to the AC system through the rectifier. Also, the PV system and the DC load have connected in the LVDC system through the DC/DC converter. The voltage of the LVDC system has composed bipolar 750 [V].

This paper focuses on analysing the trip signal of the protection relay, so the model of the circuit breaker used in Figure 1 could be opened immediately after receiving the trip signal on the protection relay.

In this paper, the protection relay for fault detection has consists of the over current relay and selective protection relay which have mainly used in the LVDC system [13,27–29].

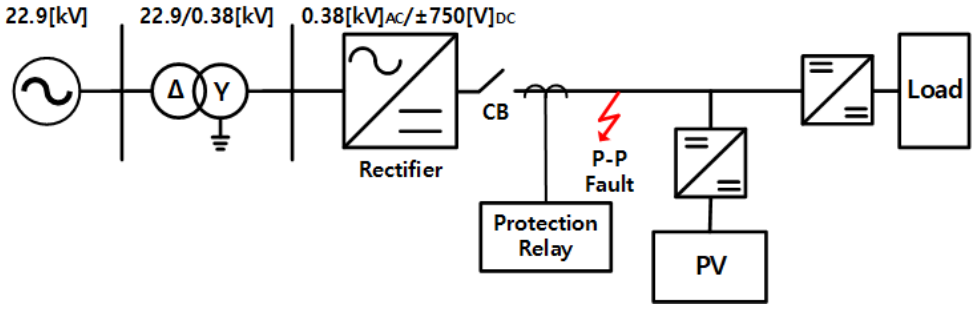

Figure 1. Modelling of low voltage direct current (LVDC) System.

Table 1 shows the parameters used in the LVDC system modelling in Figure 1. The small-capacity transformer at the front position of the PV and load was not shown in Figure 1. Also, power supply from the AC system to the DC system was not limited by the transformer capacity. The profile of the PV and load did not have a significant effect on the fault analysis because the fault analysis of the DC system was transient (under 0.02 [s]). Table 2 shows the fault scenario for the analysis of the fault response and the operational characteristics of the protection relay in the LVDC system. The fault was simulated by a short-circuit fault between positive-pole and negative-pole. The simulation factors such as measurement time of the protection relay and the operation signal of the circuit breaker are assumed to be ideal.

Table 1. Parameters of LVDC system .

Classification	Parameter
Photovoltaic (PV)	50 [kW]
Load	100 [kW]
Transformer	22.9/0.38 [kV], 1 [MVA]
Line Impedance	3.48 + j7.44 [%/km]

Table 2. Fault Scenario.

Classification	Parameter
Fault Start Time	0.5 [s]
Fault Duration Time	0.1 [s]
Fault Type	P-P Fault (Positive-to-Negative)
Fault Resistance	0.01 [ohm]

2.2. Superconducting Fault Current Limiters (SFCL)

Section 2.2 describes the modelling of the SFCL for limiting fault current. Various SFCLs such as resistive-, trigger- and flux lock types have been studied. Among them, the resistive type which consists of the simple component has a fast operation due to only using the characteristics of the high temperature superconductivity (HTSC) elements [30,31]. Fast operation characteristics are a very important issue in the LVDC system. Therefore, the resistive type SFCL was applied in this paper.

The SFCL has zero resistance under normal state. This feature has the advantage that there is no line loss than the method of increasing the line impedance to limit the fault current. Also, the power quality has not degraded compare with changing the capacity of the DC capacitor. The application of the SFCL on the LVDC system is an economical method to limit the fault current because it does not require an upgrade of the circuit breaker. Table 3 shows the parameter of the SFCL in this paper. Equation (1) shows the resistance of the HTSC elements according to the time. The R_n represents the resistance of the HTSC elements when quench phenomenon occurs. The t_0,t_0 and t_2 represent the quench starting time, first recovery starting time and secondary recovery starting time, respectively. The a_1, a_2, b_1 and b_2 represent the coefficients of experimental results [32–34].

Table 3. Parameter of superconducting fault limiter (SFCL).

Parameter	R_n	T_f	a_1 **[1/s]**	a_2 **[1/s]**	b_1	b_2
Value	Variable	0.01	−80	−160	R_n	$R_n/2$

$$R(t) = \begin{cases} 0 & (t > t_0) \\ R_n[1 - exp(-\frac{t-t_0}{T_F})]^{\frac{1}{2}} & (t_0 \leq t < t_1) \\ a_1(t - t_1) + b_1 & (t_1 \leq t < t_2) \\ a_2(t - t_2) + b_2 & (t_2 \leq t) \end{cases} \quad (1)$$

The HTSC elements have resistance due to a phenomenon called quench when the fault current exceeds a critical current. Therefore, the fault current was limited by the resistance on the HTSC elements when the quench phenomenon occurs. The phenomenon called quench could effectively limit the fault current faster than other methods. As shown in Figure 2, the method of applying SFCL on the LVDC system has following advantages:

- The fault current could be limited quickly by the resistance on the HTSC elements when the quench phenomenon occurs.
- The line losses were reduced than the method of increasing the impedance for limiting fault current.
- The power quality was not degraded compared to the method of changing the capacity of the DC capacitor.
- Since there is no need to upgrade the circuit breaker, the operation cost could be reduced.

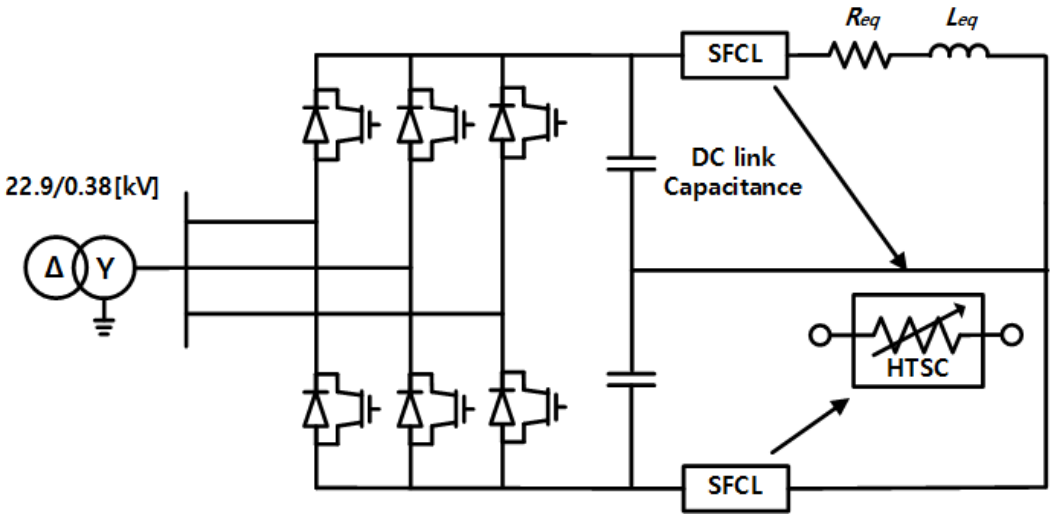

Figure 2. Concept of SFCL on LVDC system.

3. Simulation Results

Section 3 verified the effectiveness of limiting the fault current when the SFCL was applied using PSCAD/EMTDC. Also, the operational characteristics of the protection relay such as over current relay, selective protection relay were analysed when the fault current was limited by applying the SFCL [5–7].

3.1. Fault Analysis in LVDC System

Section 3.1 analysed the short-circuit fault in the LVDC system. In order to solve the complete response of the non-linear circuit, the different stages of the fault are analysed separately. Figure 3 shows the equivalent circuit for the short circuit fault on the LVDC system. The fault analysis on the LVDC system was analysed in detail in three stage from Subsecions 3.1.1–3.1.3.

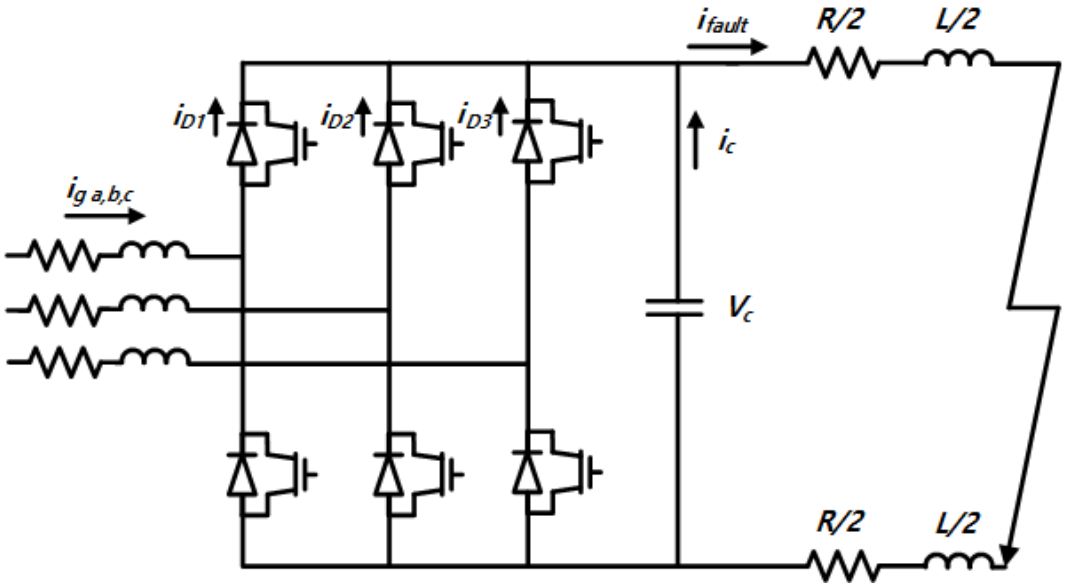

Figure 3. Equivalent Circuit for Short Circuit Fault in LVDC System.

3.1.1. Stage 1: Capacitor-Discharge Stage (Natural Response)

The first stage on the DC fault analysis is the DC-link capacitor-discharge. When the fault occurs on the LVDC system, the IGBT is quickly opened for self-protection. The capacitor on the DC-link discharges the current to the line. When the fault occurs at time t_0, under the initial conditions of $v_c(t_0) = V_0$ and $i_{fault}(t_0) = I_0$, Equations (2) and (3) represent the voltage of the DC-link and fault current.

$$v_C = \frac{V_0\omega_0}{\omega}e^{-\delta t}\sin(\omega t + \beta) - \frac{I_0}{\omega C}e^{-\delta t}\sin\omega t \tag{2}$$

$$i_{fault} = C\frac{dv_C}{dt} = -\frac{I_0\omega_0}{w}e^{-\delta t}\sin(\omega t - \beta) + \frac{V_0}{\omega L}e^{-\delta t}\sin\omega t \tag{3}$$

where, $\delta = R/2L, w^2 = 1/LC - (R/2L)^2, w_0 = \sqrt{\delta^2 + \omega^2}$ and $\beta = arctan(w/\delta)$.

t_1 is represented by Equation (4) when the voltage of the DC link to zero.

$$t_1 = t_0 + (\pi - \gamma)/\omega \tag{4}$$

where, $\gamma = arctan[(V_0\omega_0 C\sin\beta)/V_0\omega_0 C\cos\beta - I_0)]$.

3.1.2. Stage 2: Diode Freewheel Stage(Natural Response; After $V_C = 0$)

The second stage is line inductance discharges the current when the voltage of the DC-link drops to zero. Typically, this stage occurs within a few ms after the fault and the time for the inductance to discharge the current is affected by the capacity of the DC capacitor. The fault current has an initial value $i_{fault}(t_1) = I_0'$. The fault current where each phase-leg freewheel diode current carries a third of the current is represented by Equation (5).

$$i_{fault} = I_0' e^{-(R/L)t} \qquad i_{D1} = i_{fault}/3. \tag{5}$$

3.1.3. Stage 3: Grid-Side Current Feeding Stage (Forced Response)

This stage is to receive the current from the grid after the capacitor of the DC-link and line inductance have exhausted their source. The Equations (6) and (7) represent the line current and voltage respectively.

$$i_{fault} = A\sin(\omega_s t + \gamma) + Be^{-t/\tau} + [C_1\omega_0 e^{-\delta t}\sin(\omega t + \beta)]/\omega + (C_2 e^{-\delta t}\sin\omega t)/\omega, \tag{6}$$

$$v_C = Ri_{fault} + L\frac{di_{fault}}{dt} \tag{7}$$

where, $A = I_g[(1 - \omega_s^2 LC)^2 + (RC\omega_s)^2]^{-1/2}$, $\gamma = a - \epsilon - \theta$, $\theta = arctan[(RC\omega_s/(1 - \omega_s^2 LC)]$, $B = I_{gn}[\tau^2/(\tau^2 - RC\tau + LC)]$, $C_1 = -(A\sin\gamma + B)$ $C_2 = B/\tau - \omega_s A\cos\gamma$.

3.2. Application of Superconducting Fault Current Limiters (SFCL)

Section 3.2 verified the effect of applying the SFCL through PSCAD/EMTDC. Figure 4 shows the fault current in the LVDC system when the SFCL was applied or not. The peak of the fault current was increased sharply to 4.124 [kA] by the discharge current of the capacitor on the DC-link. The fault current which is rapidly increased than the AC system caused problems for the LVDC system. In order to protect the power conversion system, the LVDC system needed a method for limiting the fault current. This paper proposed the application of the SFCL to take advantage mentioned in Section 2.2. When the SFCL was applied to the LVDC system, the fault current was limited from 4.124 [kA] to 1.494 [kA] due to a

resistance of the HTSC elements by quenching phenomenon. As a result, limiting the fault current was confirmed when the SFCL was installed.

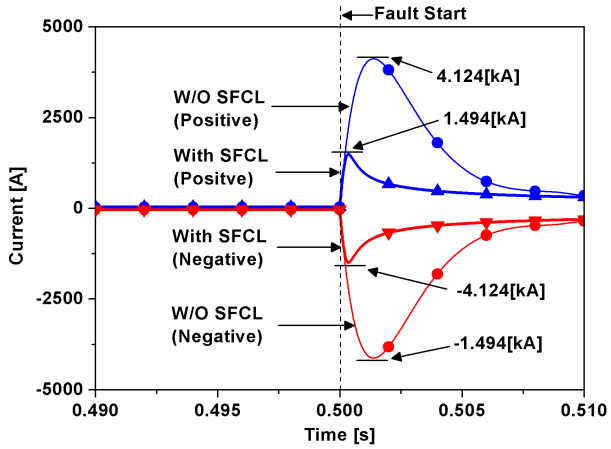

Figure 4. Fault Current according to apply or not SFCL.

Figure 5 shows the DC voltage in the LVDC system when the SFCL was applied or not. When the SFCL was not applied, the DC voltage dropped to near zero. However, when the SFCL was applied, the DC voltage drop was improved by the resistance of the HTSC. As a result, the improvement of the voltage drop was confirmed when the SFCL was installed.

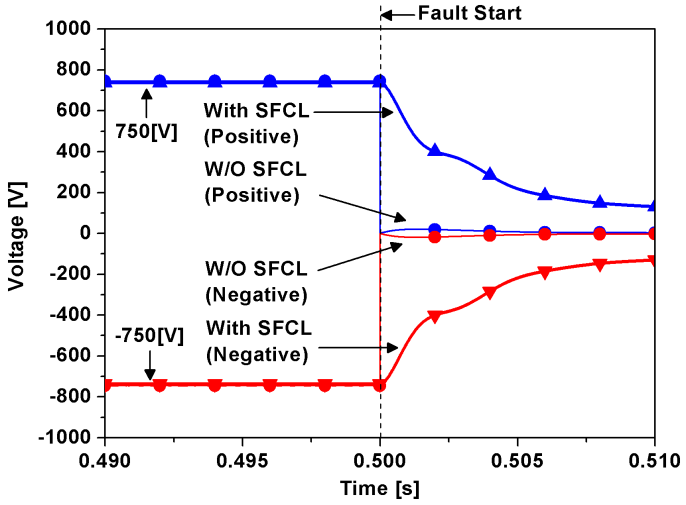

Figure 5. DC Voltage in LVDC system according to apply or not SFCL.

3.3. Operational Characteristics of Over Current Relay

Section 3.3 describes the operational characteristics of the inverse time relay. The inverse time relay sends the trip signal to the circuit breaker depending on the magnitude of the fault current flowing through the current transformer(CT). The inverse time relay was mainly used in back up protection because the timing of sending the trip signal changes depending on the magnitude of the fault current. The inverse time relay reviewed in this paper were modelled using Equation (8) which represents the extremely inverse

(EI) of IEC 60255 standard characteristics [25,26]. In this paper, the time multiplier setting (TMS) value of 0.2 was selected for fast fault detection of the LVDC system.

$$t = TMS \cdot \frac{80}{I_r^2 - 1} \tag{8}$$

where, $I_r = I/I_s$, $I = Measured\,Current$, $I_s = Relay\,Setting\,Current$, $TMS = Time\,Multiplier\,Setting$

Figures 6–8 show the fault current of the positive pole and the trip signal of the protection relay. Figure 6 shows the fault current and trip signal in the over current relay when the SFCL was applied or not. The fault current was limited from 4.124 kA to 1.494 kA by the resistance of the HTSC elements. However, the trip signal was not sent to the circuit breaker because the I_r was reduced by limiting the fault current. To solve the problem of no trip signal, there are two conventional methods. The first method is to change the value of the TMS. The second method is to change the relay setting current (I_{pickup}) value of I_r. However, these methods which are to change the parameter of the relay are not recommended because it is difficult to take into account changes in the system. In addition, when the HTSC elements are not quenched, the LVDC system is fatally damaged because the relay is not properly working. To solve these problems, the over current relay was set in consideration of the voltage component of the HTSC elements.

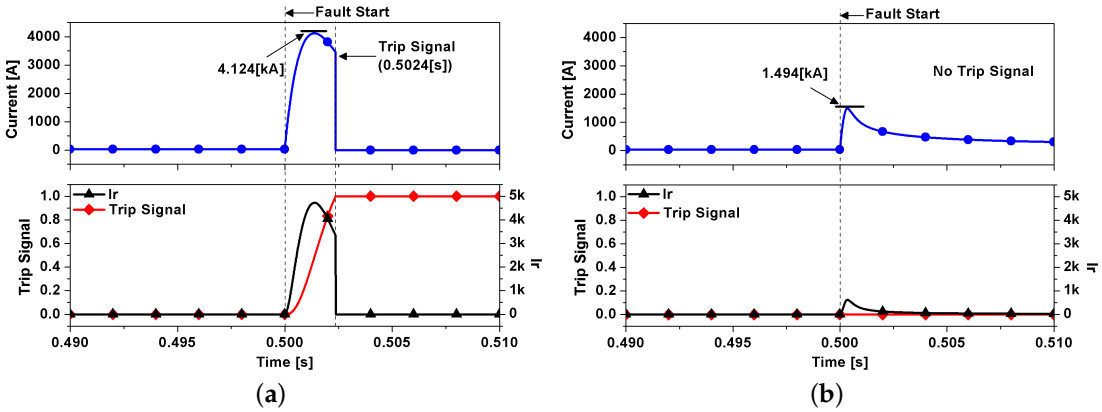

Figure 6. Fault Current and Trip Signal in Over Current Relay (**a**) W/O SFCL (**b**) With SFCL.

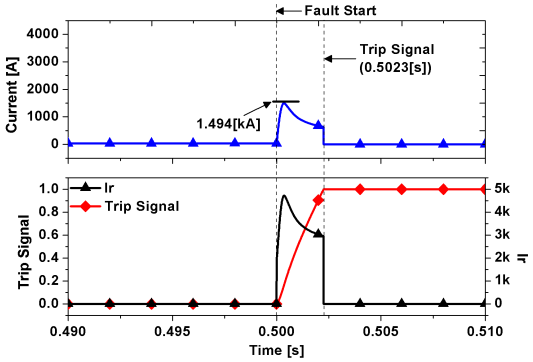

Figure 7. Fault Current and Trip Signal when using the voltage component of high temperature superconductivity (HTSC) element.

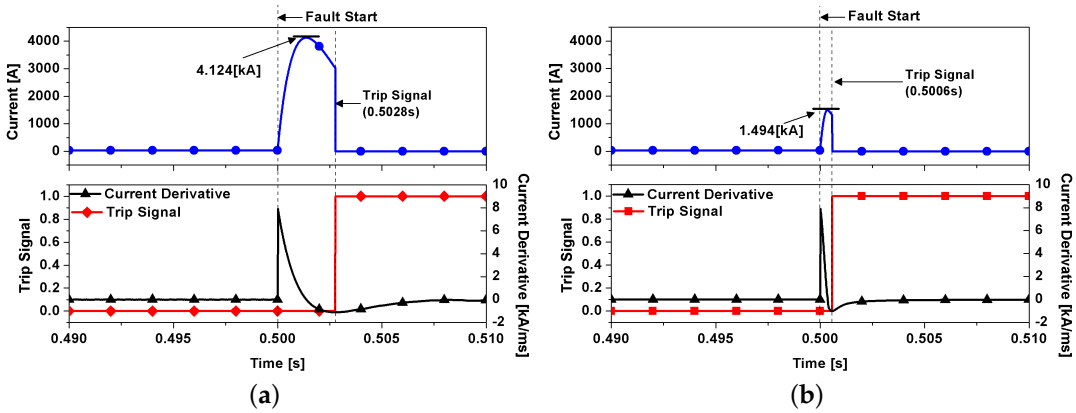

Figure 8. Fault Current and Trip Signal in Selective Protection Relay (**a**) W/O SFCL (**b**) With SFCL.

Equation (9) shows the modified I_r of the over current relay using the voltage component of the HTSC elements. When the fault current was below a critical current, since the HTSC voltage was zero($V_{SFCL} = 0$), the over current relay sent a trip signal to the circuit breaker similar to the case of the without SFCL. On the other hand, when the fault current exceeded a critical current, I_r reduced by the limited fault current could be compensated by the voltage component (αV_{SFCL}).

$$I_r = \frac{I_{fault}^{SFCL} + \alpha V_{SFCL}}{I_s} = \frac{I_{fault}^{SFCL}}{I_{pickup}} \cdot (1 + \alpha Z_{SFCL}) \tag{9}$$

where, $\alpha = \frac{(\frac{I_{fault}}{I_{fault}^{SFCL}}) - 1}{Z_{SFCL}}$.

Figure 7 shows the fault current and trip signal in the over current relay using the voltage component of the SFCL. The fault current was not only limited by the SFCL, but also the malfunction of the over current relay was improved through the use of the voltage component.

3.4. Operational Characteristics of Selective Protection Relay

Section 3.4 describes the operational characteristics of the selective protection relay. The selective protection relay sends a trip signal to the circuit breaker when the derivative(di/dt) of the fault current flowing through the CT exceeds a certain value. The selective protection relay has been used to main protection because the LVDC system is no phase and a large fault current flows momentarily by the capacitor of the DC-link. Under the normal condition of the LVDC system, the derivative in load current is close to zero. However, when the fault occurs on the LVDC system, the derivative is very high due to the capacitor of the DC-link. The selective protection relay detects the fault by using the derivative in the fault current. Figure 8 shows the fault current and the trip signal of the selective protection relay when the SFCL was applied or not. The fault current was limited from 4.124 [kA] to 1.494 [kA] by the resistance of the HTSC elements. Also, the timing of the trip signal was changed from 0.5028 [s] to 0.5006 [s] due to the change in the derivative.

4. Discussion

Section 3.1 represents the characteristics of the fault current in the LVDC system. In Section 3.2, the effect of limiting fault current on the LVDC system using the SFCL was confirmed. The fault current on the LVDC system was limited through applying SFCL, but this causes a problem in the operational

characteristics of the protection relay. In Section 3.3, the trip signal of the over current relay was not sent to the circuit breaker properly due to reducing I_r. Therefore, in this paper, the voltage component of the HTSC was used to improve the relay's trip signal to the circuit breaker even when the fault current was limited. The I_r reduced by the SFCL was compensated by the voltage component of the HTSC elements. Even if the fault current was limited by applying the SFCL, the over current relay properly detected the fault through the method proposed in this paper. Section 3.4 describes the selective protection relay that are mainly used as main protection relay in the LVDC system. The selective protection relay has quickly detected the fault because the current derivative changed through the application of the SFCL. Therefore, the performance of the fault detection on selective protection relays was improved by applying the SFCL. Table 4 shows the results of the method proposed in this paper.

Table 4. Simulation Results.

Classification	Over Current Relay	Selective Protection Relay
Peak of Fault Current W/O SFCL [A]	4124	4124
Peak of Fault Current With SFCL [A]	1494	1494
Timing of Trip Signal W/O SFCL [s]	0.0024	0.0028
Timing of Trip Signal With SFCL [s]	No Trip Signal	0.0006
Timing of Trip Signal With SFCL using Voltage Component [s]	0.0023	-

5. Conclusions

The LVDC system has a problem with large fault currents by the capacitor of the DC-link when the fault occurs. To solve these problems of LVDC system, this paper proposed applying an SFCL for limiting fault current in the LVDC system. The operation characteristics of the over current relay which caused malfunction due to limiting fault current was improved by using voltage component proposed in this paper. The selective fault relay operated by derivative has quickly detected the fault by applying the SFCL proposed in this paper. The solution proposed in this paper have the following advantages:

- The fault current on the LVDC system could be limited by applying the SFCL. Therefore, the economics have been improved due to not require the upgrade of the circuit breaker. Also, the LVDC system mitigated the risk of the fault current.
- The DC voltage drop was improved by the resistance of the HTSC elements.
- The line losses were reduced compared to the method of increasing impedance.
- The power quality was not affected compared to the method of changing the capacity of the DC capacitor.
- Unlike other methods, the application of the SFCL for limiting fault current could not affect the system.
- Even if the fault current was limited, the over current relay properly sent the trip signal to the circuit breaker through using the voltage component of the HTSC.
- The operational characteristics of the selective protection relay were improved by applying the SFCL.

Through the advantages mentioned above, the LVDC system could be effectively operated. In the future, it is necessary to research the fault characteristics on the LVDC system according to the system configuration, fault type and location.

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Nomenclature

PV	Photovoltaic
ESS	Energy Storage System
IGBT	Insulated Gate Bipolar Transistor
SFCL	Superconducting Fault Current Limiter
MMC	Modular Multi-level Converter
FCL	Fault Current Limiter
SC	Superconducting Cable
PSCAD/EMTDC	Power System Computer Aided Design/Electromagnetic Transients including DC
R_n	Resistance of HTSC Element
t_0, t_1, t_2	Recovery Starting Time
a_1, a_2, b_1, b_2	Coefficients of Experimental Results
CT	Current Transformer
EI	Extremely Inverse
TMS	Time Multiplier Setting
HTSC	High Temperature Superconductivity

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