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Numerical Laplace Inversion Method for Through-Silicon Via (TSV) Noise Coupling in 3D-IC Design

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Abstract: Typical 3D integrated circuit structures based on through-silicon vias (TSVs) are complicated to study and analyze. Therefore, it seems important to find some methods to investigate them. In this paper, a method is proposed to model and compute the time-domain coupling noise in 3D Integrated Circuit (3D-IC) based on TSVs. It is based on the numerical inversion Laplace transform (NILT) method and the chain matrices. The method is validated using some experimental results and the Pspice and Matlab tools. The results confirm the effectiveness of the proposed technique and the noise is analyzed in several cases. It is found that TSV noise coupling is affected by different factors such as source characteristics, horizontal interconnections, and the type of Inputs and Outputs (I/O) drivers.

Keywords: 3D-IC design; NILT; TSV noise coupling; RDL; chain matrix; interconnect line

1. Introduction

Over the last four decades, silicon semiconductor technology has advanced at exponential rates in terms of performance and productivity [1,2]. Analysis of the fundamentals, materials, devices, circuits, and system limits discloses that silicon technology still has colossal potential for achieving terascale integration (TSI) of a significant number of transistors per chip. Such large-scale integration is feasible by assuming the development and bulk economic production of metal-oxide-semiconductor double-gate field-effect transistors. The development of interconnect lines for these transistors is a major challenge for the realization of nanoelectronics for TSI. Employing systems with high performance requires using two approaches. The first consists of reducing the size of the transistors, to enhance IC reduction technologies, and assembling ICs on the same chip (SoC) [3]. The second consists of developing high-performance technologies for interconnections between chips (SiP). For proper functioning, the area occupied by interconnections, which sometimes exceeds that occupied by the main functional blocks or chips, as well as their lengths must be reduced. However, since the interconnections are required in electronic systems, the number of interconnections cannot be decreased adversely to the area which can be reduced using 3D technology based on vertical interconnections.

Three-dimensional technology is acknowledged as an effective solution to overcome the challenges of miniaturization and distribution density. It combines More Moore and More than Moore, which offers many benefits. Some advantages of this technology are power efficiency, performance enhancement, cost reduction, and modular design [4–6]. Three-dimensional technology allows vertical stacking of chips through vertical interconnections like Through-Silicon-Via. Three-dimensional architectures contain different elements, such as through-silicon vias (TSVs), the substrate, redistribution layers (RDLs), and active circuits, which makes them difficult to model and study. To model these structures, each element is modeled using lumped circuits, and the entire model is then constructed by combining these element models in an appropriate manner.

Several papers have discussed the issue of modeling TSVs. In [7,8], the authors proposed a methodology based on Radio Frequency (RF) characterizations and simulations, leading to a frequency-dependent analytical model including the metal-oxide-semiconductor (MOS) effect of high ratio TSVs. The authors of [9] gave an accurate electrical model of TSVs considering metal-oxide-semiconductor (MOS) capacitance effects. The MOS capacitance accurately solved Poisson's equation in cylindrical coordinates. Another compact wideband equivalent circuit model for electrical modeling of TSVs has been presented in [10]. In another previous work [11], the Resistance, Inductance and Capacitance (RLC) parameters of TSVs were modeled as a function of physical parameters and material characteristics. The RLC model is applied to predict the resistance, inductance, and capacitance of small-geometry TSV architectures. TSV impedance can also be extracted using a fully analytical and physical model in addition to Green's function in high frequency [12]. All these previous works have given models of one TSV without considering general multi-TSV architectures. Thus, in [3,13,14] a TSV noise coupling model and TSV-to-active circuit have been proposed based on a three-dimensional transmission line matrix method (3D-TLM). Using this method, the noise transfer functions in the frequency domain from TSV-to-TSV and TSV-to-active circuit can be estimated. Other analytical models, for vias and traces, have been proposed in [15]. Vias are modeled using an analytical formulation for the parallel-plate impedance and capacitive elements, whereas the trace-via transitions are described by modal decomposition. All these proposed models are validated against full-wave methods and measurements up to 40 GHz. An efficient method to model TSV interconnections is proposed in [16]. This technique is based on solving Maxwell's equation in integral form, the method uses a small number of global modal basis functions and can be much faster than discretization-based integral-equation methods. The models proposed in the literature differ; indeed, some models contain the depletion capacitance, TSV resistance, and TSV inductance, others neglect these elements, especially for frequencies below 20 GHs [3,13,14].

The TSV capacitance depends on both the oxide capacitance and the depletion capacitance [17]. As the TSV gate bias increases, the depletion region capacitance starts to increase, and it acts in series with oxide capacitance. Hence, a TSV capacitor, C_{TSV}, is modeled with a series connection of the oxide capacitors and a depletion region capacitor [18]. The width of the depletion region is calculated for every geometrical variation by means of the exact Poisson's equation for an average TSV voltage of 0.5 V, and modeled as an area where the substrate has no free charge carriers [19]. Consequently, an increasing average TSV voltage increases its isolation from the substrate [20]. Thus, a power V_{dd}-TSV generally draws less E-field lines than a ground GND-TSV. However, the influence of the depletion region can be neglected [19].

RDLs have an important role in TSV packaging applications, they are used to connect various elements in 3D-IC and to redistribute the signals between dies. Therefore, different works have proposed several models for these interconnections. In [3,21], the authors gave analytic RLGC equations for the equivalent circuit model of a single-ended signal RDL to estimate the electrical characteristics. For the substrate, which has a distribution nature, its model can be extracted from numerical techniques mentioned in [22,23]. By combining each partial model, the global model of 3D structures is obtained.

One of the 3D-architecture challenges is to avoid noise coupling, which is a significant problem and causes serious effects. This noise degrades system performance and makes it more sensitive. It can also be transmitted directly to an active circuit through the substrate; therefore, the signal and power are corrupted, the system reliability is reduced, and the bit error rate is increased [24,25].

The investigation of the noise coupling in 3D architecture based on TSVs is mainly done in the frequency domain. Yet, as far as we know, no technique has been proposed to compute these noises in the time domain. Hence, the objective of this paper is to propose a method to compute noise coupling in 3D-IC in the time domain. It is necessary to obtain the wave forms of these noises in the time domain in order to analyze them, since the transition effects can be better observed in the time domain. Time-domain noise coupling was obtained by the NILT method and chain matrices. First, the method

was applied to three different structures. Then, the TSV coupling noise was analyzed, for each structure, to deduce how the coupling between the horizontal interconnections affects it. Simulations in Pspice were done to validate the method.

The rest of the paper is organized as follows. The NILT method in addition to a chain matrix of many studied circuits are explained in Section 2. The results and simulations are analyzed in Section 3. The conclusions are drawn in the last section.

2. Calculation of Time-Domain TSV Noise Coupling in 3D-IC Design with NILT

The use of the Laplace transform method has simplified the solution of transients on transmission lines (TL), of transients of dynamic systems, and other problems in electrical engineering. However, some difficulties appear when transforming solutions to the time domain. This makes researchers concerned to find accurate and precise numerical methods. One of these numerical methods is the numerical inverse Laplace transform (NILT) method, which can be used in cases when, for instance, the transform is a transcendental, irrational or some other complex function; then finding the solution in its analytical form is difficult and sometimes impossible [26,27].

The NILT method has been used in several works. In [28], NILT methods were selected to evaluate their performance for dealing with solution transportation in the subsurface under uniform or radial flow conditions. The authors of [29] evaluate and compare some numerical algorithms of the NILT method for the inversion accuracy of some fractional order differential equation solutions. In [30–35] the multidimensional NILT method has been explained in detail for electrical circuits.

In this paper, we were interested in 1D-NILT. Thus, a one-dimensional Laplace transform of a function $f(t)$, with; $t \geq 0$, is defined as:

$$F(s) = \int_0^\infty f(t)e^{-st}dt \tag{1}$$

Under the assumption $\left|f(t)\right| \leq Me^{\alpha t}$, M is real positive, α is a minimal abscissa of convergence, and $F(s)$ is defined on a region $\{s \in C : \mathrm{Re}[s] > \alpha\}$, with $s = c + j\Omega$, c is defined as an abscissa of convergence, $\Omega = \frac{2\pi}{\tau}$ as the generalized frequency step, and τ forms a region of the solutions $t \in [0\ \tau]$.

The original function can be given using the Bromwich integral [36]:

$$f(t) = \frac{1}{2\pi j}\int_{c-j\infty}^{c+j\infty} F(s).e^{st}ds \tag{2}$$

By using a rectangular rule of integration as mentioned in [30], Equation (3) is found.

$$\tilde{f}(t) = \frac{\exp(ct)}{\tau}\ \sum_{n=0}^{\infty} F(s)\exp(jn\Omega t) \tag{3}$$

As explained in [30], by substituting $s = c + jn\Omega$ into Equation (1), if the obtained function has integration ranges split into infinite numbers of steps of the length τ, $F(s)$ could be written as:

$$F_n = F(c + jn\Omega) = \sum_{l=0}^{\infty}\ \int_{l\tau}^{(l+1)\tau} g(t)\ \exp(-jn\Omega t)\ dt \tag{4}$$

$g(t)$ is an exponentially damped object function. Then for $t \in [l\tau, \tau(l+1)]$, the functions $g_l(t)$ and $F(s)$ are given by:

$$g_l(t) = f(t)\exp(-ct) \tag{5}$$

$$F(c + jn\Omega) = \tau \sum_{l=0}^{\infty} C_{l,n} \tag{6}$$

where:

$$C_{l,n} = \frac{1}{\tau} \int_{l\tau}^{(l+1)\tau} g_l(t)\ \exp(-jn\Omega t)dt \tag{7}$$

Applying complex Fourier series to Equation (5), $g_l(t)$ could be found as:

$$g_l(t) = \sum_{n=-\infty}^{+\infty} C_{l,n} \exp(jn\Omega t) \tag{8}$$

Moreover, by substituting Equation (6) into Equation (3) and considering Equation (8), it is found that the approximate original function exponentially damped could be expressed as the infinite sum of the newly defined periodical function, Equation (5).

By exploiting all the previous equations, $\tilde{f}(t)$ is obtained and the absolute error $\varepsilon(t) = \tilde{f}(t) - f(t)$ can be computed.

$$\tilde{f}(t) = f(t) + \sum_{l=1}^{\infty} f(l\tau + t).\exp(-cl\tau) \tag{9}$$

A limiting absolute error is determined as $\varepsilon_M(t) \geq \varepsilon(t)$, then $\left|f(t)\right| \leq Me^{\alpha t}$, so a limiting relative error δ_M could also be controlled, and a path of integration from a required limit relative error could be chosen using Equation (10).

$$c = \alpha - \frac{1}{\tau} \ln\left(1 - \frac{1}{1+\delta_M}\right) \approx \alpha - \frac{1}{\tau} \ln(\delta_M) \tag{10}$$

This formula is valid, with a relative error achieved by the NILT $\tilde{f}(t)$, if infinite numbers of terms are used in series, and is a suitable technique for accelerating a convergence and for achieving the convergence of infinite series in a suitable way. Equation (3) can be rewritten using FFT and IFFT algorithms for an effective computation. Based on the experience of the authors of [31], the quotient-difference (q-d) algorithm of Rutishanser seems to give errors rather close to δ_M predicted by Equation (10), while considering a relatively small number of additional terms.

While considering a discrete variable in the original domain, $t_k = kT$, where T is a sampling period, $\tilde{f}(t)$ could be expressed as:

$$\tilde{f}_k = \frac{\exp(ckT)}{\tau} \sum_{n=-\infty}^{\infty} \tilde{F}\left(c + jn\frac{2\pi}{\tau}\right) \exp\left(j2\pi\frac{nkT}{\tau}\right) \tag{11}$$

The above stated formula could be decomposed as:

$$\tilde{f}_k = C_k \left[\sum_{n=0}^{N-1} \tilde{F}^{(-n)} z_{-k}^n + \sum_{n=0}^{\infty} \tilde{G}^{(-n)} z_{-k}^n + \sum_{n=0}^{N-1} \tilde{F}^{(n)} z_k^n + \sum_{n=0}^{\infty} \tilde{G}^{(n)} z_k^n - \tilde{F}^{(0)} \right] \tag{12}$$

where $N = 2^k$, k integer, $\tilde{F}^{(\pm n)} = \tilde{F}(c - jn\Omega)$, $\tilde{G}^{(\pm n)} = \tilde{F}^{(\pm N \pm n)}$, $z_{\pm k} = \exp\left(\pm j\frac{2\pi kT}{\tau}\right)$, and $C_k = \frac{\exp(ckT)}{\tau}$, while $\tau = NT$, $\forall k$, and $z_{\pm k}^N = \exp(\pm j2\pi k) = 1$.

In Equation (12), the first and the third sum are evaluated using the FFT and IFFT algorithms, respectively, while other parts, which present the infinite sum, are used as the input data in the q-d algorithm that uses a very small number of necessary additional terms, as explained in [24]. The computing region should be chosen as: $O_{cal} = (0, t_{cal})$, where $t_{cal} = \left(\frac{N}{2} - 1\right).T$.

Time-domain noise coupling could be easily obtained by the explained method in 3D technology based on TSVs.

In order to compute the noise coupling, different circuits were treated. The first structure is illustrated in Figure 1. This figure represents a basic structure of the TSV–TSV noise coupling [3]. It is composed of two signal TSVs, two ground TSVs, and is terminated by I/O drivers. The simplified lumped circuit model of this structure is given in Figure 2, where $C_{TSV\text{-}equiv}$ is the total equivalent TSV capacitance, $R_{sub\text{-}equiv}$ is the substrate resistance, and $C_{sub\text{-}equiv}$ is the substrate capacitance. In this simplified model, proposed in [3], the TSV resistance (R_{TSV}), the TSV inductance (L_{TSV}), and the depletion region are neglected, but in our work R_{TSV} and L_{TSV} are kept. In the study just mentioned, the authors assume that their effects appear in frequencies above 12 GHz. To consider the effect of the depletion region, which is modeled by a capacitance, it is enough to add its value to the TSV capacitance. The I/O drivers can be modeled as a resistor for the output driver and as a capacitor for the input driver that represents the MOS gate capacitance. The I/O drivers are presented by the impedances Z_1, Z_2, Z_3, and Z_4. To apply the NILT method, the conceptual structure can be modeled with a T-matrix, as illustrated in the figure. The entire matrix of the circuit is the product of T_1, T_2, and T_3, as defined below.

$$\begin{pmatrix} V_1 \\ I_1 \end{pmatrix} = [T] \begin{pmatrix} V_2 \\ -I_2 \end{pmatrix} \tag{13}$$

where:

$$[T] = [T_4]\,[T_1]\,[T_2]\,[T_3]\,[T_4] \tag{14}$$

$$[T_1] = \begin{bmatrix} 1 & 0 \\ 1\Big/\left(Z_2 + \frac{R_{tsv}}{2} + s\frac{L_{tsv}}{2}\right) & 1 \end{bmatrix} \tag{15}$$

$$[T_2] = \begin{bmatrix} 1 & Z_{eq} \\ 0 & 1 \end{bmatrix} \tag{16}$$

$$[T_3] = \begin{bmatrix} 1 & 0 \\ 1\Big/\left(Z_3 + \frac{R_{tsv}}{2}\right) + s\frac{L_{tsv}}{2} & 1 \end{bmatrix} \tag{17}$$

$$[T_4] = \begin{bmatrix} 1 & R_{tsv} + sL_{tsv} \\ 0 & 1 \end{bmatrix} \tag{18}$$

$$Z_{eq} = \frac{2}{2C_{TSV-equiv}s} + \frac{R_{sub-equiv}}{1 + R_{sub-equiv}C_{sub-equiv}s} \tag{19}$$

Observing the circuit, Equations (14) and (15) are found:

$$V_{in}(s) = Z_1(s)I_1(s) + V_1(s) \tag{20}$$

$$V_2(s) = -Z_4(s)I_2(s) \tag{21}$$

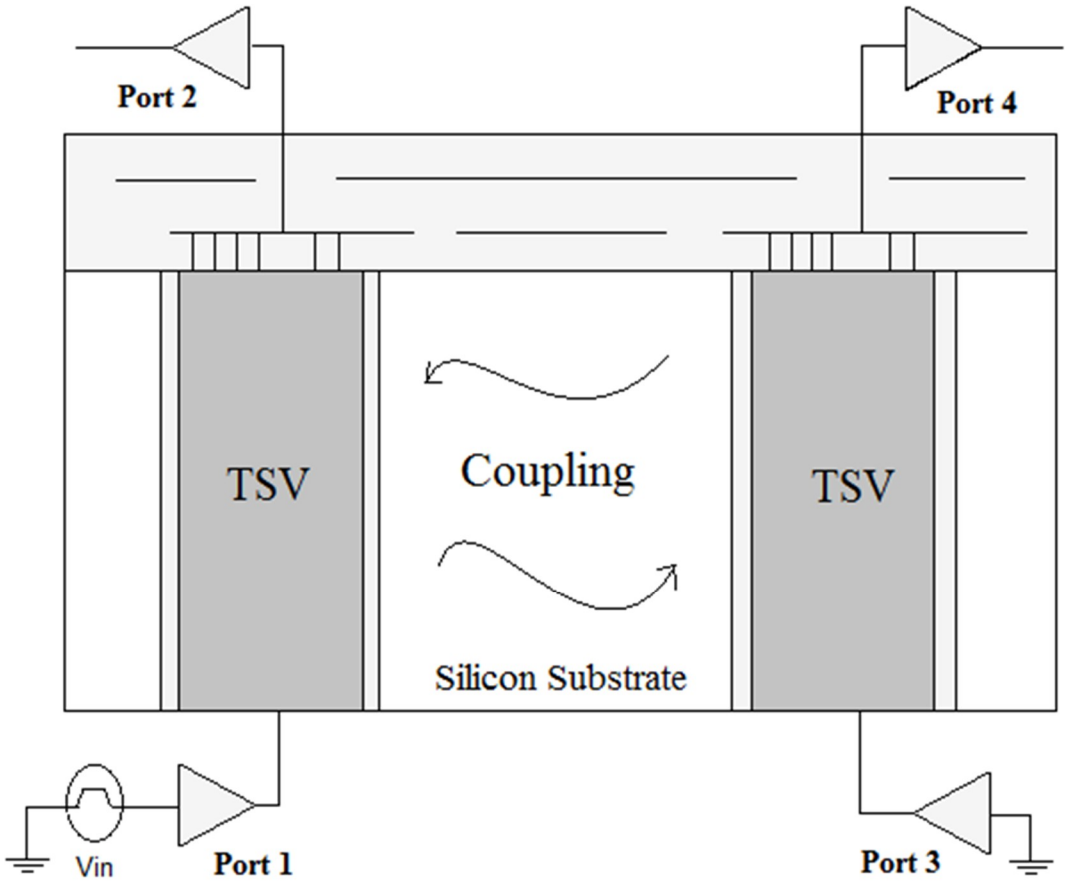

Figure 1. The through-silicon via (TSV)–TSV noise coupling structure with I/O termination.

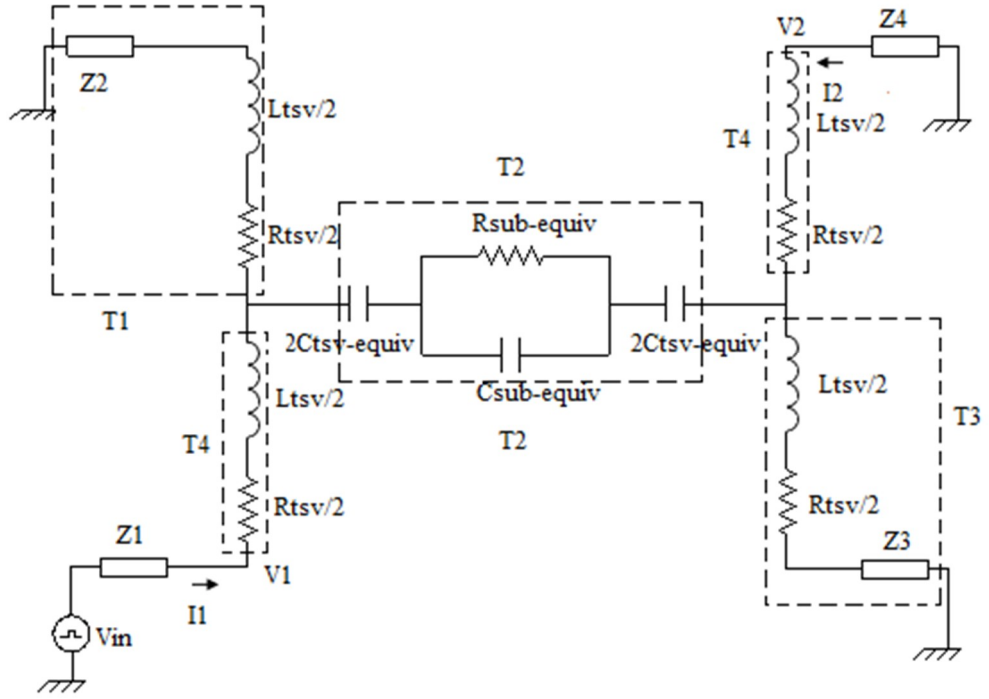

Figure 2. Lumped circuit model of TSV–TSV noise coupling.

By exploiting Equations (13)–(15), the noise V_2 could be expressed in the frequency domain according to V_{in}, then the NILT method can be applied, by replacing F(s) by V_2(s) in previous equations, to find the noise in the time domain. The voltage source V_{in} is a periodic trapezoidal signal switching expressed by Equation (16).

$$V_{in}(s) = \sum_{n=0}^{\infty} \exp(-snT).E(s) \tag{22}$$

where T is the period and E(s) represents the trapeze shape.

Then, while $\frac{1}{1-x} = \sum_{n=0}^{\infty} x^n$, Equation (16) could be written as:

$$V_{in}(s) = \frac{1}{1-\exp(-Ts)}E(s) \tag{23}$$

The second analyzed structure is given in Figure 3. It represents the conceptual view of TSV–active circuit noise coupling. The equivalent circuit model of this structure is similar to that in Figure 2, except that the capacity on the right is eliminated [3]. Consequently, the calculation was also done in the same way.

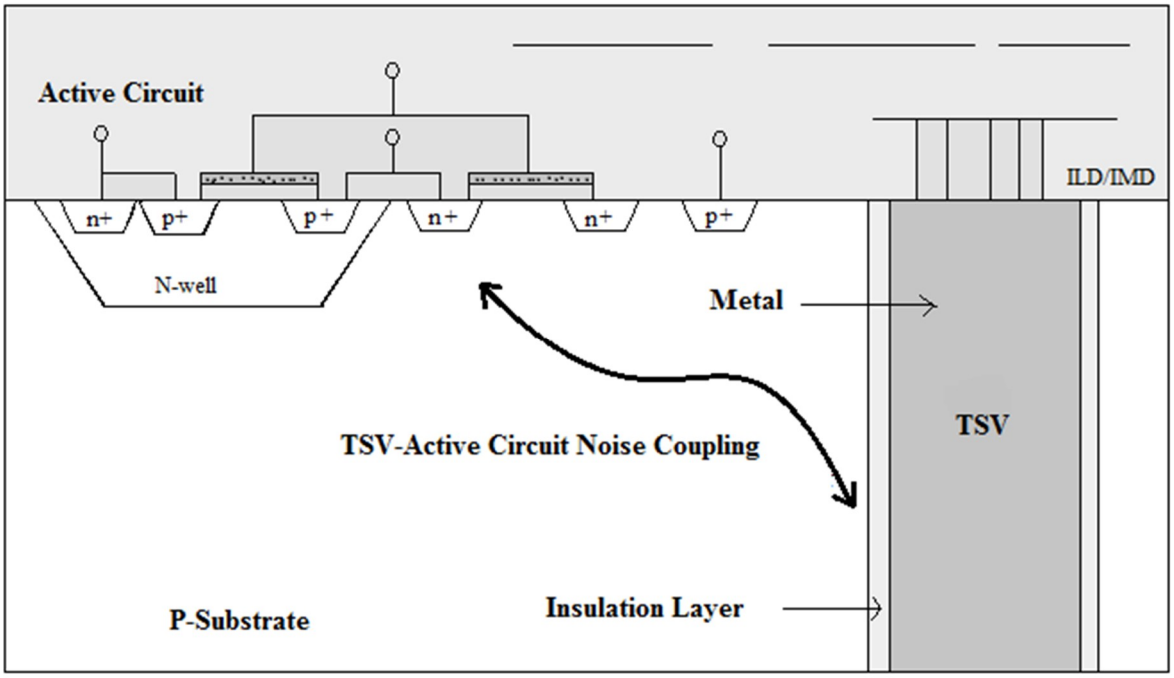

Figure 3. The conceptual view of TSV–active circuit noise coupling.

Because of the diversity of electronic devices, and the presence of many stacked dies in 3D technology, the second studied circuit contains two stacked dies with two interconnect lines. The concerned structure is presented in Figure 4. First, the noise coupling was calculated without taking into consideration the coupling between the two interconnect lines, only the coupling between the TSVs in each level was considered. This conceptual structure is modeled by a lumped circuit, as given in Figure 5.

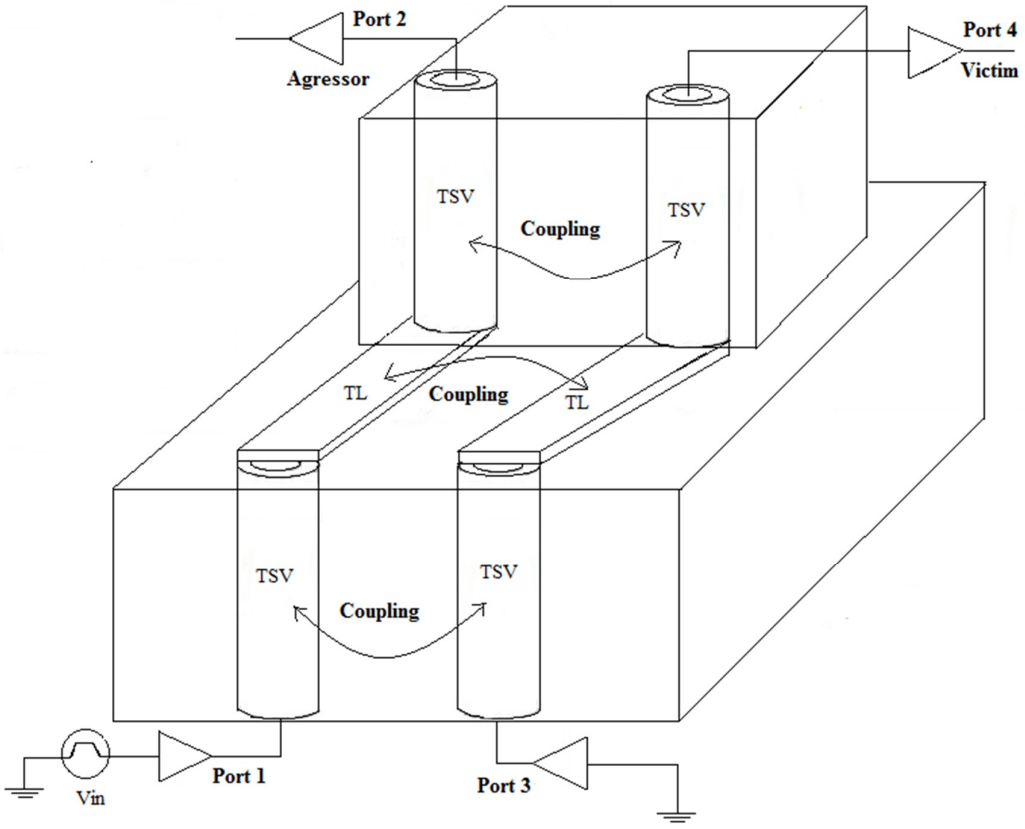

Figure 4. The conceptual view of a TSV noise coupling structure with interconnect lines and I/O drivers.

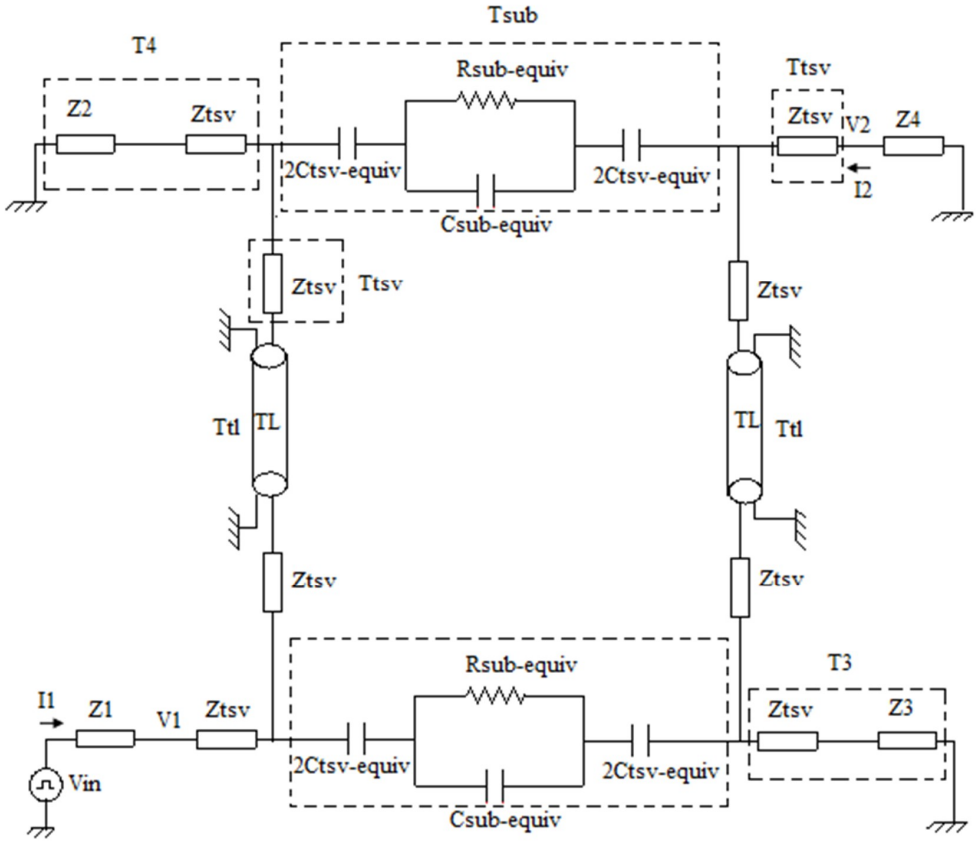

Figure 5. The equivalent circuit model of TSV noise coupling with interconnect line.

The electrical schema presented in Figure 5 is composed of a lumped circuit model of TSV–TSV noise coupling in each die, two interconnect lines to distribute signals between dies, and I/O drivers modeled by Z_1, Z_2, Z_3, and Z_4.

As explained above, before applying the NILT method, the global T-matrix of the circuit must be found. The matrices T_{sub}, T_{tsv}, T_{tl}, T_3, and T_4 were used. First, T_1 and T_2 were calculated using Equations (18) and (19), respectively, then a transformation to Y_1 and Y_2 of T_1 and T_2, respectively, was made. This transformation was performed to find the global Y_g of the circuit without Z_1, Z_4, and Z_{tsv} near Z_1 and Z_4. Then another transformation from Y_g to T_g was performed. When finding T_g, it is multiplied by T_{tsv} on the left and right sides, and by using Equations (13), (14), and (21) V_2 is found according to V_{in}.

$$[T_1] = [T_{sub}].[T_3].[T_{tsv}].[T_{tl}].[T_{tsv}] \tag{24}$$

$$[T_2] = [T_{tsv}].[T_{tl}].[T_{tsv}].[T_4].[T_{sub}] \tag{25}$$

$$[Y_g] = [Y_1] + [Y_2] \tag{26}$$

$$V_2 = -Z_4.I_2 \tag{27}$$

where:

$$[T_{tl}] = \begin{bmatrix} \cos(\beta l) & jZ_0 \sin(\beta l) \\ j\sin(\beta l)/Z_0 & \cos(\beta l) \end{bmatrix} \tag{28}$$

where β is the propagation constant, l and Z_0 are the length and the characteristic impedance, respectively, of the interconnect line, and:

$$[T_{sub}] = \begin{bmatrix} 1 & Zeq \\ 0 & 1 \end{bmatrix} \tag{29}$$

$$[T_{tsv}] = \begin{bmatrix} 1 & Z_{tsv} \\ 0 & 1 \end{bmatrix} \tag{30}$$

$$[T_4] = \begin{bmatrix} 1 & 0 \\ \frac{1}{Z_4+Z_{tsv}} & 1 \end{bmatrix} \tag{31}$$

$$[T_3] = \begin{bmatrix} 1 & 0 \\ \frac{1}{Z_{tsv}+Z_3} & 1 \end{bmatrix} \tag{32}$$

To consider the coupling between the interconnect lines, the conceptual structure presented in Figure 4 is modeled by the lumped circuit model shown in Figure 6. In the schema, the interconnect lines are presented by the equivalent circuit model of RDL [21]. As already explained above, to apply the NILT method, the total T-matrix of the circuit was calculated and then the noise V_n according to V_{in} was found.

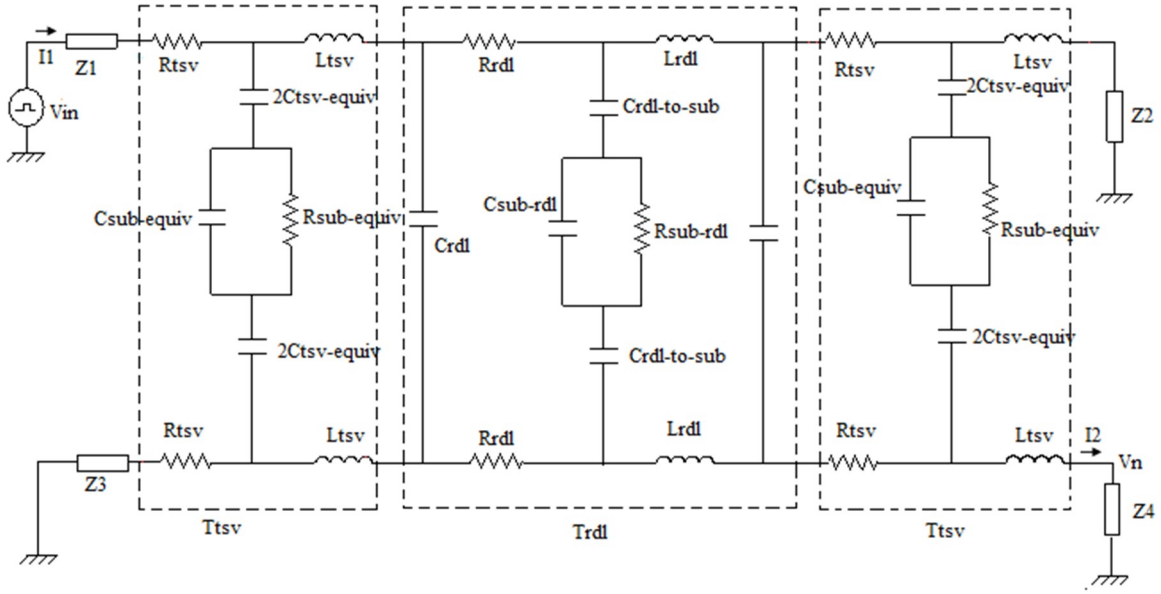

Figure 6. The equivalent circuit model of TSV noise coupling with redistribution layers (RDLs).

First, the total T-matrix, T_g, was computed as in Equation (23), then a transformation to Y_g was done to find the equivalent circuit of Figure 7. Hence, exploiting this figure and Equations (24)–(26), the noise V_n was calculated according to V_{in}.

$$\left[T_g\right] = [T_{tsv}].[T_{rdl}].[T_{tsv}] \tag{33}$$

$$\begin{pmatrix} I_1 \\ I_2 \end{pmatrix} = \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} \begin{pmatrix} V_1 \\ V_2 \end{pmatrix} \tag{34}$$

$$V_{in} = (Z_1 + Z_3)\, I_1 + V_1 \tag{35}$$

$$V_2 + \left(\frac{Z_4 + Z_2}{Z_4}\right) V_n = 0 \tag{36}$$

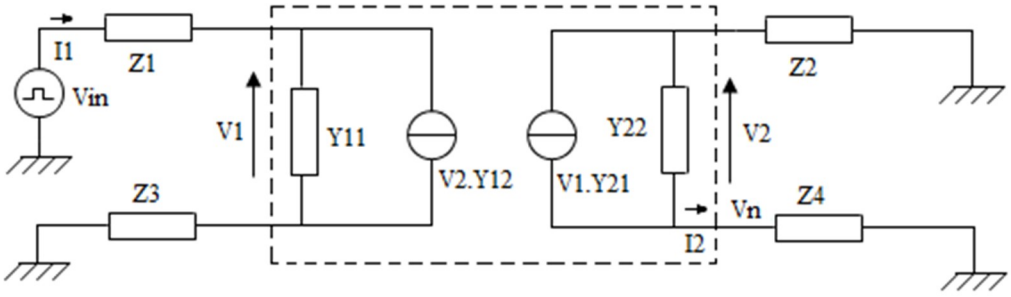

Figure 7. The admittance equivalent circuit of TSV noise coupling with RDLs.

The total admittance of all previous circuits could also be calculated, as mentioned in [37], before applying the NILT method.

The proposed method can be summarized in the diagram of Figure 8.

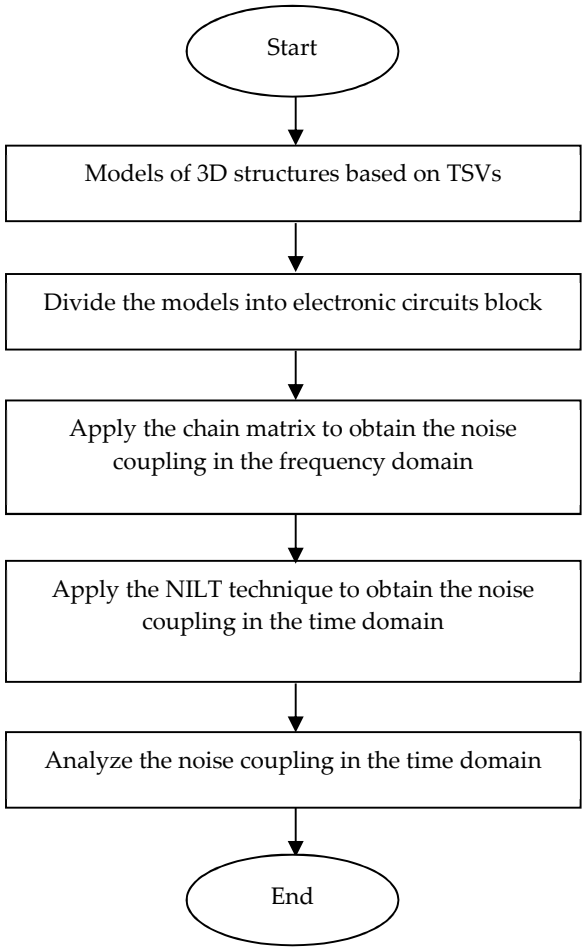

Figure 8. Block diagram of the proposed method.

3. Results and Discussions

In order to evaluate the effectiveness of the proposed method, simulation tests of the previous circuits were carried out. Simulations were performed with the Matlab and Pspice tools for all schemes, while the experimental tests of circuits 1 and 2 were taken from [13]. To take the measurements, the test vehicle in Figure 1 was fabricated using the Hynix via-last TSV process. The TSV circuit elements were calculated using the TLM-3D method; when the TSV diameter is 33 µm, the TSV pitch is 250 µm, the TSV dioxide thickness is 0.52 µm, and the TSV height is 105.2 µm. The RDL parameters were calculated using the method cited in [21]. Lumped circuit element values are listed in Tables 1–3. The accuracy and efficiency of the computing method were validated by simulations in Pspice and the measurements of [13].

Table 1. Lumped circuit elements of TSV–TSV noise coupling.

Component	Value
$C_{tsv\text{-}equi}$	201.3 fF
R_{tsv}	0.001 Ω
L_{tsv}	20.7 pH
$R_{sub\text{-}equi}$	928.5 Ω
$C_{sub\text{-}equiv}$	11.2 fF

Table 2. Lumped circuit elements of TSV–active circuit noise coupling.

Component	Value
$C_{tsv\text{-}equiv}$	817.5 fF
R_{tsv}	0.001 Ω
Ltsv	20.7 pH
$R_{sub\text{-}equiv}$	879.5 Ω
$C_{sub\text{-}equiv}$	12 fF

Table 3. Lumped circuit elements of the RDL.

Length of the Line	Component	Value
l_{RDL} = 200 µm	R_{rdl}	0.00672 Ω
	L_{rdl}	0.1664 nH
	C_{rdl}	7.66 fF
	$C_{rdl\text{-}to\text{-}sub}$	364.65 fF
	$C_{sub\text{-}rdl}$	0.13 fF
	$R_{sub\text{-}rdl}$	836.12 fF
l_{RDL} = 500 µm	R_{rdl}	0.0168 Ω
	L_{rdl}	0.42 nH
	C_{rdl}	19.15 fF
	$C_{rdl\text{-}to\text{-}sub}$	911.64 fF
	$C_{sub\text{-}rdl}$	0.33 fF
	$R_{sub\text{-}rdl}$	334.44 Ω

3.1. Validation of the Proposed Method

In order to verify the validity of the proposed method, it was applied first to the TSV–TSV and TSV–active circuit noise coupling circuits. The simulated waveforms of the electrical models of Figures 2 and 3 are shown in Figures 9–11. A trapezoidal signal switching from 0 to 1.8 V with a rising/falling time of 40 ps and a source resistance of 50 Ω at frequencies 100 MHz and 1 GHz is used. For a first test, Z_1, Z_2, Z_3, and Z_4 were replaced by resistances of 50 Ω.

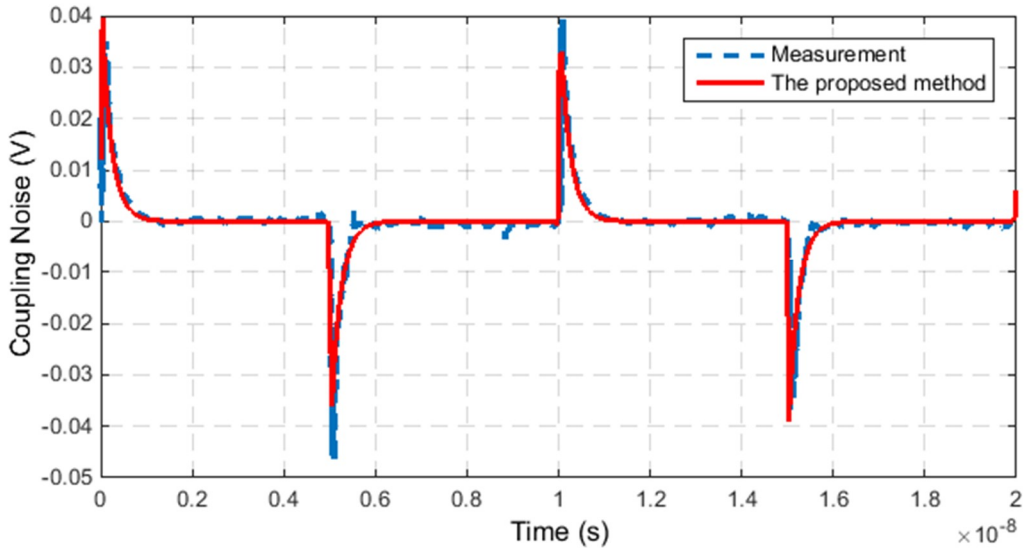

Figure 9. The proposed method and measured coupling of the TSV–TSV test vehicle (the input clock frequency is 100 MHz).

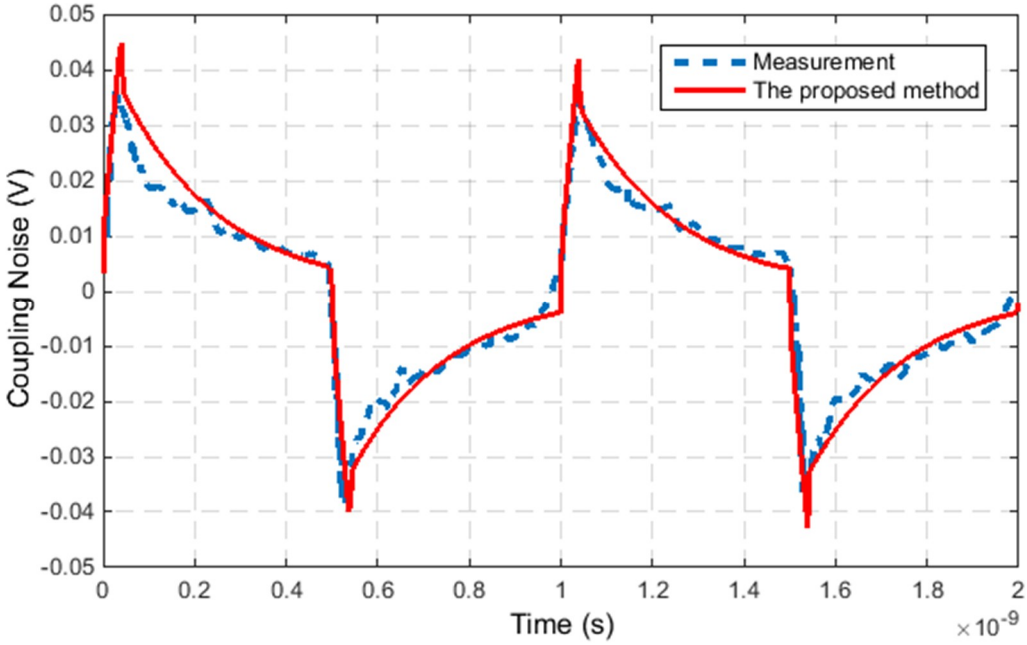

Figure 10. The proposed method and measured coupling of the TSV–TSV test vehicle (the input clock frequency at port 1 is 1 GHz).

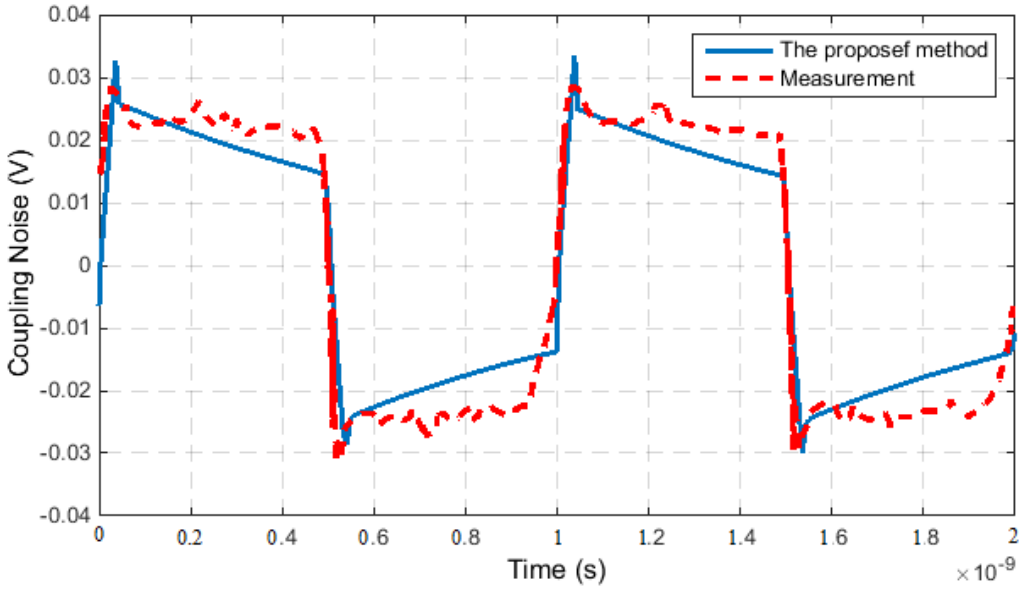

Figure 11. The proposed method and measured coupling noise of the TSV–active circuit (the input clock frequency at port 1 is 1 GHz).

Based on the results reported in the figures, it can be seen that the proposed method is in good agreement with the experiments. By analyzing these results, one can see that the proposed method is valid.

3.2. Time-Domain Analysis of the Coupling Noise with I/O Drivers Load

In Figures 9–11, the TSV coupling noise was computed based on the assumption that all TSVs are terminated with 50 Ω. However, TSVs are usually terminated with I/O drivers; therefore, the TSV I/O terminations must be considered as mentioned before. For the analysis, Z_2 and Z_4 were replaced by a capacitance of 10 fF. Figure 11 depicts the TSV–TSV noise coupling for a trapezoidal signal switching

from 0 to 1 V and from 0 to 1.8 V. The results show that the coupling noise increases when Z_2 and Z_4 are replaced by the capacitances. The peak-to-peak coupling noise increases from 80 mV (Figure 10) to 170 mV (Figure 12). The peak-to-peak coupling noise increases from 170 mV to 310 mV when the source changes from 1 V to 1.8 V. These results imply that the type of termination and the source significantly affects the coupling noise. The TSV I/O buffer size also influences TSV noise coupling and must be considered.

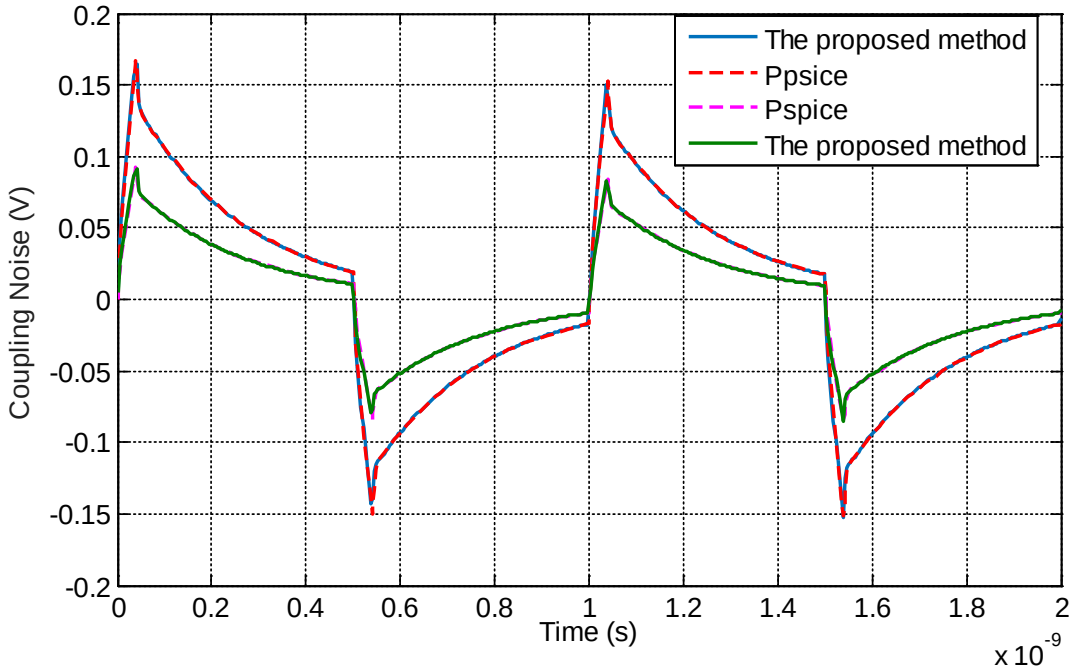

Figure 12. The proposed method and Pspice simulation of the coupling noise of TSV–TSV (V_{in} = 1 V and 1.8 V).

The RDL redistributes the signals to connect I/Os or power/ground when two different dies with via-last processed TSVs are integrated vertically. Therefore, for advanced 3D-IC design, analyzing TSV noise coupling with RDLs is very important.

The results found for the circuit presented in Figure 5 are illustrated in Figures 13–16 separately for l_{RDL} = 200 µm and l_{RDL} = 500 µm. These results present the TSV noise coupling without the coupling among the RDLs. A trapezoidal signal switching from 0 to 1.8 V with a rising/falling time of 10 ps and a source resistance of 50 Ω at frequency 1 GHz was used, Z_1 and Z_3 were replaced by resistances of 50 Ω, and Z_2 and Z_4 were replaced by capacitances of 10 fF.

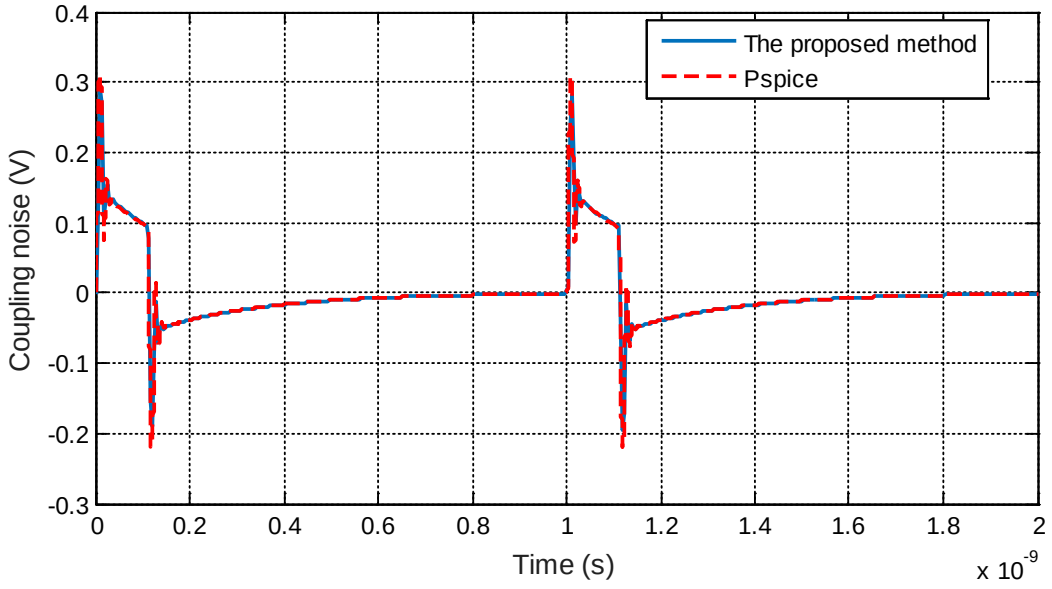

Figure 13. The proposed method and Pspice simulation of the TSV–TSV coupling noise with uncoupled RDLs (l_{RDL} = 200 μm) at port 4.

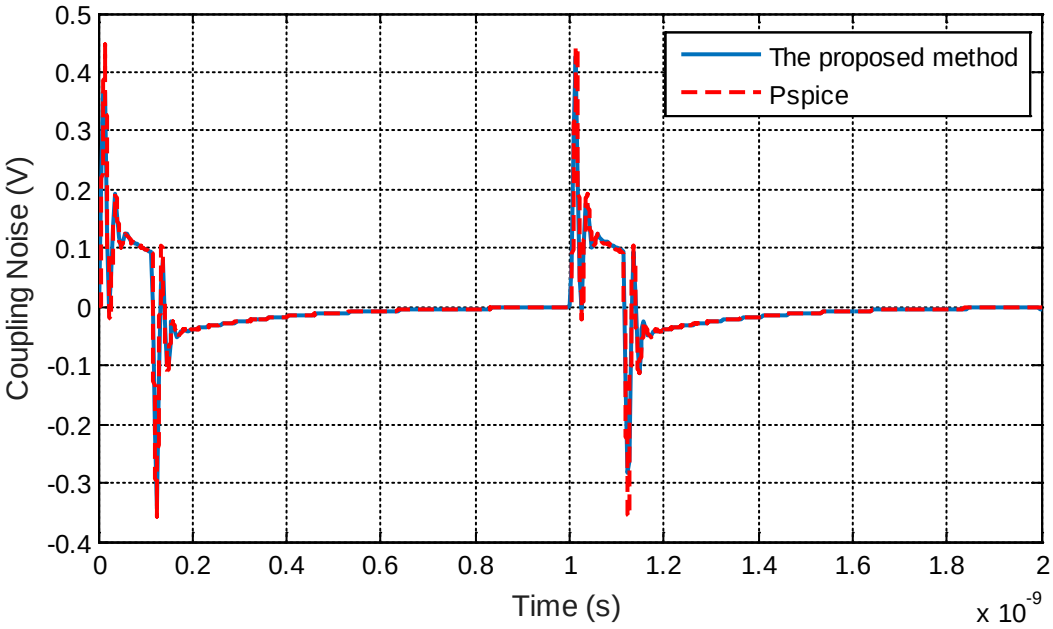

Figure 14. The proposed method and Pspice simulation of the TSV–TSV coupling noise with uncoupled RDLs (l_{RDL} = 500 μm) at port 4.

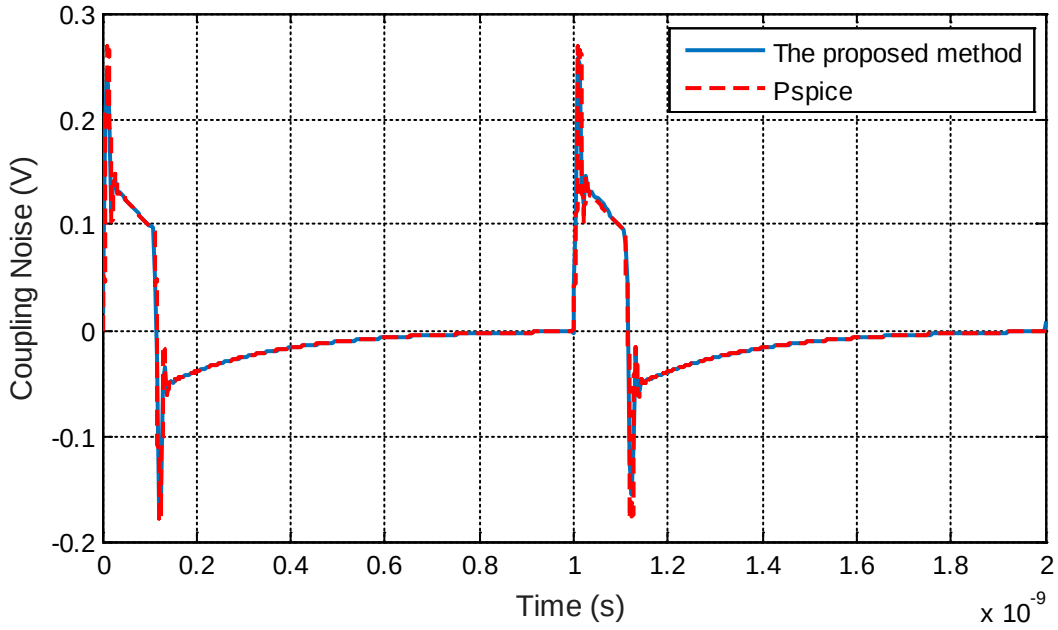

Figure 15. The proposed method and Pspice simulation of the TSV–TSV coupling noise with uncoupled RDLs (l_{RDL} = 200 µm) at port 3.

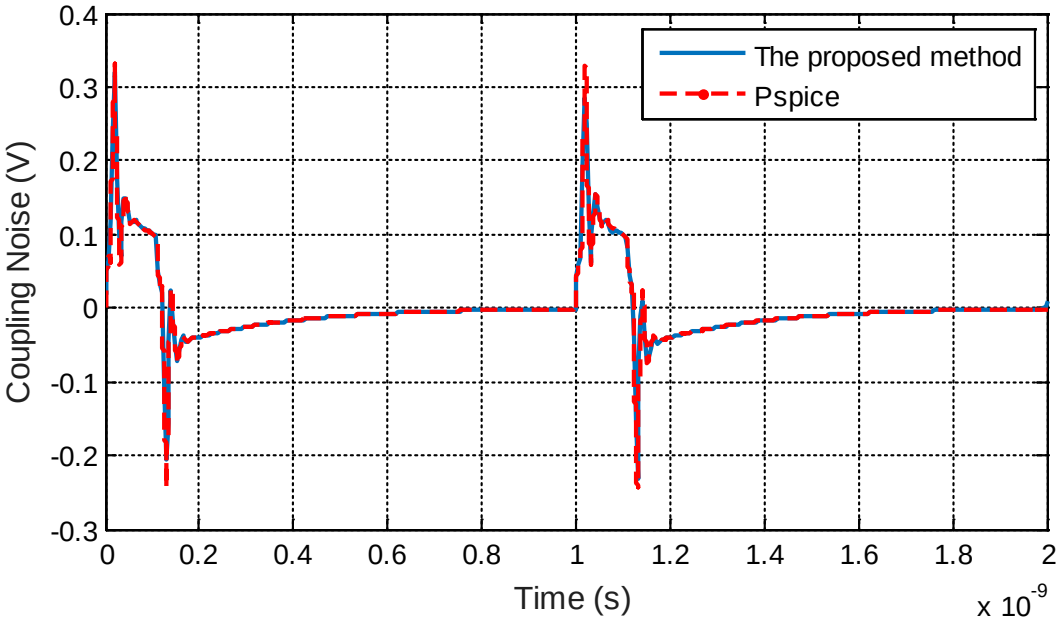

Figure 16. The proposed method and Pspice simulation of the TSV–TSV coupling noise with uncoupled RDLs (l_{RDL} = 500 µm) at port 3.

It is observed that the coupling noise spreads on the stacked dies through used interconnections. The peak-to-peak coupling noise increases from 50 mV to 80 mV when the length of the interconnect line (RDL) changes. It is also observed that both ports 3 and 4, which represent, respectively, the input and the output drivers, are affected by the coupling noise. By analyzing the obtained results, the presence of horizontal interconnections can add the coupling noise.

In high frequencies, coupling among the horizontal interconnections cannot be neglected. Indeed, a study including the coupling between the RDLs was done. The obtained results based on Figure 6 are depicted in Figures 17–19.

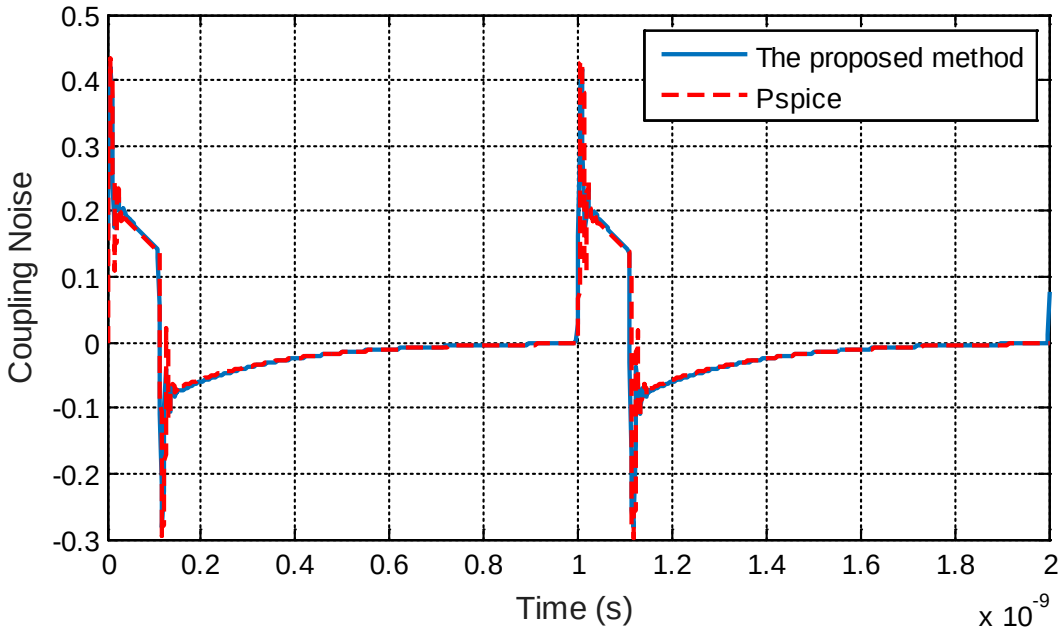

Figure 17. The proposed method and Pspice simulation of the TSV–TSV coupling noise with coupled RDLs (l_{RDL} = 200 μm and t_r = 10 ps) at port 4.

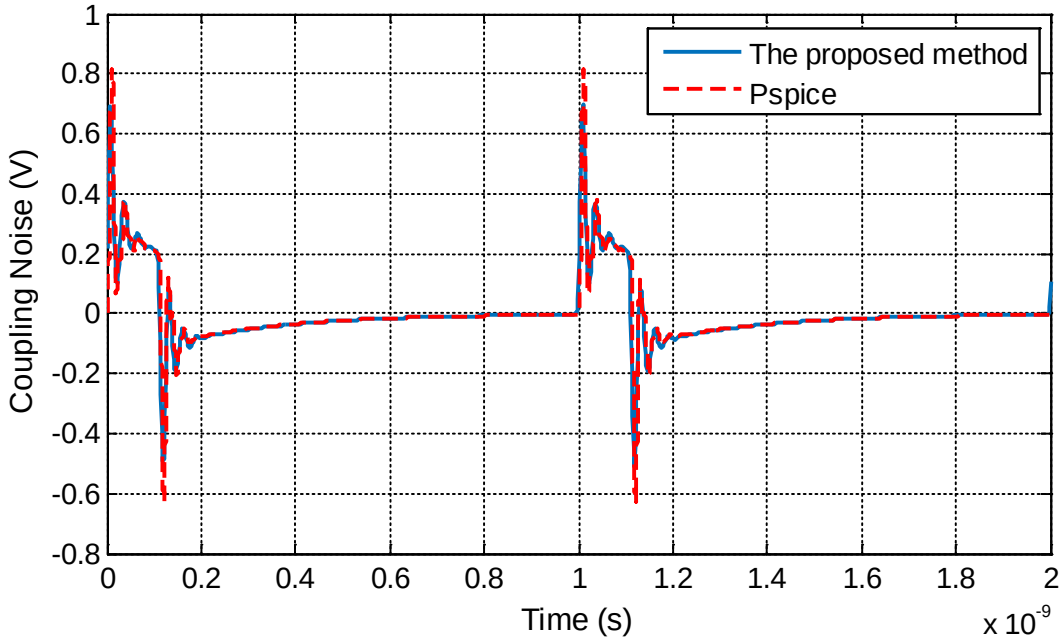

Figure 18. The proposed method and Pspice simulation of the TSV–TSV coupling noise with coupled RDLs (l_{RDL} = 500 μm and t_r = 10 ps) at port 4.

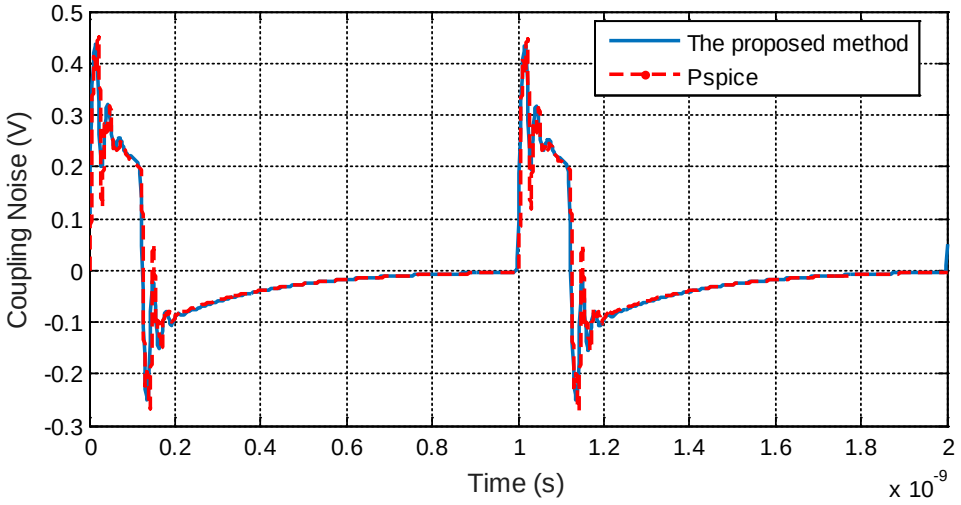

Figure 19. The proposed method and Pspice simulation of the TSV–TSV coupling noise with RDL (l_{RDL} = 500 μm and t_r = 20 ps) at port 4.

The simulations were done for different RDL lengths and several rise/fall time values. The noise was studied only at port 4.

Observing Figures 13 and 17, the peak-to-peak coupling noise increases when the coupling between RDLs is added. In addition, comparing the results of Figures 17 and 18, the peak-to-peak coupling noise increases when the RDL length increases. Simulation results of these case studies imply that, when the RDL length increases, the effect of the substrate elements among RDLs increases, and R_{RDL} and L_{RDL} change. Thus, the losses from the RDL are significant.

In a similar manner to the previous analysis, the effect of the rise/fall time variation is depicted in Figures 18–20. The results show that, as t_r increases from 10 ps to 20 ps and from 20 ps to 50 ps, pick-to-pick coupling noise decreases, respectively, from 1400 mV to 700 mV and from 700 mV to 550 mV. As a result, the rise/fall time is one of the most important factors that affect the TSV–TSV noise coupling in 3D-IC design.

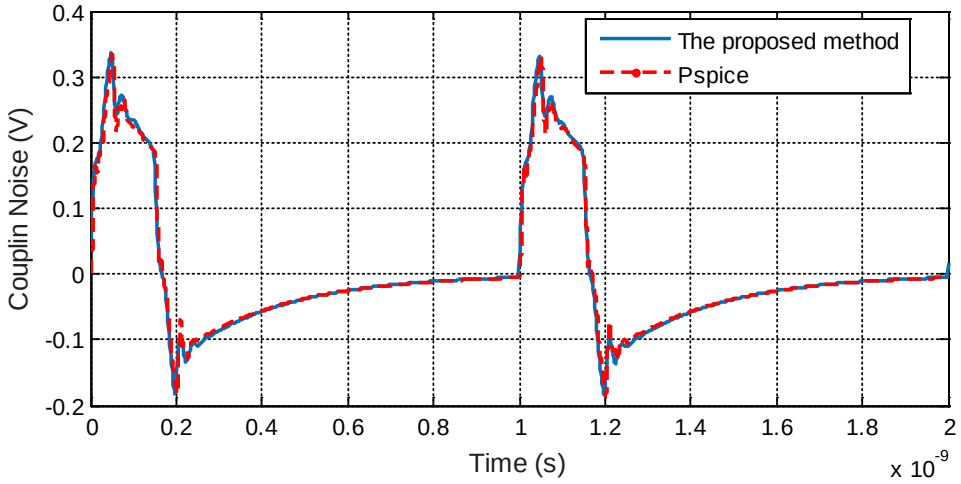

Figure 20. The proposed method and Pspice simulation of the TSV–TSV coupling noise with RDL (l_{RDL} = 500 μm and t_r = 50 ps) at port 4.

In summary, the method proposed to compute the coupling noise was validated using measurements and the Pspice and Matlab tools. Then, the time-domain analysis for several factors that must be considered was done.

4. Conclusions

In this paper, a method to compute the time-domain coupling noise in 3D-IC design has been proposed and explained in detail. The proposed method is based on 1D-NILT and chain matrices. It is effective and simple to apply. The used technique was validated using measurements of [13] and the Pspice tool.

The advantage of the proposed method is to compute the coupling noises of 3D structures based on TSVs, since transition phenomena are better observed in the time domain and not in the frequency domain.

A time domain analysis was done using several factors, such as different types of I/O drivers, the coupling between the horizontal interconnections, and the rise/fall time of the source. It was found that the type and the size of the TSV I/O buffer significantly influence the coupling noise. In addition, the presence of coupling between horizontal interconnections increases the noise at components of the 3D structures. These noises must be taken into consideration and must be minimized.

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