

Article

# Heterogeneous Integration of GaN and BCD Technologies

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**Abstract:** Light-emitting diodes (LEDs) are solid-state devices that are highly energy efficient, fast switching, have a small form factor, and can emit a specific wavelength of light. The ability to precisely control the wavelength of light emitted with the fabrication process enables LEDs to not only provide illumination, but also find applications in biology and life science research. To enable the new generation of LED devices, methods to improve the energy efficiency for possible battery operation and integration level for miniaturized lighting devices should be explored. This paper presents the first case of the heterogeneous integration of gallium nitride (GaN) power devices, both GaN LED and GaN transistor, with bipolar CMOS DMOS (BCD) circuits that can achieve this. To validate this concept, an LED driver was designed, implemented and verified experimentally. It features an output electrical power of 1.36 W and compact size of  $2.4 \times 4.4 \text{ mm}^2$ . The designed fully integrated LED lighting device emits visible light at a wavelength of approximately 454 nm and can therefore be adopted for biology research and life science applications.

**Keywords:** Bipolar CMOS DMOS (BCD); complementary metal oxide semiconductor (CMOS); gallium nitride (GaN); integrated circuits (ICs); LED driver; life science; linear voltage regulator

## 1. Introduction

The three main types of light bulbs in the lighting industry today are incandescent light bulbs, compact fluorescent lights (CFLs) and light-emitting diode (LED) bulbs. It has been shown that LED bulbs generally require significantly less electrical power compared to CFL or incandescent light bulbs. LED bulbs are also much more energy efficient and have a longer lifespan compared to other types of light bulbs [1]. Other than providing illumination with great energy savings, LEDs can play a significant role in smart cities, such as in the implementation of visible light communication (VLC) technology, where digital lighting is enhanced to complement radio frequency (RF) transmissions [2–6]. To enable the next generation of smart lighting, it is therefore crucial to explore methods that improve the energy efficiency of current integrated LED technology to reduce such costs.

Furthermore, the ability to precisely control the wavelength of light emitted through LEDs with the fabrication process can enable further advancements in areas previously inconceivable with traditional light sources. For instance, the use of blue LEDs (with a wavelength of 450–490 nm) in life science research has been shown to successfully inhibit the growth of skin tumours in the v-Ha-ras transgenic mouse [7] and improve wound healing in an excision model of rats [8]. In human biology research, it has

been proven that blue light emitted by high-power LEDs are selectively absorbed by the haemoglobin content of blood and then converted into heat, thus enabling the selective photocoagulation of superficial abrasions with reduced overall treatment time and scar formation [9]. In terms of life science application, a high-intensity collapsible phototherapy device for neonatal jaundice has been patented by Little Sparrows Technologies [10]. The portable device makes use of high-intensity blue light to trigger a chemical reaction that causes bilirubin in the bloodstream to become water soluble, allowing it to be filtered naturally in urine without liver processing.

The system block diagram for the typical LED lighting system shown in Figure 1 was presented in [11]. It should be noted that the intensity of the LED lighting depends on the current that is flowing through the device in forward bias condition.

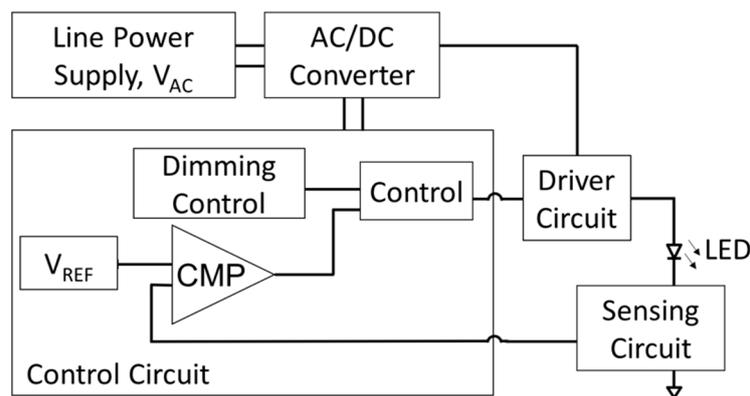


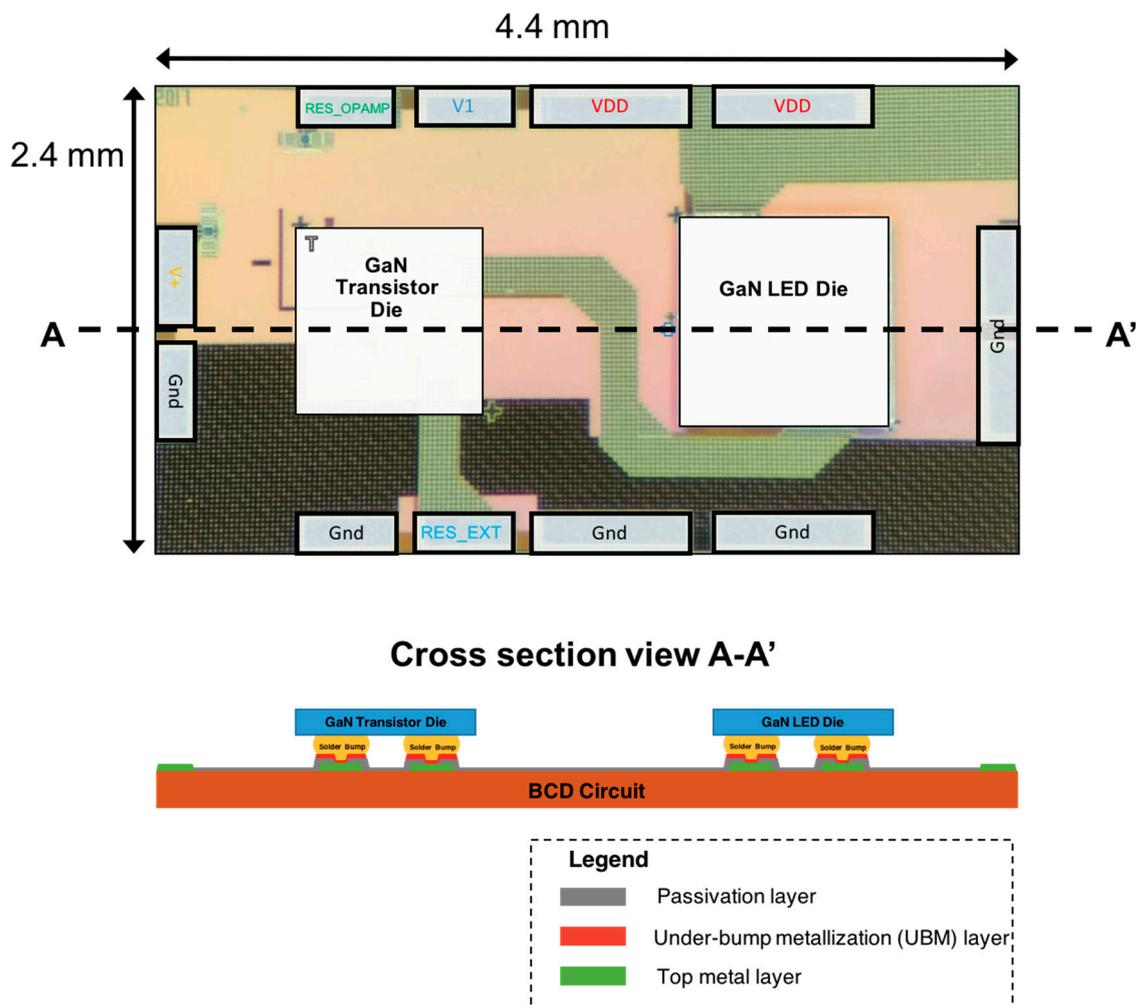
Figure 1. System block diagram of LED lighting.

The AC/DC converter in the system block diagram converts the AC supply power into DC power, which powers the control circuit for the LED. For hand-held application, battery power that supplies DC power can also be adopted. Since slight variations in the forward voltage can result in exponential effects on the forward current of an LED [12], it is more effective for LED driver circuitry to be current mode regulators.

Wide-bandgap semiconductors like GaN [13,14] and silicon carbide (SiC) [15] have successfully enabled power field effect transistors (FETs) with superior performances over silicon-based FETs [16,17]. Driven by Moore's law and advancements in semiconductor technologies, research into 3D integrated circuits (ICs), which includes the heterogeneous integration of wide-bandgap semiconductors with silicon technology, has become a hot research area [18]. The heterogeneous integration of III-V devices and complementary metal oxide semiconductor (CMOS) processes has been explored in the area of power electronics in recent years [19–21]. For instance, the Defense Advanced Research Projects Agency (DARPA) Diverse Accessible Heterogeneous Integration (DAHI) program has demonstrated InP chips integrated on CMOS chips through flip-chip bonding [22–24]. The direct integration of III-V devices on top of CMOS wafers has been shown to achieve better function complexities [25] as well as a reduction in board space required over conventional monolithic designs [26,27]. The on-chip integration of a GaN LED on CMOS driver circuits has also demonstrated lower packaging costs by eliminating the need for a ribbon cable to connect the LED and integrated circuit driver, reducing the number of required packages from two to one [28].

In this paper, the heterogeneous integration of both the GaN LED die and GaN transistor on top of the bipolar CMOS DMOS (BCD) driver IC is first reported. The GaN LED and GaN transistor are both directly mounted onto the BCD driver circuit via solder bumps such that they are stacked vertically, as shown in Figure 2. The integrated LED lighting device serves as a proof-of-concept that both GaN LED and GaN FET can be integrated on the BCD wafer without any process changes required during standard back end of line (BEOL) processing in the foundry. For approaches that

require heterogeneous integration happening before or during the BEOL processes, extensive process changes and budgets would be required in the foundry, posing difficulties to process adoption.



**Figure 2.** Microchip snapshot indicating bond pad layouts for GaN LED and GaN transistor to the bipolar CMOS DMOS (BCD) LED driver circuit with the cross-section sketch view of the GaN2BCD™ technology.

This work is enabled by GLOBALFOUNDRIES GaN2BCD™ Technology, and is transferable to other generic combinations of high-performance III-V devices and BCD chips. Since the GaN LED used in this prototype emits blue light with a wavelength of 454 nm, the designed fully integrated LED lighting device can potentially be used for future biological research applications. The design target of 350 mA was set for the LED driver so as to ensure that the LED die turns on with a minimum optical output power of 27.5 mW, which is more than the minimum output optical power of 5 mW for a single LED die used in human biology research to reduce scar formation [9]. The compactness of the designed prototype, given that the III-V devices are directly integrated on the chip level rather than on board level, provides the possibility of enabling hand-held devices in biomedical applications.

## 2. Materials and Methods

This section elaborates on the design of the LED driver, as well as the assembly of GaN elements to the BCD circuits.

### 2.1. LED Driver Design

To demonstrate the novel heterogeneous integration scheme, a 5 V-to-3.5 V linear voltage regulator was designed. The schematic of the linear voltage regulator is shown in Figure 3a. The objective of the LED driver is to maintain the current flowing through the GaN LED at 350 mA. The block diagram of the designed linear voltage regulator is shown in Figure 3b.

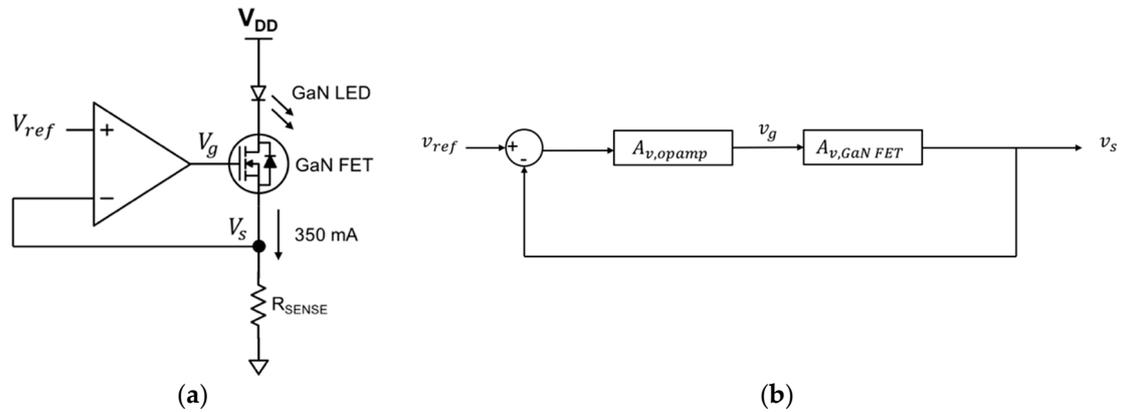


Figure 3. (a) Schematic and (b) block diagram of designed linear voltage regulator.

The transfer function of the linear voltage regulator is thus given as Equation (1):

$$\frac{v_s}{v_{ref}} = \frac{A_{v,opamp} A_{v,GaN FET}}{1 + A_{v,opamp} A_{v,GaN FET}} \tag{1}$$

To ensure accuracy, the value of  $A_{v,opamp} A_{v,GaN FET}$  must be sufficiently large such that  $\frac{v_s}{v_{ref}} \approx 1$ . The values of  $A_{v,opamp}$  and  $A_{v,GaN FET}$  are derived in the subsequent sections.

#### 2.1.1. Two-Stage Operational Amplifier (opamp)

The schematic of the two-stage opamp used in the LED driver is shown in Figure 4.

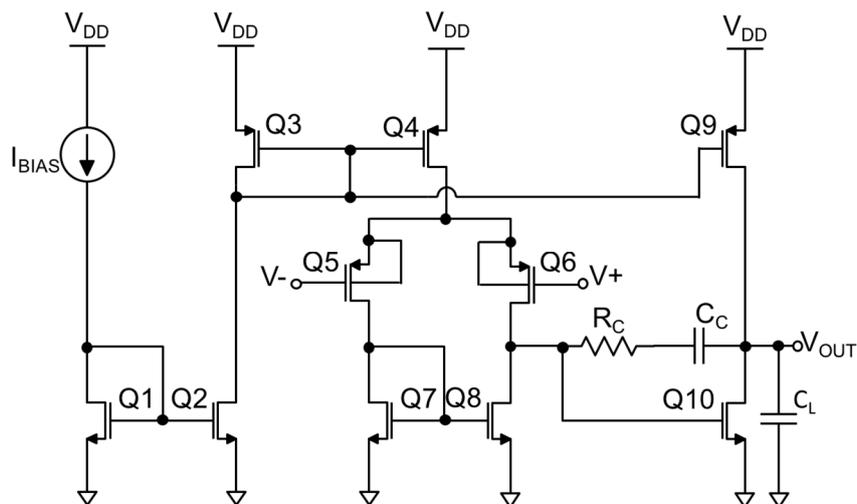


Figure 4. Schematic of the two-stage opamp.

For proper functionality, all transistors (Q1 to Q10) must be in saturation. Let  $S_i$  denote  $\frac{W_i}{L_i}$  of transistor  $Q_i$ . From Figure 4, transistors Q4 and Q9 form a current mirror with Q3. Therefore,  $I_3$  (current flowing through transistor Q3) determines the gate-to-source voltages of the current source

devices (Q3, Q4 and Q9). As such, these transistors will have the same gate-to-source voltage and their currents will be related by their dimensions.

$$I_4 = \frac{S_4}{S_3} I_3, \quad I_9 = \frac{S_9}{S_3} I_3 \quad (2)$$

Since Q5 and Q6 are symmetrical, the current  $I_4$  splits equally among them, as shown in Equation (3):

$$I_5 = \frac{I_4}{2} = I_6 = I_7 = I_8. \quad (3)$$

Since Q8 is the only transistor that cannot be forced into saturation by internal connections or external voltages, conditions to force Q8 into saturation are developed. Assuming that  $v_{gs,Q8} = v_{gs,Q10}$ , then

$$I_{10} = \frac{S_{10}}{S_8} I_8. \quad (4)$$

From Equation (2),

$$I_9 = \frac{S_9}{S_3} I_3 = \frac{S_9}{S_3} \left( \frac{S_3}{S_4} \right) I_4 = \frac{S_9}{S_4} I_4. \quad (5)$$

Since  $I_9 = I_{10}$ , combining Equations (3)–(5), the DC balance condition is derived.

$$\begin{aligned} I_9 = I_{10} &= \frac{S_{10}}{S_8} I_8 = \frac{S_9}{S_4} I_4, \\ \frac{S_{10}}{S_8} \left( \frac{I_4}{2} \right) &= \frac{S_9}{S_4} I_4, \\ \frac{S_{10}}{S_8} &= \frac{S_9}{S_4} \times 2. \end{aligned} \quad (6)$$

Assuming that the lengths of the transistors are kept the same, Equation (6) can be further simplified to

$$\frac{W_{10}}{W_8} = \frac{W_9}{W_4} \times 2. \quad (7)$$

With the DC balance condition fulfilled,  $V_{DG,Q8} = 0$ , hence transistor Q8 would be operating in saturation mode.

The small signal equivalent circuit of the two-stage opamp shown in Figure 4 is illustrated in Figure 5.

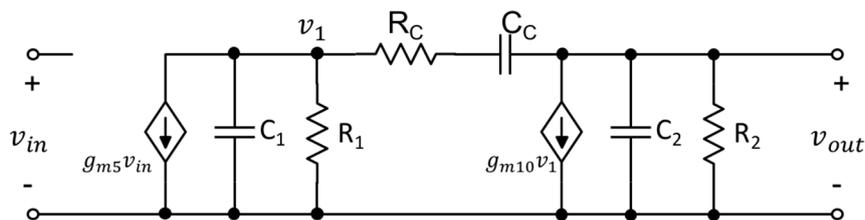


Figure 5. Small signal equivalent circuit of the two-stage opamp.

The values of  $R_1$ ,  $C_1$ ,  $R_2$  and  $C_2$  are derived as shown in Equation (8):

$$\begin{aligned} R_1 &= r_{ds,Q6} \parallel r_{ds,Q8}, \\ C_1 &= C_{db,Q6} + C_{db,Q8} + C_{gs,Q8} + C_{gs,Q10} + C_{gd,Q6} + C_{gd,Q8}, \\ R_2 &= r_{ds,Q9} \parallel r_{ds,Q10}, \\ C_2 &= C_{db,Q10} + C_{db,Q9} + C_{gd,Q9} + C_{gd,Q10} + C_L, \\ C_L &= C_{ISS} + C_P, \end{aligned} \quad (8)$$

where

$C_{ISS}$  = input capacitance of GaN FET,  
 $C_p$  = parasitic capacitance.

In order to improve the closed-loop stability of the two-stage opamp, Miller compensation (in the form of  $C_c$ ) is implemented. By connecting a capacitor across the high-gain stage shown in Figure 6, the pole-splitting phenomenon occurs by moving the dominant pole to a lower frequency, as illustrated in Figure 7.

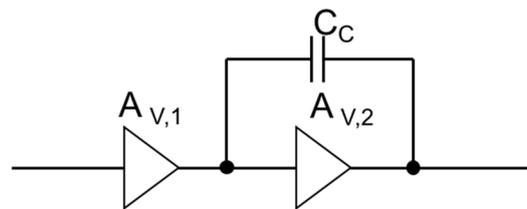


Figure 6. Miller compensation.

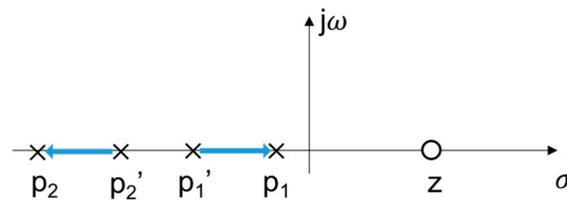


Figure 7. Pole splitting phenomenon due to Miller compensation.

However, due to the feed-forward path through the Miller capacitor ( $C_c$ ), a right-half-plane (RHP) zero is also created. To obtain the frequency response of the two-stage opamp, we assumed  $R_c = 0$ , hence

$$A_{v,opamp}(s) = \frac{v_{out}}{v_{in}} = \frac{g_{m,Q5}g_{m,Q10}R_1R_2 \left(1 - \frac{sC_c}{g_{m,Q9}}\right)}{1 + as + bs^2}, \tag{9}$$

where

$$a = (C_2 + C_C)R_2 + (C_1 + C_c)R_1 + g_{m,Q10}R_1R_2C_c,$$

$$b = R_1R_2(C_1C_2 + C_1C_c + C_2C_C).$$

Assuming that the two poles are widely separated, the denominator of Equation (9) can be represented as

$$D(s) = \left(1 + \frac{s}{\omega_{P1}}\right) \left(1 + \frac{s}{\omega_{P2}}\right) \approx 1 + \frac{s}{\omega_{P1}} + \frac{s^2}{\omega_{P1}\omega_{P2}}. \tag{10}$$

The frequencies at which the two poles and zero are located can therefore be derived using Equation (11) [29]:

$$\omega_{P1} \approx \frac{1}{R_1[C_1 + C_C(1 + g_{m,Q10}R_2)] + R_2(C_2 + C_c)}$$

$$\approx \frac{1}{R_1C_C(1 + g_{m,Q10}R_2)} \approx \frac{1}{R_1R_2C_cg_{m,Q10}}, \tag{11}$$

$$\omega_{P2} \approx \frac{g_{m,Q10}C_c}{C_1C_C + C_2C_C + C_1C_c} \approx \frac{g_{m,Q10}}{C_1 + C_2},$$

$$\omega_Z = \frac{-g_{m,Q10}}{C_c}.$$

Note that Miller compensation comes from the feedback path through  $C_c$  but the RHP zero is from the feed-forward path through  $C_c$ . As a result, lead compensation using  $R_c$  was used such that RHP zero was moved to be slightly larger than the unity gain frequency.

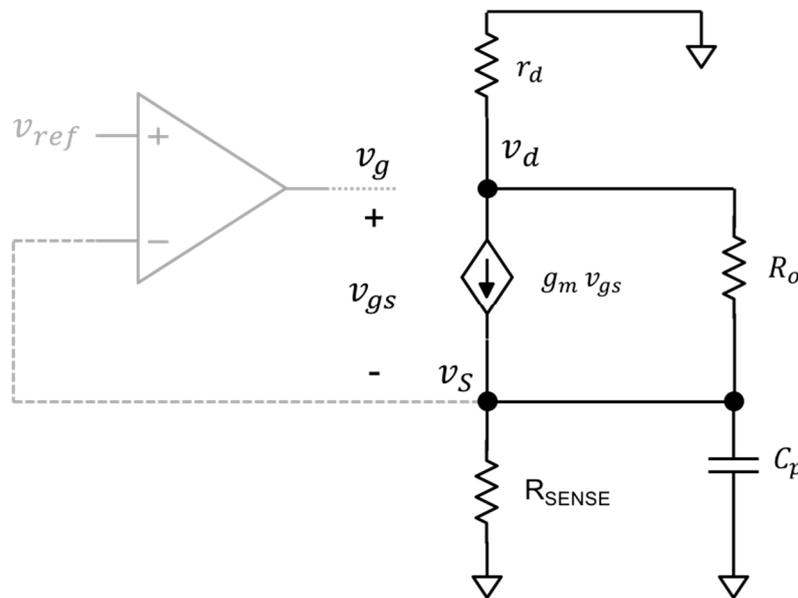
From Equation (9), the DC gain can be derived as

$$\text{DC Gain} = A_{v,opamp} = \frac{V_G}{V_{ref} - V_s} = g_{m,Q5}g_{m,Q10}R_1R_2. \tag{12}$$

DC gain was designed to be more than 60 dB in order to ensure accuracy when the opamp is used in the feedback loop of the LED driver shown in Figure 3b. The phase margin of the opamp is also designed to be higher than 60° to guarantee stability in the feedback loop. In order to achieve higher gain with lower power consumption, an opamp with folder-cascode topology can be utilised [30,31].

### 2.1.2. GaN FET Common Drain Stage

The small signal diagram of the GaN FET common drain stage is shown in Figure 8.



**Figure 8.** Small signal equivalent circuit of the GaN field effect transistor (FET) common drain stage.

The GaN LED was modelled as a voltage source with a series resistance of  $r_d$ .  $r_d$  that can be estimated from the slope of the I-V curve of the GaN LED in the forward biased region.

Applying Kirchoff’s current law (KCL) at  $v_s$ ,

$$\frac{v_d - v_s}{R_o} + g_m v_{gs} = \frac{v_s}{R_{SENSE}} + sC_p v_s. \tag{13}$$

Applying KCL at  $v_d$ ,

$$\frac{-v_d}{r_d} = g_m v_{gs} + \frac{v_d - v_s}{R_o}. \tag{14}$$

From Equation (14),

$$\begin{aligned} g_m v_{gs} &= \frac{v_d}{R_o} + \frac{v_d}{r_d} + \frac{v_s}{R_o}, \\ v_d &= \frac{g_m v_{gs} + \frac{v_s}{R_o}}{\left(\frac{1}{R_o} + \frac{1}{r_d}\right)} \\ &= \frac{R_o r_d g_m v_{gs} + r_d v_s}{R_o + r_d}. \end{aligned} \tag{15}$$

Substituting Equation (15) into Equation (13),

$$\frac{r_d g_m v_{gs}}{R_o + r_d} + \frac{r_d v_s}{R_o (R_o + r_d)} - \frac{v_s}{R_o} + g_m v_{gs} = \frac{v_s}{R_{SENSE}} + sC_p v_s. \tag{16}$$

Since  $v_{gs} = v_g - v_s$ , Equation (16) can be further evaluated as follows

$$\frac{r_d g_m v_g}{R_o + r_d} - \frac{r_d g_m v_s}{R_o + r_d} + \frac{r_d v_s}{R_o(R_o + r_d)} - \frac{v_s}{R_o} + g_m v_g - g_m v_s = \frac{v_s}{R_{SENSE}} + sC_p v_s,$$

$$v_s \left( \frac{1}{R_{SENSE}} + sC_p + \frac{r_d g_m}{R_o + r_d} + \frac{r_d}{R_o(R_o + r_d)} + \frac{1}{R_o} + g_m \right) = v_g \left( \frac{r_d g_m}{R_o + r_d} + g_m \right).$$

Therefore, the transfer function of the common drain stage can be obtained as shown in Equation (17):

$$A_{v,GaN FET}(s) = \frac{v_s}{v_g} = \frac{\frac{r_d g_m}{R_o + r_d} + g_m}{\frac{1}{R_{SENSE}} + sC_p + \frac{r_d g_m}{R_o + r_d} + \frac{r_d}{R_o(R_o + r_d)} + \frac{1}{R_o} + g_m}. \tag{17}$$

### 2.1.3. Stability Analysis

The LED driver was designed to be a stable negative-feedback system. The loop response time, which is related to dynamic specifications such as the line and load response of the regulator, is determined by its frequency behaviour. The major pole in the linear voltage regulator is determined by the two-stage opamp output and the load capacitance consisting of the gate capacitance of the pass transistor (GaN FET) and parasitic capacitances. The parasitic capacitances are mainly from flip-chip bonding and printed circuit board (PCB). The two-stage opamp has an output resistance which, due to the large capacitance at its output (coming mainly from the GaN FET), shunts and creates a pole at low frequency. The frequencies at which the major pole locates can be derived with Equation (18):

$$\omega_{Pole1} = \frac{1}{R_2 C_L}. \tag{18}$$

From Equation (18), it can be observed that changes in  $C_{ISS}$  can move the dominant pole. Note that the input capacitance of the selected GaN FET can differ from 75 to 90 pF [29]. As such, it is crucial to ensure that the designed Miller-compensated two-stage opamp is able to compensate for the changes in the input capacitance of the GaN FET.

### 2.2. Assembly of GaN Transistor

The enhancement mode (normally off) EPC2036 GaN FET [32] was chosen to be the power transistor used in the LED driver circuit described in Figure 3a. The packaged die form of the EPC2036 GaN FET is shown in Figure 9. The top metallisation layer of the design was laid out to form pad terminals matched to the gate, drain and source terminals of the GaN transistor. This was done to enable the flip-chip bonding of the GaN transistor die to the bipolar CMOS DMOS (BCD) circuit, as shown in Figure 2.

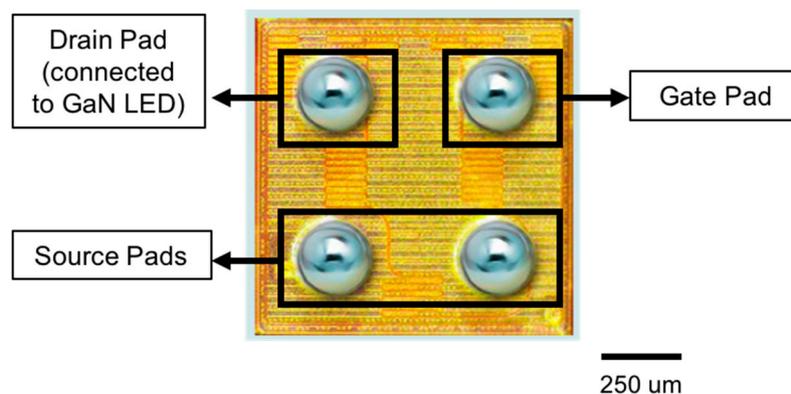
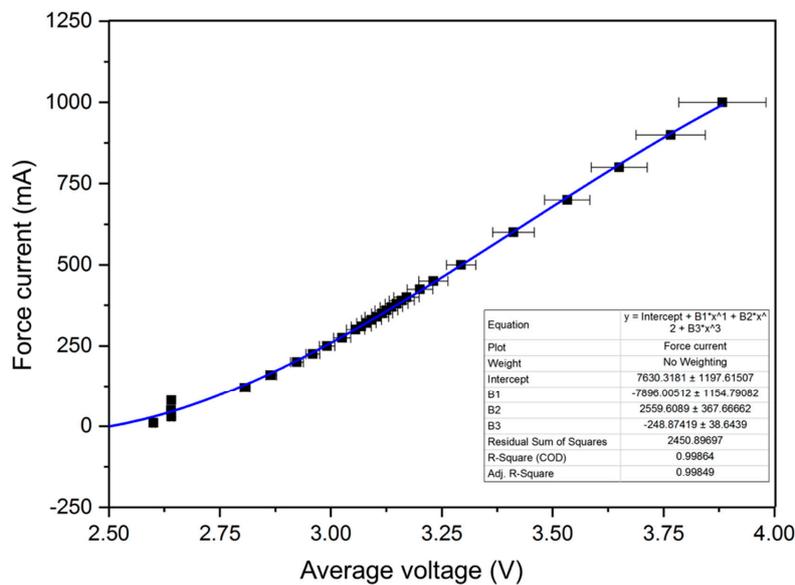


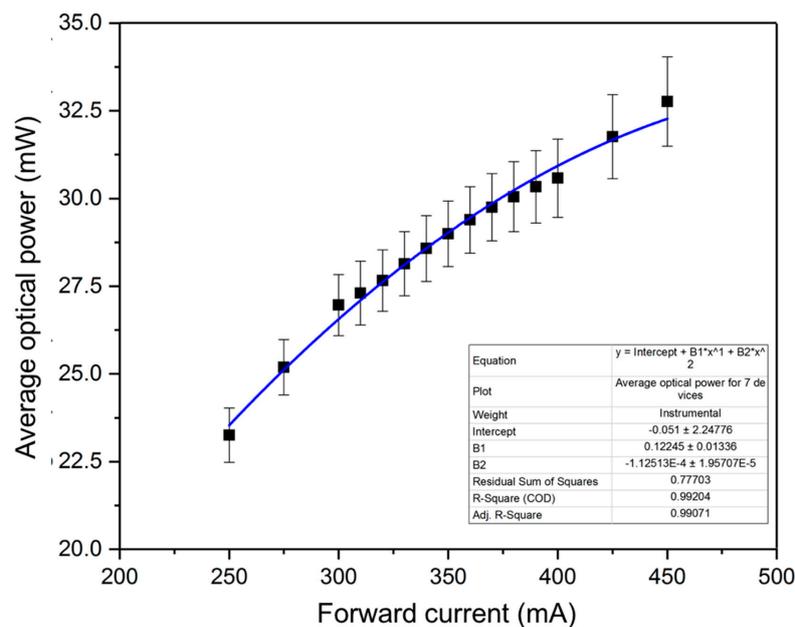
Figure 9. EPC2036 in passivated die form with solder bumps.

### 2.3. Fabrication and Assembly of Custom GaN LED

As the GaN LED has to be flip-chip bonded to the BCD circuit, a custom GaN LED (approximately 1 mm × 1 mm size) was designed and fabricated such that both the anode and cathode terminals were on the top surface. The GaN high-power LEDs were fabricated on 2-inch sapphire substrates with top metal pads having a thick gold (Au) finish that is suitable for solder bumping to the BCD circuits. In addition, the LEDs were fabricated using a transparent sapphire substrate to prevent the blocking of light emission by the sapphire substrate after the flip-chip bonding process. The measured graph of forward bias current versus average forward bias voltage of seven LED devices is shown in Figure 10. Figure 11 presents the measured graph of the average optical power for seven custom GaN LED devices versus forward bias current. The GaN LED device emits visible light at a wavelength of approximately 454 nm.



**Figure 10.** Measured forward bias current versus average forward bias voltage of seven custom GaN LED devices.



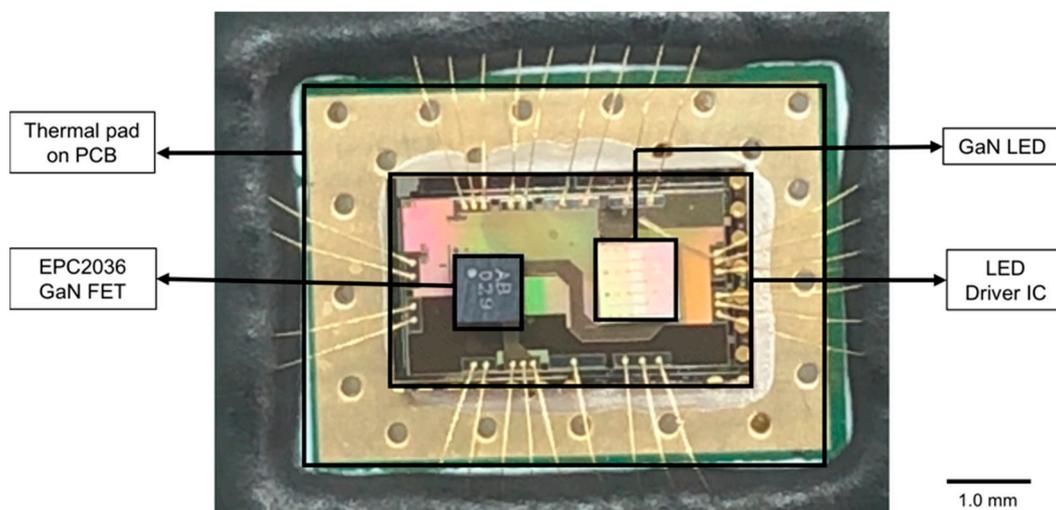
**Figure 11.** Measured average optical power for seven custom GaN LED devices versus forward bias current.

#### 2.4. Physical Implementation of Driver IC Using BCD Technology

The driver IC was fabricated in-house using GLOBALFOUNDRIES 0.18- $\mu\text{m}$  BCDlite™ technology. After the wafer fabrication process, an under-bump metallisation (UBM) layer was formed on top of the top metal metallization layer in order to enable on-chip wafer-level integration as shown in Figure 2. The heterogeneous integration process involved the application of solder, flip-chip placement of both GaN LED and GaN transistor on top of the BCD circuit as well as a solder reflow process. Both the GaN LED chip and GaN transistor chip were first bonded on the wafer-level, followed by wafer dicing. As the EPC2036 GaN FET comes in the passivated die form with solder bumps as shown in Figure 9, the application of solder to its terminals was not required. The flip-chip bonding process was similar to the flip-chip bonding process described for micro-LED display systems [33,34], except that the wafers went through further processing after the BEOL processes to form a UBM layer on top of the top metal layer of the BCD driver IC, as shown in Figure 2. The UBM layer serves multiple functions: as an adhesion layer, a diffusion layer and as a solder wettable layer [35]. Figure 2 shows the pad layouts for bonding both the GaN FET and the GaN LED on top of the BCD LED driver circuit.

#### 2.5. PCB Design and Prototype

To verify the functionality of the integrated LED design and validate the GaN2BCD™ technology, a printed circuit board (PCB) evaluation board was designed. In this PCB, the LED driver IC was affixed to the PCB evaluation board after the UBM process and flip-chip bonding was completed. Dedicated input/output (IO) pads were designed to meet the high current flow requirement. The integrated LED was then wire-bonded to the back side of the PCB evaluation board as shown in Figure 12 (zoom in). The IC had a compact size of  $2.4 \times 4.4 \text{ mm}^2$ . PCB assembly was then performed to fabricate the PCB evaluation board shown in Figure 13. The PCB evaluation board had a compact size of  $50 \times 50 \text{ mm}^2$ . From Figure 12, it is noted that there was still space between the GaN LED and the GaN FET due to machine constraints, which can be reduced in the future.



**Figure 12.** LED driver integrated circuit (IC) wire-bonded to the printed circuit board (PCB) evaluation board.

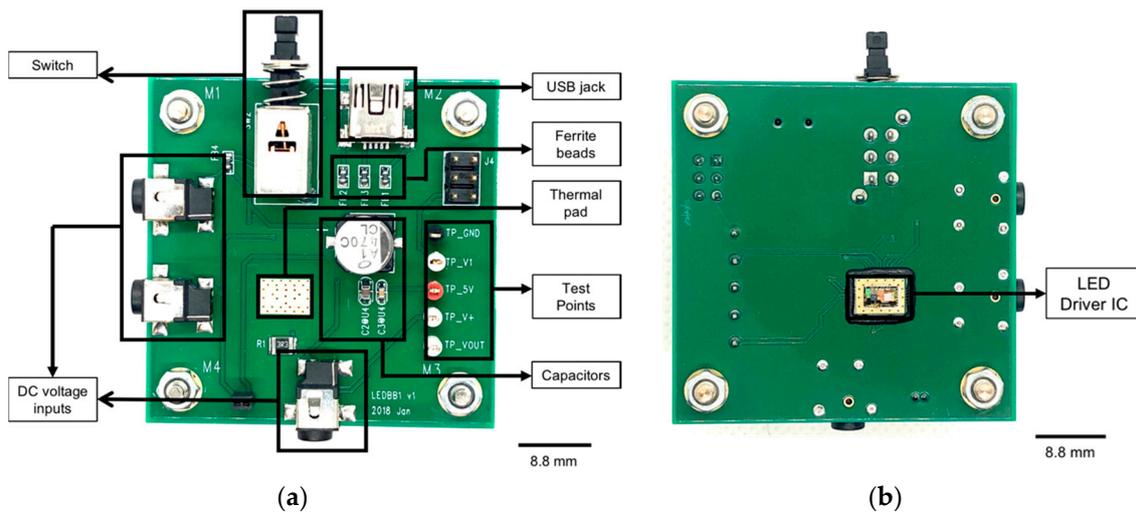


Figure 13. (a) Front side and (b) back side of PCB evaluation board.

### 3. Results

This section discusses the experimental results obtained from the operation of the designed LED driver.

#### 3.1. Functionality

The measured LED current was 353 mA, which successfully met the design target of 350 mA  $\pm$ 5% with an accuracy error of less than 0.85% without tuning. The efficiency of the integrated LED driver was estimated using Equation (19) and found to be 76.8%. Based on this value, the expected battery lifetime using two VARTA V4903 batteries [36] at 350 mA and 3 V was approximately 1.954 h using the battery life calculator available at Digikey’s website [37]. The efficiency of the integrated LED driver can be further improved by reducing  $R_{SENSE}$  shown in Figure 3a.

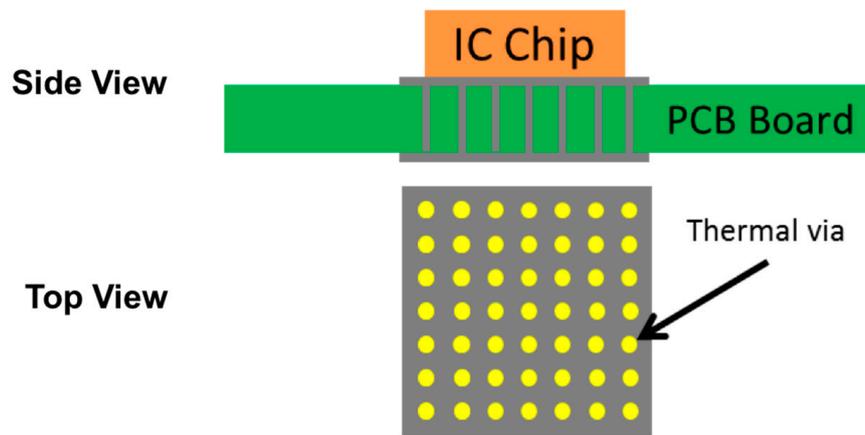
$$\eta = \frac{P_{LED}}{P_{Total}} \times 100\% = \frac{P_{Total} - I_{LED}^2 \times R_{SENSE} - P_{disp}}{P_{Total}} \times 100\%, \tag{19}$$

where

- $P_{LED}$  = power emitted by the LED,
- $P_{Total}$  = power dissipated by the integrated LED,
- $I_{LED}$  = current flowing through the LED,
- $R_{SENSE}$  = resistance value of sensing resistor,
- $P_{disp}$  = power dissipated by GaN FET.

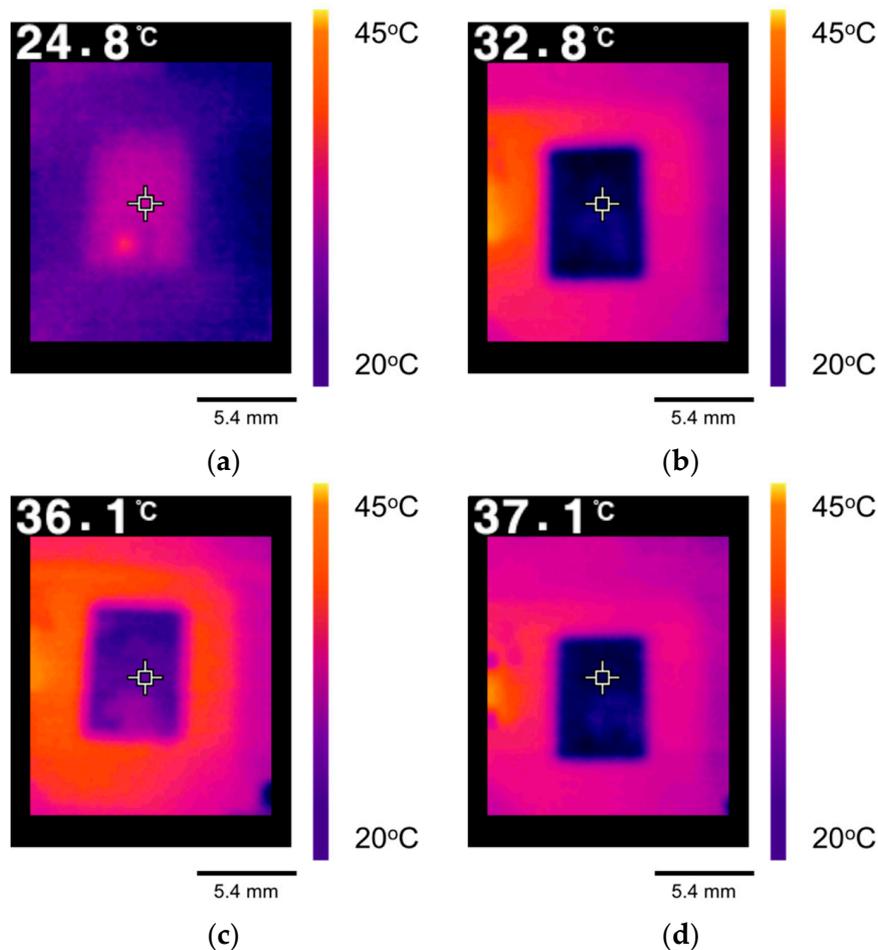
#### 3.2. Thermal Testing

A common concern in using GaN devices (GaN FET, GaN LED etc.) is heat dissipation. This section discusses the results of thermal testing for the dedicated thermal pad that was designed for thermal heat dissipation as shown in Figure 13a. The thermal pad refers to the copper pad on the PCB that was designed to enhance heat transfer away from the IC chip. The measured thermal pad was located on the reverse side of the IC and was connected to the pad directly below the IC chip via thermal vias as shown in Figure 14.



**Figure 14.** Positioning and layout of thermal pads and thermal vias on PCB.

Infrared (IR) imaging was conducted before and after operation of the LED driver using a FLIR TG165 [38] to monitor the surface temperature. Thermal testing was conducted based on careful calibration with a Digi-Sense Model 20250-03 thermocouple [39], to ensure that the temperature recorded by the IR thermometer matched that on the thermocouple so as to factor in surface emissivity [40]. Figure 15 shows the IR image of the thermal pad at 0, 30, 180 and 300 min intervals while the circuit was operating. The graph, which depicts the temperature of the thermal pad on the evaluation board against time, is shown in Figure 16.



**Figure 15.** IR image of thermal pad (a) before operation, (b) after 30 min operation, (c) after 3 h operation and (d) after 5 h operation.

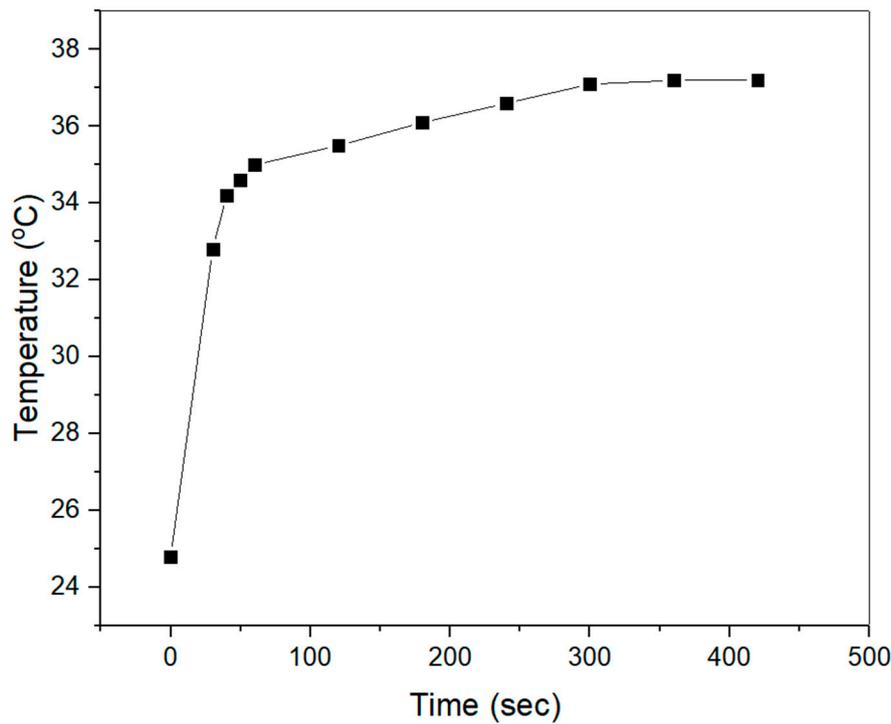


Figure 16. Graph of thermal pad temperature of on the evaluation board against time.

From the thermal results, it can be observed that the maximal surface temperature was 37.1 °C. In addition, there was a 12.3 °C increment in the board surface temperature over 5 h of operation. Based on the most utilised standard for consumer electronics devices (IEC’s 60950-1 (2005) [41]), the maximum surface temperature of any device for human touch is 70 °C. As such, it can be concluded that the maximal surface temperature of 37.1 °C in the designed evaluation board is acceptable for industrial consumer electronics applications.

#### 4. Discussion

A comparison table comparing the nominal current and maximum efficiency of on-board integrated LED drivers, which are linear current regulators, with the chosen technical solution (i.e., on-chip integrated), is shown in Table 1 below.

Table 1. Comparisons between on-board integrated LED drivers with the chosen technical solution.

LED Drivers	Yi-Hua Fan, 2006 [42]	Jingjie Shen, 2011 [43]	Philips [44]	This Work
Nominal Driving Current (mA)	350	350	332–368	350
Efficiency	78.6	73.1	80.0	76.8

Note that the measured efficiency of the designed integrated LED lighting device was slightly lower compared with other on-board integrated LED drivers. It is expected that better thermal dissipation methods and improvements made on the driving circuitry can help to narrow the gap in performance. For instance, the use of diamond-added AgSnCu solder materials for chip package coupled with a high thermal conductive metal-core printed circuit board (MCPCB), where the conventional dielectric layer was replaced with a thin diamond-like layer, has been shown to improve thermal heat dissipation [45]. Furthermore, resonance topologies can be utilised to improve the efficiency value [46,47].

## 5. Conclusions

This paper presents the first case of the heterogeneous integration of GaN power devices, both GaN LED and GaN transistor with BCD circuits. The integrated LED lighting device using a 5 V-to-3.5 V linear voltage regulator was designed and fabricated using the GLOBALFOUNDRIES GaN2BCD™ technology. It features an output electrical power of 1.36 W, stable thermal performance and a compact size of  $2.4 \times 4.4 \text{ mm}^2$ . The lighting device emits visible light at a wavelength of approximately 454 nm, and is a promising platform for biological and life science applications. Furthermore, other wavelength devices with different turn-on voltages can be integrated with the design by adjusting  $V_{ref}$  or  $R_{SENSE}$ . Future plans involve improving the efficiency of the integrated LED driver via better thermal dissipation methods and improving the driving circuitry.

**Author Contributions:** M.Y.S. and T.H.T. conceived, designed, implemented and tested the integrated LED circuits and system; S.L.S., L.P., D.D. and K.S.Y. contributed to the heterogeneous integration concept and specification.

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**Conflicts of Interest:** The authors declare no conflict of interest.

## Abbreviations

The following abbreviations are used in this manuscript:

BCD	Bipolar CMOS DMOS
BEOL	Back End of Line
CFL	Compact Fluorescent Lights
CMOS	Complementary Metal Oxide Semiconductor
DAHI	Diverse Accessible Heterogeneous Integration
DARPA	Defense Advanced Research Projects Agency
DMOS	Double-Diffused Metal Oxide Semiconductor
FET	Field Effect Transistor
EDB	Economic Development Board
IC	Integrated Circuits
IO	Input/Output
IR	Infrared
KCL	Kirchhoff's Current Law
LED	Light Emitting Diode
MCPCB	Metal-Core Printed Circuit Board
NTU	Nanyang Technological University
PCB	Printed Circuit Board
RF	Radio Frequency
SUTD	Singapore University of Technology and Design
UBM	Under-Bump Metallization

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