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A Highly Robust Interface Circuit for Resistive Sensors

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Abstract: The signal from a resistive sensor must be converted into a digital signal to be compatible with a computer through an interface circuit. Resistance-to-Period converter, used as interface, is preferred if the resistance variations are very large. This paper presents the structure of an interface circuit for resistive sensors that is highly robust to component and power supply variations. Robustness is achieved by using the ratiometric approach, thus complex circuits or highly accurate voltage references are not necessary. To validate the proposed approach, a prototype was implemented using discrete components. Measurements were carried out considering a variation of ±35% in the single supply voltage and a range from 1 kΩ to 1 MΩ.

Keywords: Resistance-to-Period converter; robust read-out circuits; ratiometric technique

1. Introduction

In recent years, the demand for sensors has increased in many areas, from medical and consumer electronics to automotive and industrial applications. In particular, resistive sensors are widely used in the industry for the measurement of displacement, strain, flow, force, pressure, temperature, light, weight, humidity, gas concentration and moisture, among others. Their resistance may vary from a few tens Ω such as thermistors, strain gauges, Resistance Temperature Detectors (RTD), piezo-resistive sensors, etc., to several MΩ such as various gas chemiresistive sensors, light dependent resistors (LDR), soil moisture, etc. To assess the resistive parameter, voltage may be applied across the sensor while the current is read or vice versa. Then, this voltage or current must be converted into a digital domain to be compatible with a computer, DAQ system, microcontroller or microprocessor using an interface.

According to [1], direct measurement of resistance changes can be done by two different ways: In the case of small resistance variations, circuits based on voltage dividers and Wheatstone bridges followed by precision differential or instrumentation amplifiers to reduce the offset voltage are used. This results in large and complex configurations and linearization techniques must be applied due to the intrinsic limitation in the dynamic range [2–4]. In contrast, quasi-digital converters, i.e., resistance-to-frequency [5,6], -period [7,8] or -duty-cycle [9] converters, are preferred if the resistance variations are very large. This converters not only provide a wider dynamic range but also simplify interfacing to digital systems, as no analog-to-digital converters (ADCs) are required [10,11]. In this way, the resistance is measured indirectly using a simple digital counter.

Most of the quasi-digital converters proposed in the literature focus on achieving a wide dynamic range (e.g., [12–16]), whereas other issues such as robustness and simplicity have not been

fully addressed, as required for low-cost, low-power readout circuits for practical implementations. Accuracy and robustness of most quasi-digital converters strongly depend on a bandgap voltage reference or on high performance building blocks, such as low-offset and high-speed comparators, resulting in higher complexity and/or power consumption [17,18]. In fact, the few papers on these converters found in the literature that consider robustness to voltage variations suffer from these disadvantages [19–22]. In this paper, the ratiometric concept is applied to achieve robustness to component and power supply variations without increasing complexity and without the use of bandgap circuits. The ratiometric approach is a common technique for measuring analog signals from sensors, to be conditioned in a digital signal to be compatible with a computer, DAQ system, microcontroller or microprocessor [23–26]. The advantage of the ratiometric approach is that it avoids the need for internal regulators, which reduces energy consumption and costs, but one disadvantage is that the dynamic range of the output depends on the supply voltage, and would be a major problem where the supply voltage decreases continuously, e.g., in autonomous portable equipment.

The aim of this study was to design a low-cost and versatile interface for resistive sensors, offering both wide operative range and robustness to component and power supply variations. The result is a simple, compact, low-cost, low-voltage and low-power solution.

The paper is organized as follows: after the introduction in Section 1, the proposed approach is described in Section 2 An implementation with discrete devices following the proposed approach is described in Section 3. Section 4 shows the measurement results of a prototype. Finally, the conclusion is provided in Section 5.

2. Circuit Description and Operation

The principle of the proposed resistive sensor interface is shown in Figure 1, which is implemented using a Resistance-to-Current (R-I) converter and a Current Controlled Oscillator (CCO). In the R-I converter, V_{bias} provides a constant voltage to biasing the sensor R_S and produces a current inversely proportional to the sensor resistance $I_{out}(R_S) = V_{bias}/R_S$. This current charges and discharges a capacitor C, generating a triangular signal $V_C(t)$ whose slope depends on the current. $V_C(t)$ is compared with a reference voltage V_{ref} to generate a square wave, $T_{out}(I_{out})$, whose period is proportional to the resistance variation.

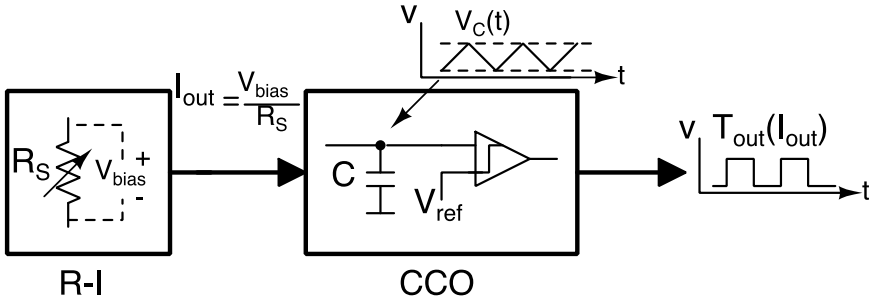

Figure 1. Block diagram of the proposed resistive sensor interface.

In Figure 2, an implementation of a Resistance-to-Current converter is shown. It is used to give an output current inversely proportional to the sensor resistance. The high open-loop gain of the amplifier will force the Gate of M1 to the required voltage such that V_{bias} appears across R_S. The current in R_S will be V_{bias}/R_S. This will flow only in the source of the transistor M1 and will be replied at its drain. Finally, it is mirrored by the current mirror with a gain of $1/\beta$. In this way, output current is equal to

$$I_{out} = \frac{I_{in}}{\beta} = \frac{V_{bias}}{R_S \beta}. \quad (1)$$

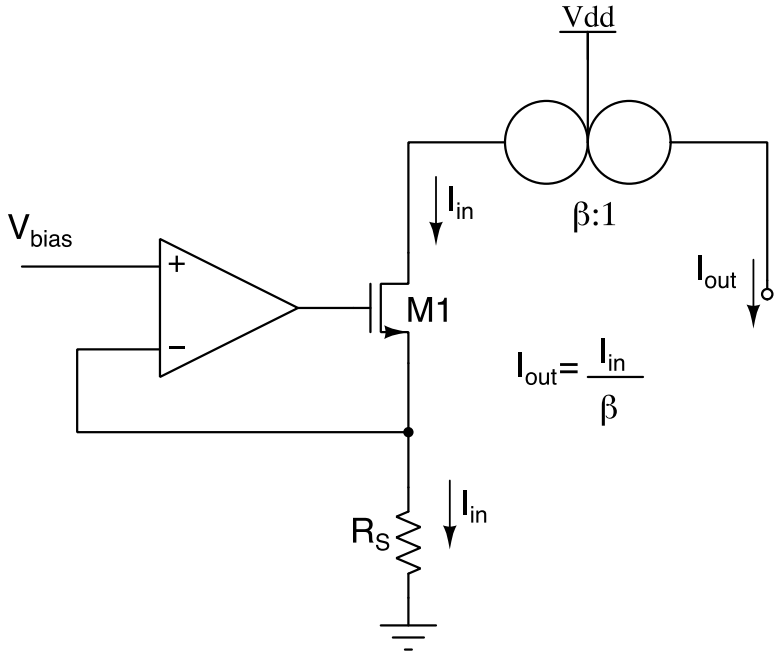

Figure 2. R-I converter.

The output current, I_{out}, will charge and discharge a capacitor C through a switch (SW1), which changes depending of the comparator output, as can be seen in Figure 3. The Voltage across the capacitor C, $V_C(t)$ is compared with a reference voltage V_H when it is charged and to another reference voltage V_L when it is discharged, being $V_H > V_L$. Each time $V_C(t)$ reaches V_H or V_L, the direction of the current through the capacitor is reversed. Therefore, the period of the output signal is given by

$$T_{out} = \frac{2C(V_H - V_L)}{I_{out}}, \tag{2}$$

where C is the capacitance from capacitor C.

Substituting Equation (1) into Equation (2),

$$T_{out} = \frac{2CR_S\beta(V_H - V_L)}{V_{bias}}. \tag{3}$$

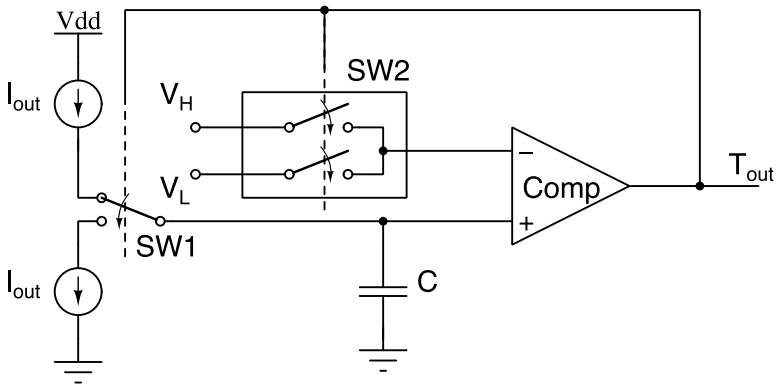

Figure 3. Implementation of the Current Controlled Oscillator.

To avoid the need for robust voltage reference, for V_{bias} implementation, the ratiometric approach is applied by using the same voltage reference for both the first block and the second block, i.e., $V_{bias} = (V_H - V_L)$. Thus, the period of the output signal is now given by

$$T_{out} = 2CR_S\beta. \tag{4}$$

In this way, the proposed architecture produces an output independent of any reference voltage, and no bandgap circuit is required. This reduces complexity, cost and power consumption of the system.

Minimal capacitance tolerance in commercial capacitors (ΔC) is 0.5%, so the maximum error is equal the same value. Additionally, error due to the delay in the comparator and switches is considered by adding a delay factor, t_d. To consider errors due to variations on the capacitor and delays, the period of the output signal of the proposed interface is given by:

$$T_{out} = 2(C \pm \Delta C)\beta R_S + t_d. \tag{5}$$

The switches that control the reference level (SW2) were implemented with a pair of complementary transistors. In this way, the change in the reference level is faster than the change in the integration sign, avoiding a deadlock situation, as shown in Figure 4. The change in the integration sign can be seen as a negative feedback mechanism, as the integrator output voltage changes backward. In turn, the change in the reference level is a positive feedback mechanism since it is the action that makes the whole system regenerative. In the ideal case, both actions occur at the same time, as depicted in Figure 4a; however, in real circuits, both feedbacks have a delay. When the output voltage of the integrator becomes higher than the high reference voltage, two actions are performed: switch the sign of the integrated constant and switch the reference voltage. If the reference voltage does not change faster than the sign of the integrated constant, the output voltage of the integrator will cross the high reference voltage again, leading to a deadlock state, as illustrated in Figure 4b. To avoid a deadlock situation, the positive feedback loop has to be stronger than the negative feedback mechanism to ensure that the transition to the next state takes place, as shown in Figure 4c [27].

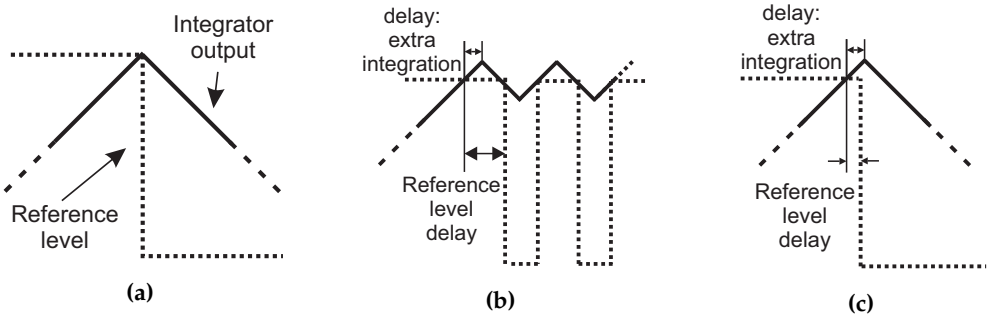

Figure 4. Transitions of both feedback loop. (**a**) Ideal case; (**b**) Deadlock situation; (**c**) No deadlock situation.

3. Proposed Circuit

This section presents an implementation designed with discrete devices to demonstrate the potential of the proposed architecture.

A variation of a linear voltage to current converter [28] shown in Figure 5 was used to implement the current mirror of Figure 2. Therefore, I_{out} is now

$$I_{out} = \frac{I_{in}R_1}{R_2}. \tag{6}$$

Thus,

$$\beta = \frac{R_2}{R_1}. \tag{7}$$

The maximum error in β is $\pm 1.4\%$ considering that commercial resistor have a minimum tolerance of 1%.

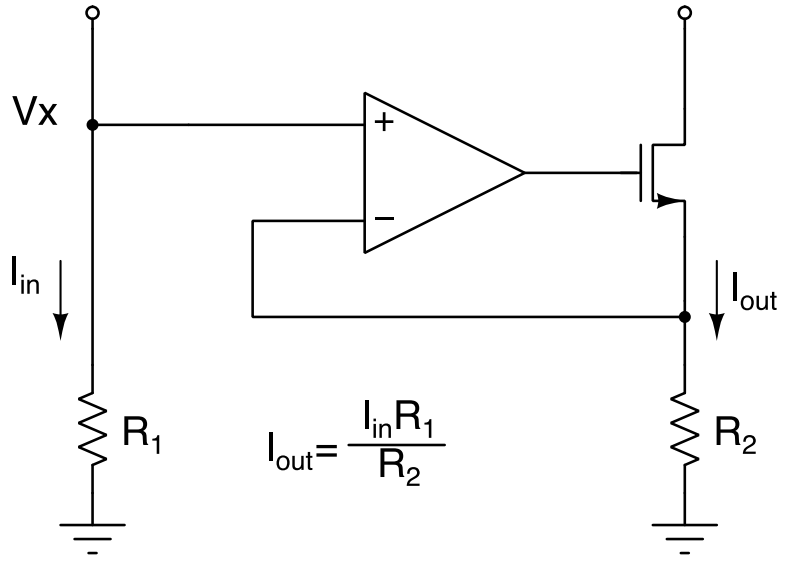

Figure 5. Current mirror implementation.

The complete resistive sensor interface is shown in Figure 6. The R-I converter consists of one resistor ladder (R_{ladder}), two amplifiers (A1 and A2) and two current mirrors (CM1 and CM2). The voltage across the resistive sensor R_S is set by amplifiers A1 and A2. The current $I(R_S)$ flowing through the sensor is driven to M1 and M2, and then current mirrors are used to improve accuracy of the copy. In this way, the current injected to or subtracted from the capacitor C remains almost independent of the variations in $V_C(t)$. The CCO consists of one comparator (comp), two switches (SW1 and SW2) and two NOT gates. The circuit that controls the current flow direction (SW1) was implemented using complementary transistors (M4 and M5). The switches that set the appropriate reference voltage level (V_H or V_L), were implemented with transmission gates to ensure that the change in the reference level is faster than the change in the integration sign.

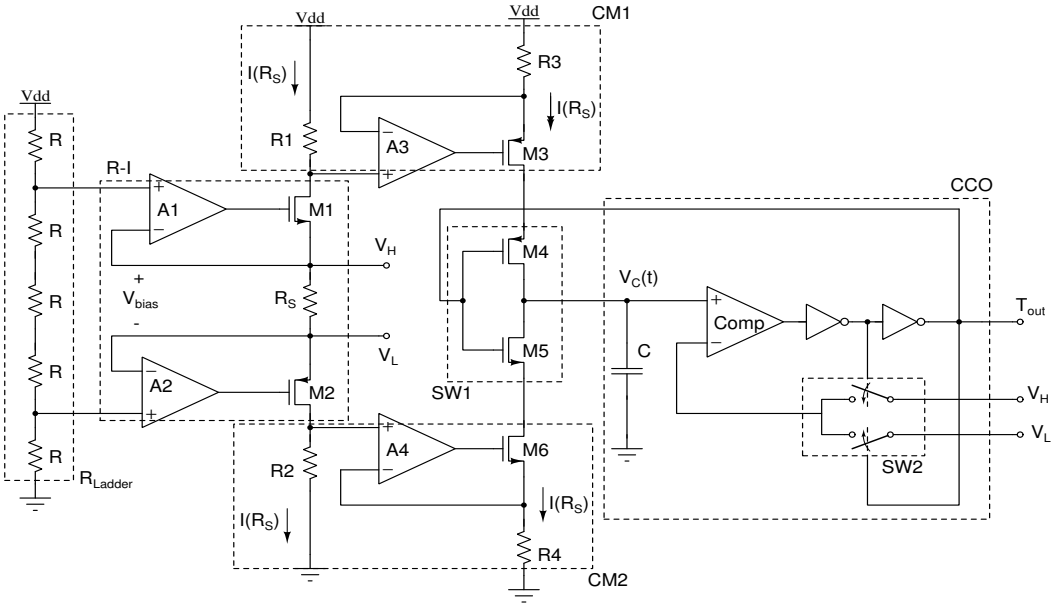

Figure 6. The proposed approach.

4. Experiments and Results

The proposed architecture was simulated in LTspice and realized with a discrete component prototype to test it. The component choice for building the prototype was done under constraints

of compactness, single-supply voltage operation and low cost. The component selection includes quad-operational amplifiers (LM324), complementary enhancement mode field effect transistors (AO4614) and precision resistors of 1 kΩ. Both NOT gates were implemented using complementary transistors. Finally, a capacitor C of 100 nF (with 5% accuracy) was used. A picture of the realized printed circuit board (PCB) is shown in Figure 7. Optimizations could therefore be made to further improve the circuit compactness.

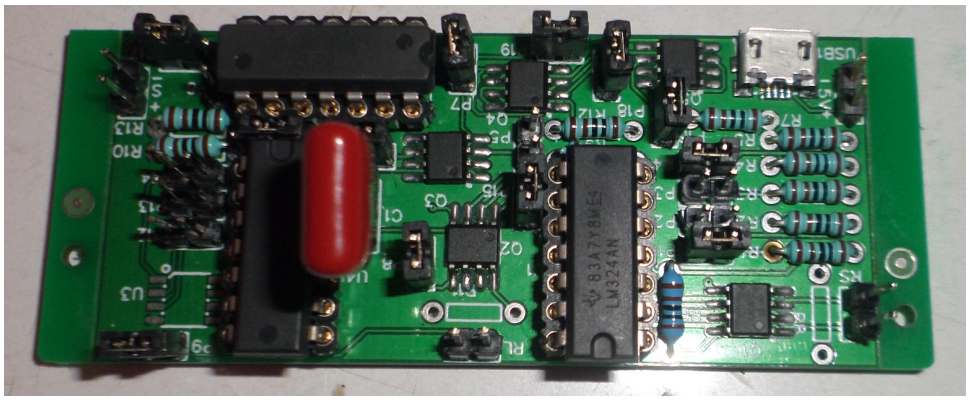

Figure 7. PCB from proposed circuit implementation.

For the experimental setup a DC Power Supply from BK PRECISION to power the circuit and a TDS1002 Mixed Signal Oscilloscope from Tektronix and a 5491A Digital Count-Multimeter from BK PRECISION to analyze the output signal were used. Experimental set-up is shown in Figure 8.

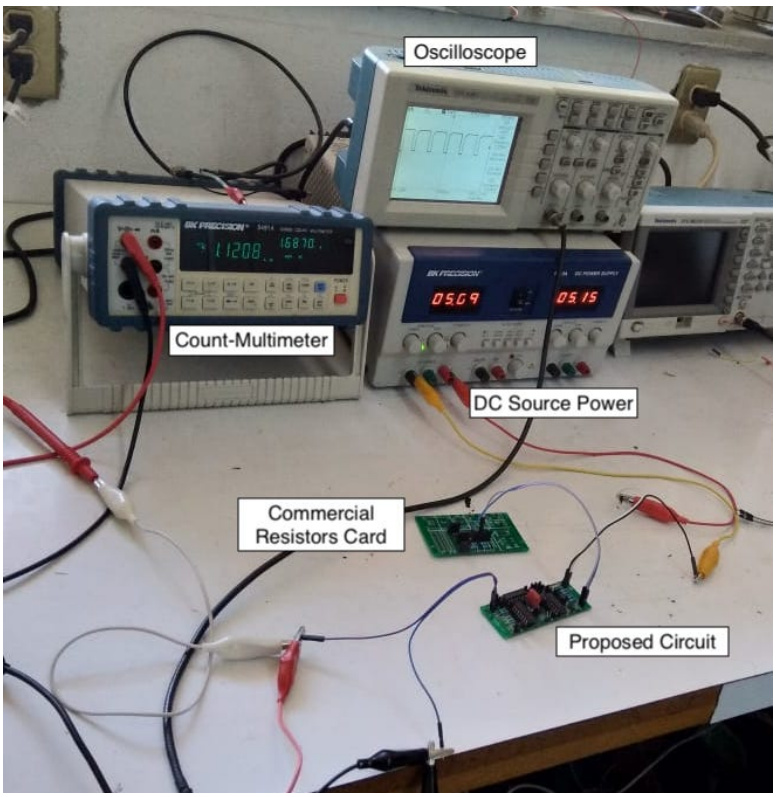

Figure 8. Experimental setup.

The converter was tested with sample resistors R_S (ranging from 1 kΩ to 100 MΩ with 1% accuracy) to emulate the sensor. Commercial resistors were used, whose values were previously determined with a 5491A Digital Multimeter from BK PRECISION. To measure output signal and to evaluate the

system performance in terms of relative standard deviation and linearity, multiple-period averaging was applied. For each tested resistance value, 1000 consecutive measurements were taken.

A snapshot from oscilloscope with an input resistance R_S equal to 1 kΩ and its corresponding frequency ($1/T_{out}$) are shown in Figure 9. Both simulation and experimental data, as well as the linear Equation (5), using the weighted least square regression, are shown in Figure 10. The circuit was tested with Vdd equal to 5 V. A linear correlation coefficient of 0.9953 was obtained with respect to Equation (5). Vertical error bars show $\pm 2\sigma$.

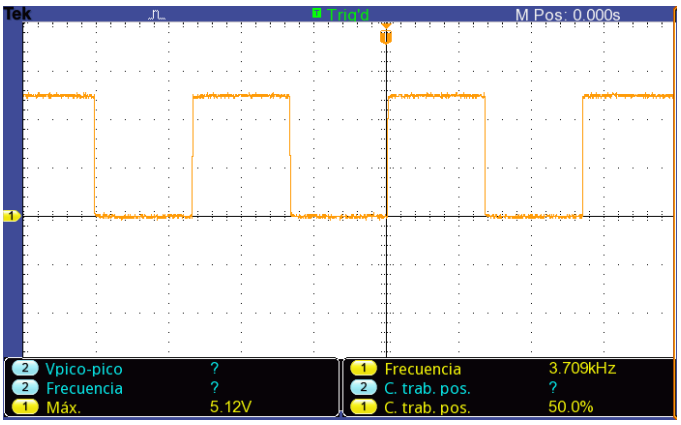

Figure 9. Oscilloscope snapshot for R_S equal to 1 kΩ.

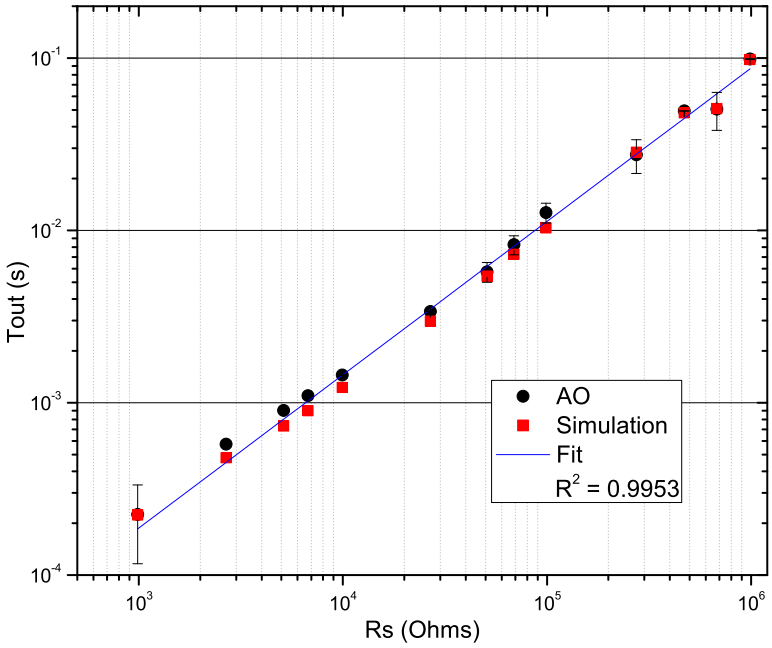

Figure 10. Period as function of the sample resistors. Simulation in solid red squares, experiment in solid black circles and linear Equation (5) in solid line.

F. Reverter et al. [29] presented an analysis of the effects of power supply interference on the output information in quasi-digital and modulating sensors, in which variations in power supply around 25, 50, and 100 mV and 0–5 times the central frequency were tested. In both cases, quasi-digital sensors have time-based outputs that are susceptible to power supply interferences. In this work, experimental measurements were carried out considering a variation of ±10% and of ±35% in the single supply voltage with a nominal value of 5 V, to demonstrate that dependence with the supply voltage (V_{DD}) was reduced when V_{bias} was matched with (V_H-V_L). In Figure 11, the experimental data from ±10% variation with a maximum error of ±2% is shown. The error was calculated using

the nominal value. In the same way, Figure 12 shows a maximum standard deviation of ±10% with respect to the mean, for a sweep from 3.5 to 7.5 V in the Vdd (more than 50% of V_{dd} variation).

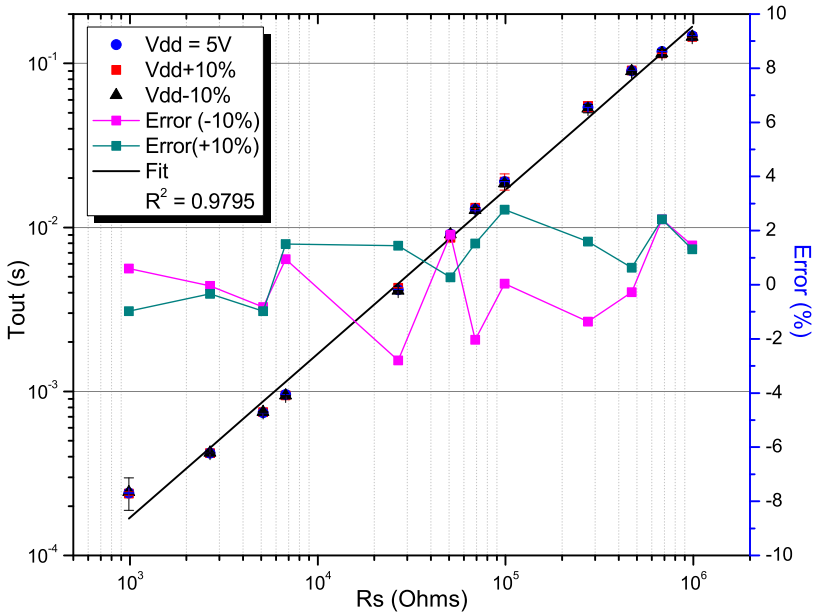

Figure 11. Period as function of the sample resistors. Experimental results with a power supply variation of ±10% from a nominal value of 5 V.

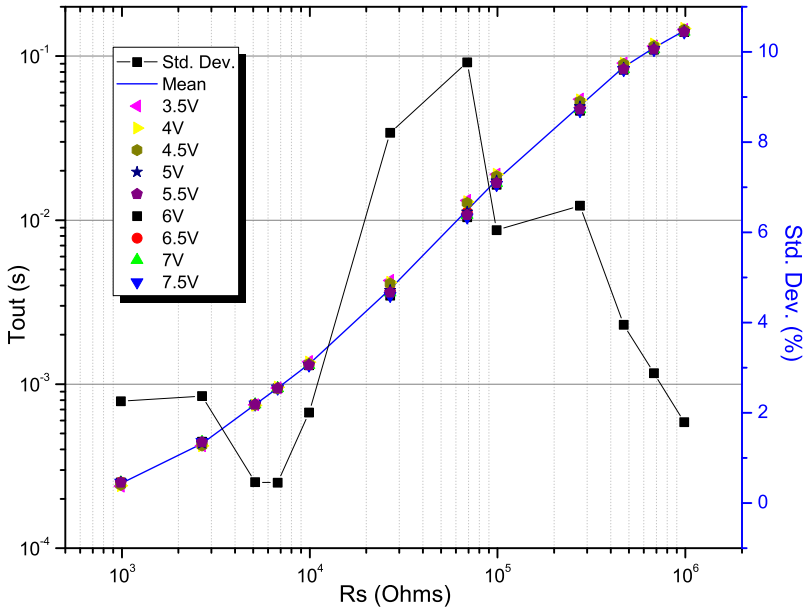

Figure 12. Period as function of the sample resistors. Experimental results with sweep from 3.5 to 7.5 V in the power supply.

To prove robustness to component variation, a second discrete component prototype was implemented. The complementary enhancement mode field effect transistors from the AO4614 family were replaced with the DMC4050 family and both NOT gates were implemented using a TTL7402. The operational amplifiers, resistors, and capacitor were kept with the same values. Figure 13 shows the experimental data from the comparison between the component replacement of the AO with the

DMC family. A correlation coefficient of 0.9956 was obtained. In the same way, another measurement was done where all operational amplifiers from the LM324 family were rotated, i.e., all the encapsulated opamps were changed by others of the same family. The rotation was done four times. Figure 14 shows four histograms and the mean value from the four measurements. Error from the histogram is less than $\pm 1.5\%$. Thus, it was found that changes on the components did not represent a significant change in the response of the proposed circuit.

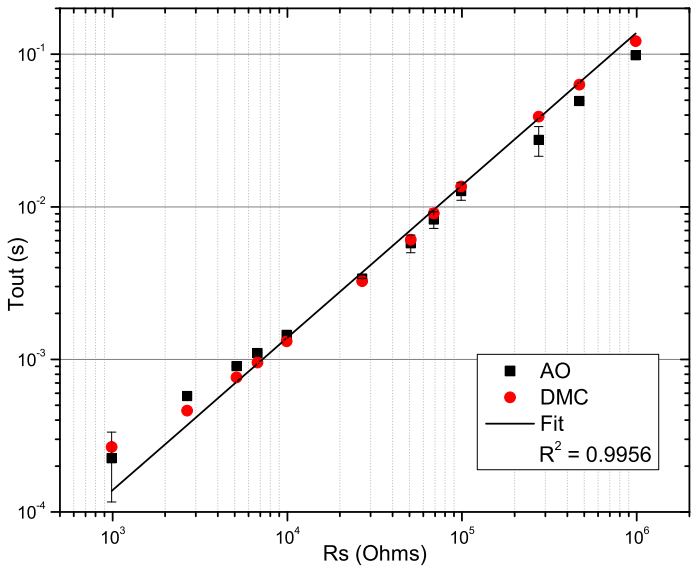

Figure 13. Experimental results from two discrete component prototypes: the first implemented with transistors from the AO4614 (AO, square) family and the second from the DMC4050 family (DMC, circle). Correlation coefficient equal to 0.9956.

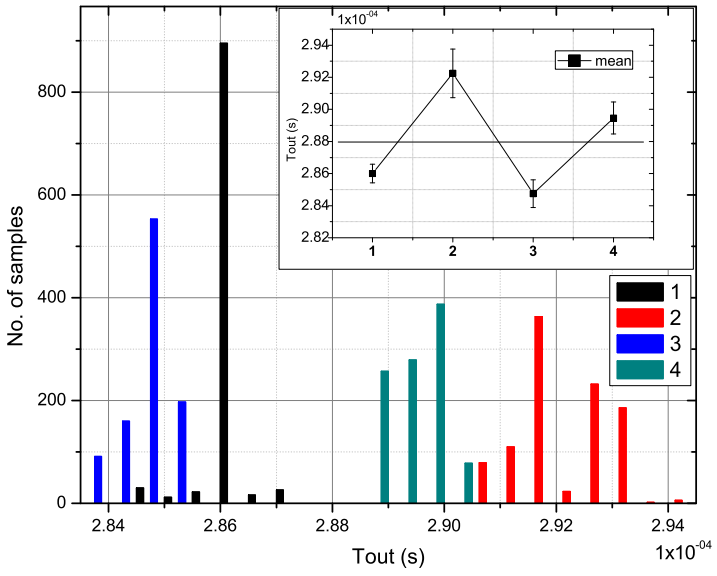

Figure 14. Histogram from the opamp variations with four different encapsulated. R_S = 2.7 KΩ.

Finally, Figure 15 shows the response of the proposed circuit for different values of capacitance C. It should be mentioned, that according to Equation (5), the smaller is the capacitance, the greater will be the error due to delay t_d.

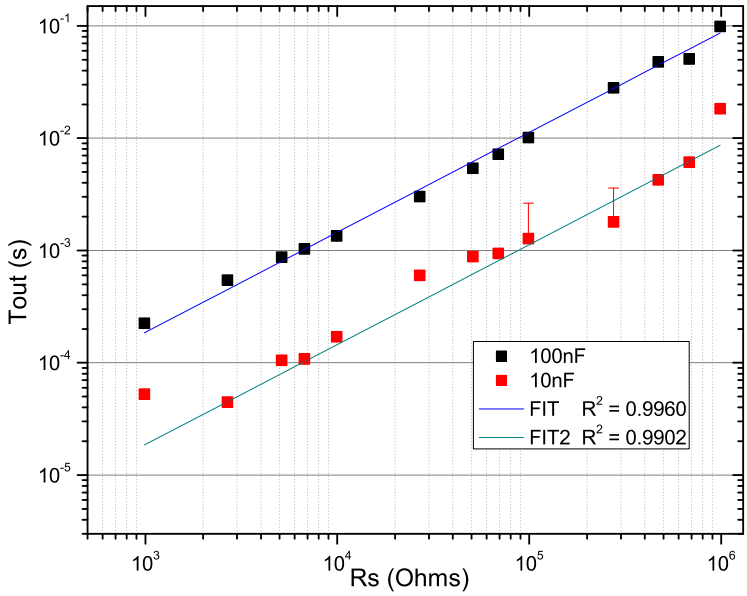

Figure 15. Measurement for different values of capacitance C.

5. Conclusions

A robust converter for obtaining a quasi-digital output directly from a resistive sensor is presented in this work. The proposed solution is based on the ratiometric approach, so the output becomes independent of any reference voltage. The square-wave output signal provides an easy way to process the sensor resistance allowing a simple data acquisition through low-cost digital processing systems.

Several works on the conditioning of resistive sensors have been reported in the literature, however, none has contemplated or shown the robustness to variations of the power supply and change of components according to the authors' knowledge. In this work, an architecture is shown that focuses on this robustness maintaining a wide dynamic range and precision.

Analysis of the proposed architecture for possible sources of errors indicates that most of the non-idealities introduce a gain error in β (in the current mirrors) and a delay t_d (by the comparator and switches), which can easily be canceled after calibration step.

Through several experimental measurements using two fabricated discrete components prototype, commercial Op-Amps and resistors emulating sensors, the results presented here establish the efficacy of the architecture proposed.

Based on the presented results, regarding its robustness and linearity with different variations, the proposed circuit is a suitable solution for portable sensor interfacing applications that have not been fully explored.

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Conflicts of Interest: The authors declare no conflict of interest.

Abbreviations

The following abbreviations are used in this manuscript:

LDR	Light Dependent Resistor
RTD	Resistance Temperature Detector
DAQ	Data Acquisition
R-I	Resistance-to-Current
CCO	Current Controlled Oscillator

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