A Nonisolated Three-Port DC–DC Converter with Continuous Input and Output Currents Based on Cuk Topology for PV/Fuel Cell Applications

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Abstract: A nonisolated three-port DC–DC converter based on Cuk topology (NI-TPC) to handle the renewable sources (RS) is proposed in this paper. This converter includes two unidirectional input ports accommodating both a fuel cell (FC) and photovoltaic (PV) cell; and one output port with DC load. Due to the inductors at all the ports, it claims the advantage of continuous input and output currents. Additionally, it uses less number of switches, diodes and inductors compared with conventional 'n-1' separate Cuk converters. Synthesis procedure for a generalized n-port DC–DC structure is explained. The derivation law based on conventional Cuk converter, operating principle, design calculation, and analysis are presented in detail, and then the analysis is validated through simulation and a 100W prototype, verifying the performance of the proposed NI-TPC converter.

Keywords: DC–DC; Nonisolated; Three-port; Cuk; PV/Fuel cell; Continuous current

1. Introduction

Fast and society-threatening global warming and health hazards due to the combustion of fossil fuels have triggered the research and development of more efficient and cleaner renewable sources (RS) namely solar, wind, fuel cell etc. Many DC–DC converters with a single inductor, for example, buck and boost converters and two inductor converters, such as Sepic, Cuk, and zeta converters, have been used to connect RS and load [1,2]. However, the stochastic and time-varying characteristics of these sources and unpredictable demand at load side necessitate the backup source for continuous power flow to the load. This condition forces the system to have at least two input ports; one for RS and another for a backup source such as fuel cell/wind/battery.

In the recent past, new converter topologies called multiport converters (MPC) have been proposed to integrate these RS, which ensure the continuous power flow to the load. The structure of conventional and MPC system is shown in Figure 1. The MPCs enhance the utilization of power sources based on their V–I characteristics, availability and cost [3]. Multiport converters (MPC) which claim the advantage of component sharing are acknowledged as one of the promising topologies to integrate the RS to cater the future energy generation requirements. Moreover, compact structure and lesser conversion stages are the reasons to adopt MPC for numerous applications such as hybrid power system [4], renewable energy integration [5], hybrid vehicles [6], aerospace applications, and uninterrupted power supplies. This MPC, in particular, the three-port converter (TPC) can be divided into three groups: (1) the isolated DC–DC converter; (2) semi-isolated DC–DC converter; and (3) nonisolated converter topologies. The isolated TPC uses a transformer with a high-frequency

to provide magnetic coupling and electrical isolation between the source and load [6–8]; partially isolated converters use a common DC bus along with magnetic coupling [9]. A nonisolated TPC uses common DC bus and finds applications where the isolation is not needed between the ports [10–12].

(a)　　　　　　　　　　　　　　　　　　　　　　**(b)**
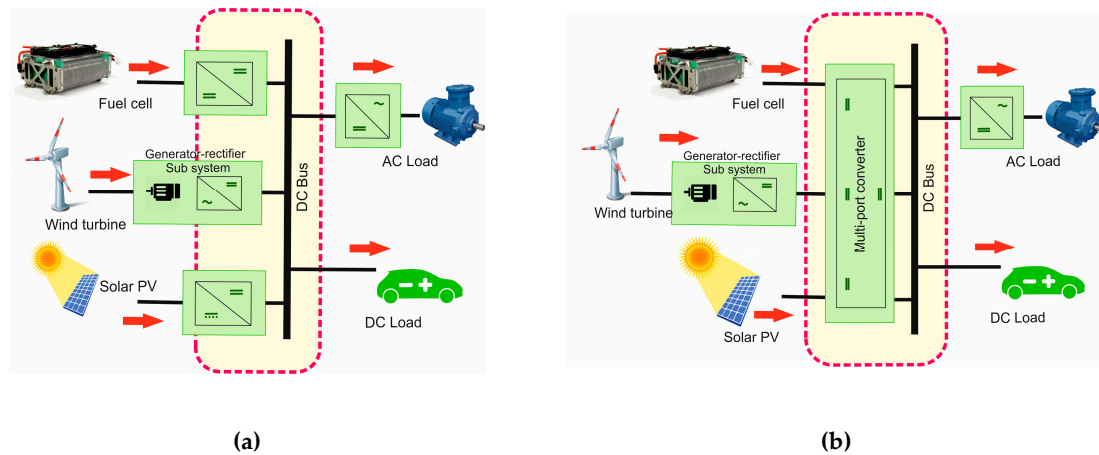
Figure 1. (**a**) Structure of the conventional system, (**b**) Proposed multiport converter (MPC) system.

TPCs can be configured in two topologies based on the nature of the input sources: series and parallel. In the series topology, the output voltage regulation becomes challenging if one of the input sources reduces (e.g., in PV shading condition) [13]. Assumptions and conditions to design the converters with multiple input–single output (MISO) from the conventional single input–single output (SISO) structures are explained [14]. The systematic way of synthesizing MISO converters is detailed in Reference [15]. Topology generation methods and principles for developing a family of NI-TPC are proposed [16]. These TPCs are developed by introducing a SISO model in an existing dual input or two output converters. In Reference [17], an approach to systematically derive MPCs with DC link inductor concept and with two input and two output converters is proposed. This procedure has developed numerous TPC topologies. A novel nonisolated TPC with single inductor is proposed for RS [18]. This converter features the integration and control of bidirectional load, compactness, single stage power conversion between any two ports, and seven possible operational modes. The design of a NI-TPC using one switch for a standalone PV power system integrating energy storage is proposed in Reference [19]. A synchronous switch with a pair of diodes has been utilized instead of two individual switches. However, the converters in both the stages must operate synchronously. The inherent buck–boost characteristics of the Cuk converter provide flexibility for standalone and grid-tied applications when the output voltage required is more or less than the input voltage. Continuous current at the input and output ports and the identical switching voltage waveforms appearing across the inductors are the salient features of the Cuk converter [20]. New topologies with high voltage ratio have been proposed using Cuk converter in Reference [21] for renewable power applications. In Reference [9], A TPC is presented by integrating a Cuk converter with bidirectional power flow and a full-bridge (FB) rectifier circuit for renewable energy applications. It used a transformer with high frequency. This converter consists of two nonisolated and one isolated ports. A nonisolated DC–DC TPC using integrated boost-cuk topology with high voltage gain is proposed [22]. An isolated TPC depending on Cuk converter is presented in Reference [23] by incorporating the inductor and transformers on a single core. Three winding transformer used in the above converter increases the size. Moreover, it uses more number of switches. The three-port Cuk converter to solve the zero-ripple problem is presented by designing a single integrated magnetic core having all the magnetics on it [24]. Methods based on circuit theory and the structure of the core are used to analyze the ripples. However, these converters are the isolated type and use bulky transformers and inductors. In Reference [25], a DC–DC converter combining a SEPIC and Cuk converter is proposed for bipolar DC microgrid

applications. A single switch shared by both converters is an added advantage. However, the number of power components is greater.

However, the TPCs mentioned above fail to provide a high voltage conversion ratio and continuous current at all the ports.

The outstanding features of the proposed converter are

- Both the input ports share common output inductor, hence minimizing the component count.
- Continuous current with less ripple in all the ports (the input and output ports).
- Delivered power from each input can be independently controlled
- Buck–boost output voltages can be obtained.

To the best of the author's knowledge, the design and development of NI-TPC converter has not been reported earlier in literature. In this paper, the design, development, and extensive analysis of the proposed converter have been carried out to validate the performance of the converter.

Generally, the energy flow control modes and circuit analysis procedure are common sense and well discussed in many other papers [4,26–31]. However, the DC–DC structure of the Cuk-Cuk converter used for the system that integrates the input ports (1 and 2) to DC Bus (Port 3) is new, which increases the novelty of the paper.

2. Proposed Converter Structure

2.1. Synthesis of the NI-TPC Converter

This section presents the illustration of synthesizing the proposed NI-TPC converter from a classical Cuk converter. Based on the fundamentals, the structure of the classical Cuk converter can be deduced to the input section, output section, and an energy buffer section that connects both, as shown in Figure 2. The capacitor acts as a voltage buffer and transfers energy from input to output section without consuming any energy. The input with voltage buffer and output sections are separated and connected as represented in Figure 2 to form the generalized n-port structure.
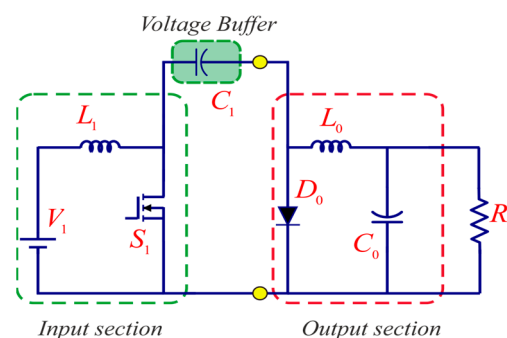

Figure 2. Structure of classical Cuk converter.

The resulting structure of the proposed 'n' port converter consists of 'n-1' input sources, 'n' inductors, 'n' capacitors, 'n-1' switches and a single diode is presented in Figure 3. Table 1 gives a comparison of the circuit elements used in the proposed and conventional structures.

A three-port converter with two input ports and a load port is taken for better understanding as shown in Figure 4. One can understand that it is based on the integration of two classical Cuk converters. The proposed TPC consists of three inductors (L_1, L_2, and L_0), three capacitors (C_1, C_2, and C_0), two switches (S_1–S_2), and one diode (D_0). Power sources V_1 and V_2 are connected to the unidirectional input ports.
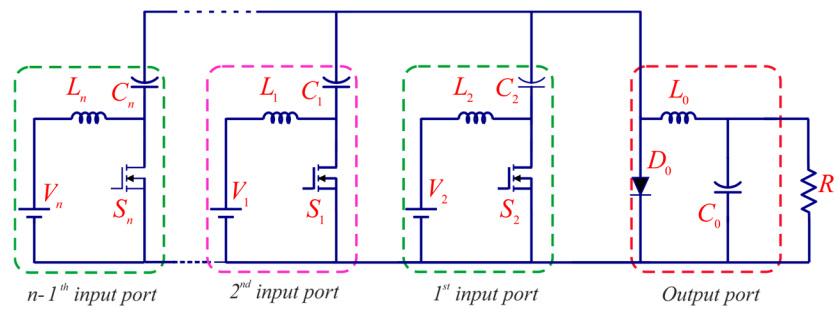
Figure 3. Generalized structure of the proposed 'n' port converter.

Table 1. Comparison of circuit elements.

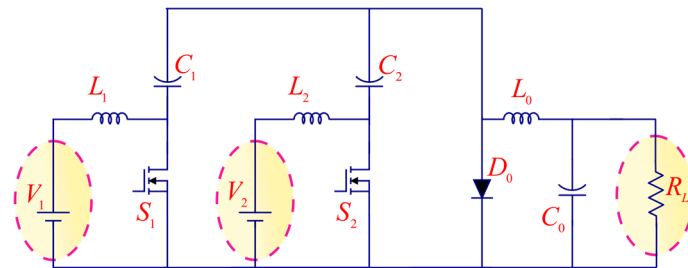| Circuit Elements	Proposed n-Port Cuk-Cuk Converter	(n-1) Individual Cuk Converters
Inductors	n	2(n-1)
Capacitors	n	2(n-1)
Switch	n-1	n
Diode	1	2(n-1)

Figure 4. Proposed three-port converter.

2.2. Operating Principles

Based on the availability of power sources, the proposed TPC can function in two different modes: the SISO and dual input single output (DISO) modes. Either of the input ports can cater to load in the absence of the other in SISO mode. In DISO mode, both sources contribute power to load when the primary power source is insufficient to meet the load demand. The proposed NI-TPC converter can function in all these modes through appropriate control.

2.2.1. SISO Mode

Figure 5a shows the Equivalent circuit when operating in SISO mode. The equivalent circuits of state 1 and state 2 are shown in Figure 5b,c, respectively. The waveforms are not shown since it is similar to the classical Cuk converter.

State 1

In this mode, switch S_1 is ON, but the diode is not conducting. Voltage source V_1 magnetizes the inductor L_1. The positive voltage on the inductor makes the inductor current i_{L1} to increase linearly. The capacitor C_1 is assumed precharged and discharging its energy to the load through the inductor L_0. Hence, the inductor current i_{L2} increases linearly. In addition, it charges the output capacitor C_0. Various currents and voltages can be expressed by (1).

$$\left.\begin{array}{l} V_{L1} = V_1, \\ V_{L0} = V_{C1} - V_{C0} \\ i_{C1} = i_{L0} \\ i_{C0} = i_{L0} - i_0 \end{array}\right\} \tag{1}$$

State 2

In this state, switch S_1 is OFF while the diode conducts and freewheels. The voltage source V_1 together with the energy stored in the inductor L_1, charge the capacitor C_1 through diode D_0. The current in the inductor i_{L1} decreases linearly. The output inductor L_0 is demagnetized and its energy flows to the load through diode D_0. Equation (2) is valid in this mode:

$$\left.\begin{array}{l} V_{L1} = V_1 - V_{C1}, \\ V_{L0} = -V_{C0} \\ i_{C1} = i_{L1} \\ i_{C0} = i_{L0} - i_0 \end{array}\right\} \tag{2}$$

$$\left.\begin{array}{l} \frac{V_0}{V_1} = -\frac{D_1}{1-D_1} \\ I_{L1} = \frac{P_1}{V_1}, I_{L0} = \frac{P_0}{V_0} \\ R_L = \frac{V_0^2}{P_0} \end{array}\right\} \tag{3}$$
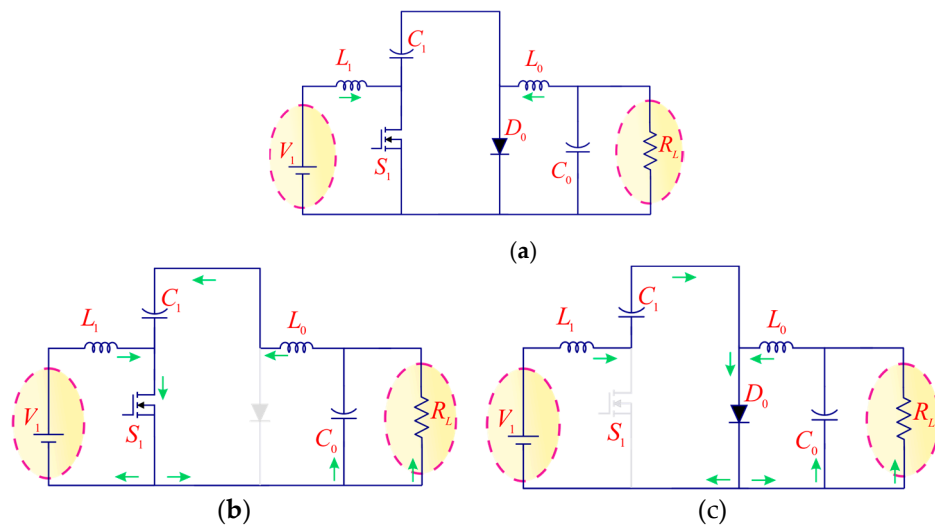
Figure 5. (**a**) Single input–single output (SISO) mode of the proposed converter: (**b**) State 1 and (**c**) State 2.

2.2.2. DISO Mode

Better utilization of power sources needs a suitable control technique to achieve the regulated output power. The appropriate switching pattern in various modes depends on the time multiplexing of switching signals.

Selection of switching sequence can be done in many ways based on whether power is catered individually or simultaneously. A left-aligned switching pattern as shown in Figure 6 has been chosen in this work for analysis of the proposed converter.
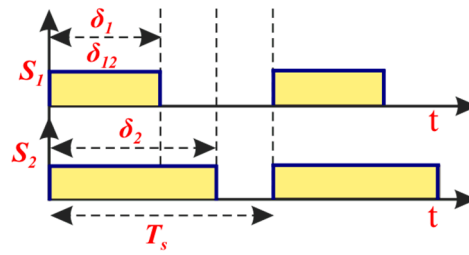
Figure 6. Left-aligned switching pattern.

State 1

During this state, both switches S_1 and S_2 are ON, but the diode remains nonconducting. The voltage sources V_1 and V_2 magnetize the inductors L_1 and L_2 respectively. The positive voltage on the inductors makes the inductor currents increase linearly. Capacitors C_1 and C_2 are assumed precharged and to be discharging energy. The load is catered by the capacitors discharge through the inductor L_0. The corresponding equivalent circuit is illustrated in Figure 7a. The corresponding equations have been presented in (4).

$$\left.\begin{array}{l} V_{L1} = V_1, V_{L2} = V_2 \\ V_{L0} = V_0 - V_{C1} \\ i_{C1} + i_{C2} = i_{L0} \\ i_{C0} = i_{L0} - i_0 \end{array}\right\} \tag{4}$$
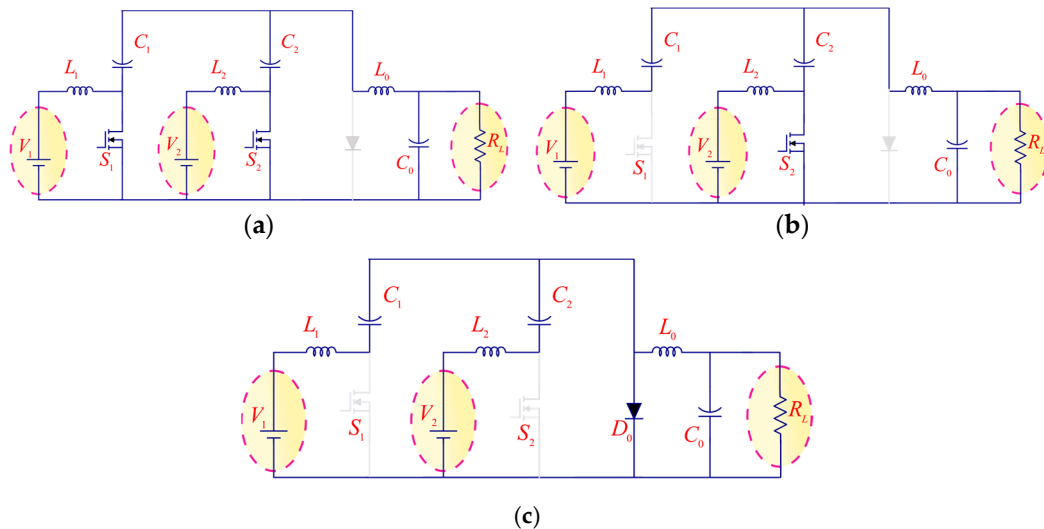

Figure 7. Equivalent circuits: (**a**) State 1, (**b**) State 2, and (**c**) State 3.

State 2

In this interval, switch S_1 is OFF and switch S_2 is ON, but the diode stays nonconducting due to the voltage across capacitor C_2. The voltage source V_1 together with the energy stored in the inductor L_1, charges the capacitor C_1. V_2 continues to discharge and magnetize the inductor L_2. Due to the positive and constant voltage on inductor L_2, its current raises linearly. The capacitor C_2 continues to discharge as in Mode 1, and the load is catered by it through the inductor L_0. The corresponding equivalent circuit is presented in Figure 7b. Equation (5) is derived for this mode.

$$\left.\begin{array}{l} V_{L1} = V_1 - V_{C1} + V_{C2} \\ V_{L2} = V_2, V_{L0} = V_0 - V_{C2} \\ i_{C1} = i_{L1}, i_{C2} = i_{L0} - i_{C1} \\ i_{C0} = i_{L0} - i_0 \end{array}\right\} \tag{5}$$

State 3

In this state, both switches S_1 and S_2 are OFF while the diode conducts and freewheels. The voltage sources V_1 and V_2 together with the energy stored in the inductors L_1 and L_2, charge capacitors C_1 and C_2 respectively. The current in the inductors i_{L1} and i_{L2} decreases linearly. The output inductor L_0 discharges and the load is catered by it through the Diode D_0. The equivalent circuit of this state is illustrated in Figure 7c. Various currents and voltages can be expressed as in (6).

$$\left.\begin{array}{l} V_{L1} = V_1 - V_{C1} \\ V_{L2} = V_2 - V_{C2}, V_{L0} = V_0 \\ i_{C1} = i_{L1}, i_{C2} = i_{L2} \\ i_{C0} = i_{L0} - i_0 \end{array}\right\} \tag{6}$$

Ideal operating conditions with Steady state and continuous conduction mode (CCM) is assumed to derive the expressions of the output voltage and voltage gain.

3. Modeling and Analysis of the Converter

The derivation of various parameters and modeling of the proposed NI-TPC converter are presented in this section.

3.1. Voltage Gain

The analytical expression for the output voltage has been obtained by applying volt second balance theory on inductors.

$$V_1 = V_{c1}(1 - \delta_1) - V_{c2}(\delta_2 - \delta_1) \tag{7}$$

$$V_{c2} = \frac{V_2}{(1 - \delta_2)} \tag{8}$$

$$V_0 = \delta_1 V_{c1} + \delta_2 V_{c2} \tag{9}$$

The expression of the output voltage can be derived from Equations (7)–(9). The voltage equation in terms of duty cycles is

$$V_0 = \frac{\delta_1}{(1 - \delta_1)} V_1 + \frac{\delta_2(\delta_2 - \delta_1)}{(1 - \delta_1)(1 - \delta_2)} V_2 = G_{V1} \cdot V_1 + G_{V2} \cdot V_2 \tag{10}$$

From (10), one can understand that the proposed converter operating in DISO mode has the same voltage gain compared with classical Cuk converter, which is plotted in Figure 8. Considering $V_1 = V_2 = V$, the output voltage of the proposed converter is presented in (11). Selecting the same duty ratio for both the switches leads to the output voltage equal to the one in classical Cuk converter as derived in (12). The voltage gain for an n-port DC–DC Cuk-Cuk converter with the proposed topology can be derived as in (13).

$$V_0 = \frac{\delta_1}{(1 - \delta_1)} V_1 + \frac{\delta_2(\delta_2 - \delta_1)}{(1 - \delta_1)(1 - \delta_2)} V_2 = G_{V1} \cdot V_1 + G_{V2} \cdot V_2 \tag{11}$$

Taking $\delta_1 = \delta_2 = \delta$

$$V_0 = \frac{\delta}{1 - \delta} V \tag{12}$$

For an n-port converter,

$$V_0 = \left[\frac{\delta_1}{1 - \delta_1} + \sum_{i=2}^{n} \frac{\delta_i(\delta_i - \delta_1)}{(1 - \delta_1)(1 - \delta_i)} \right] V_i \tag{13}$$
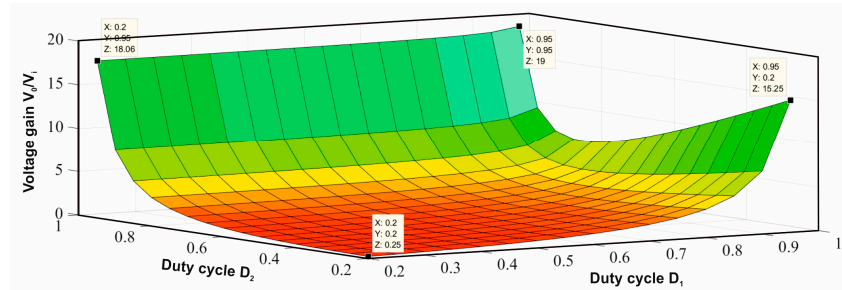

Figure 8. Voltage gain Vs Duty cycle of NI-TPC converter.

Applying the charge-sec balance principle on capacitors, the following equations are obtained.

$$\langle I_{C1} \rangle = C_1 \frac{dV_1}{dt} = \frac{i_{L0}}{dt} \delta_1 + i_{L1} \delta_e + i_{L1} \delta_{off}$$

$$i_{L1} = \frac{\delta_1}{2(\delta_1 - 1)} i_{L0} \tag{14}$$

$$\langle I_{C2} \rangle = C_2 \frac{dV_2}{dt} = \frac{i_{L0}}{2} \delta_1 + (i_{L0} - i_{L1}) \delta_e + i_{L2} \delta_{off}$$

$$i_{L2} = \left(\frac{\delta_1 \delta_2}{2(\delta_1 - 1)} - \frac{\delta_1^2}{2(\delta_1 - 1)} - \delta_2 + \frac{\delta_1}{2} \right) \frac{i_{L0}}{(1 - \delta_2)} \tag{15}$$

3.2. Current Ripples of Inductors

Current ripples and inductor volt-second balance (IVSB) principle are used to design inductors. The inductor current ripple equations are modified to obtain equations for inductor values (16)–(18).

$$\left. \begin{aligned} \Delta i_{L1} &= \frac{V_1 \delta_1 T_S}{2L_1} = \frac{V_1 \delta_1}{2L_1 f_S} \\ L_1 &= \frac{V_1 \delta_1}{2 \Delta i_{L1} f_S} \end{aligned} \right\} \tag{16}$$

$$\left. \begin{aligned} \Delta i_{L2} &= \frac{V_2 \delta_2 T_S}{2L_2} \\ L_2 &= \frac{V_2 \delta_2}{2 \Delta i_{L2} f_S} \end{aligned} \right\} \tag{17}$$

$$\left. \begin{aligned} \Delta i_{L0} &= \frac{\delta_1(1-\delta_2)}{(1-\delta_1)} \frac{V_1 T_S}{L_0} + \frac{\delta_2(\delta_2-\delta_1)}{(1-\delta_1)} \frac{V_2 T_S}{L_0} \\ L_0 &= \frac{\delta_1(1-\delta_2)}{(1-\delta_1)} \frac{V_1}{\Delta i_{L0} f_S} + \frac{\delta_2(\delta_2-\delta_1)}{(1-\delta_1)} \frac{V_2}{\Delta i_{L0} f_S} \end{aligned} \right\} \tag{18}$$

The values of the inductors can be found, if output voltage, source voltages, desired ripples, switching frequency and duty cycle are known.

3.3. Voltage Ripples of Capacitors

Voltage ripples and the capacitor charge-second balance (CCSB) principle are used to design capacitors. The voltage ripple equations are modified to obtain equations for capacitor values (19)–(21).

$$\left. \begin{aligned} \Delta V_1 &= \frac{(1-\delta_1)T_S}{C_1} \frac{2(\delta_1-1)}{\delta_1 R} V_0 \\ C_1 &= \frac{(1-\delta_1)}{\Delta V_1 f_S} \frac{2(\delta_1-1)}{\delta_1 R} V_0 \end{aligned} \right\} \tag{19}$$

$$\Delta V_2 = \frac{(1-\delta_2)T_S}{RC_2(1-\delta_1)}\left(\frac{\delta_1\delta_2}{2(\delta_1-1)} - \frac{\delta_1^2}{2(\delta_1-1)} - \delta_2 + \frac{\delta_1}{2}\right)V_0$$
$$C_2 = \frac{(1-\delta_2)}{R\Delta V_2 f_S(1-\delta_1)}\left(\frac{\delta_1\delta_2}{2(\delta_1-1)} - \frac{\delta_1^2}{2(\delta_1-1)} - \delta_2 + \frac{\delta_1}{2}\right)V_0$$

(20)

Output capacitor can be determined from the output voltage ripple.

$$\Delta V_0 = \frac{\Delta i_{L0} T_S}{8C_0}$$
$$C_0 = \frac{\Delta i_{L0}}{8\Delta V_0 f_S}$$

(21)

The values of the capacitors can be found if the output voltage, source voltages, desired ripples, switching frequency and duty cycle are known. A 5% current ripples in inductors, 5% voltage ripples in buffer capacitor C_1 and 4% voltage ripples in output capacitor C_0 have been considered to design the parameters listed in Table 2. The converter is simulated and various current and voltage waveforms are presented in Figure 9a–j.

Table 2. Components of the proposed converter.

Sl.No	Component	Symbol	Simulation	Hardware
1	Inductors	L_1 and L_2	0.8 & 1.51 mH	1 & 1.5 mH
2	Capacitors	C_1 and C_2	46.3 μF & 63 μF	50 μF, 63 V & 72 μF, 50 V
3	Output Inductor	L_0	2 mH	2 mH
4	Output Capacitor	C_0	1.7 μF	2.2 μF, 35 V
5	Load Resistance	R	5.76 Ω	6 Ω
6	Switching Frequency	f_{sw}	20 kHz	20 kHz
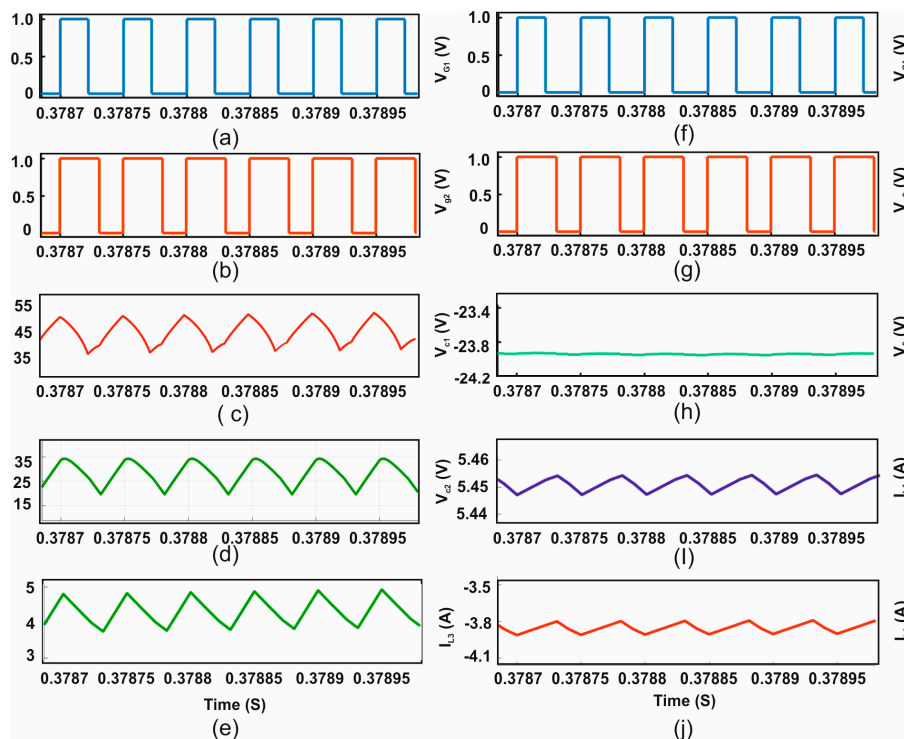
Figure 9. Waveforms of various voltages and currents during mode 2 (**a,f**) Gate signal to S_1, (**b,g**) Gate signal to S_2, (**c**) Voltage across capacitor C_1, (**d**) Voltage across capacitor C_2, (**e**) Current through the inductor i_3, (**h**) Output voltage (**i**) Current through the inductor L_1, (**j**) Current through the inductor L_2.

3.4. Small-Signal Modeling

Voltage regulation should be maintained in spite of the changes in input and output parameters in any power converter, which necessitates a design of feedback controller. Modeling plays a good role in providing information about the dynamic behavior of the converter and in deriving a feedback control system. Numerous modeling methods have been proposed for power electronic converters. The State-Space Averaging (SSA) method is the most commonly used method to design control loops and to investigate the transient and steady state response of the converter. This modeling method has three steps: (1) writing the state-space equations for all states in a switching cycle; (2) derivation of average state-space equation; and (3) applying perturbations to the averaged equation to derive the linear first order small-signal equations, from which different transfer functions relating the inputs and outputs can be obtained. Then, matrices A and B are formed, which describe the converter model. The derived model fits in the following form (22).

$$\left.\begin{array}{l} \dot{X} = AX + BU \\ Y = CX + DU \end{array}\right\} \tag{22}$$

where X, U, Y and $\dot{x} = dx/dt$ represent the state vector, the input or control vector, the output vector and the derivative of X respectively. Matrices A, B, C and D are the system, control, output and feed-forward matrices respectively. A and B are used to extract various transfer functions of the system.

$$X = \left[\begin{array}{cccccc} i_{L1} & i_{L2} & i_{L3} & v_{C1} & v_{C2} & v_0 \end{array}\right]^T \tag{23}$$

$$U = \left[\begin{array}{cc} V_1 & V_2 \end{array}\right]^T \tag{24}$$

$$Y = [V_0] \tag{25}$$

From the Equation (4) in Section 2 and according to circuit theory, the dynamic equations representing state-1 can be written as follows

$$\left.\begin{array}{l} L_1 \frac{di_{L1}}{dt} = V_1, L_2 \frac{di_{L2}}{dt} = V_2 \\ L_0 \frac{di_{L0}}{dt} = V_0 - V_{C1} \\ C_1 \frac{dv_{C1}}{dt} + C_2 \frac{dv_{C2}}{dt} = i_{L0} \\ C_0 \frac{dv_0}{dt} = i_{L0} - i_0 \end{array}\right\} \tag{26}$$

The derived dynamic equations representing state-2 and state-3 are given in (27) and (28) respectively.

$$\left.\begin{array}{l} L_1 \frac{di_{L1}}{dt} = V_1 - V_{C1} + V_{C2} \\ L_2 \frac{di_{L2}}{dt} = V_2, L_0 \frac{di_{L0}}{dt} = V_0 - V_{C2} \\ C_1 \frac{dv_{C1}}{dt} = i_{L1}, C_2 \frac{dv_{C2}}{dt} = i_{L0} - i_{C1} \\ C_0 \frac{dv_0}{dt} = i_{L0} - i_0 \end{array}\right\} \tag{27}$$

$$\left.\begin{array}{l} L_1 \frac{di_{L1}}{dt} = V_1 - V_{C1} \\ L_2 \frac{di_{L2}}{dt} = V_2 - V_{C2}, L_0 \frac{di_{L0}}{dt} = V_0 \\ C_1 \frac{dv_{C1}}{dt} = i_{L1}, C_2 \frac{dv_{C2}}{dt} = i_{L2} \\ C_0 \frac{dv_0}{dt} = i_{L0} - i_0 \end{array}\right\} \tag{28}$$

The obtained state space model in matrix form is given in (29).

$$\begin{bmatrix} \frac{di_{L1}}{dt} \\ \frac{di_{L2}}{dt} \\ \frac{di_{L3}}{dt} \\ \frac{dv_{C1}}{dt} \\ \frac{dv_{C2}}{dt} \\ \frac{dv_0}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & \frac{\delta_1-1}{L_1} & \frac{(\delta_2-\delta_1)}{L_1} & 0 \\ 0 & 0 & 0 & 0 & \frac{-(1-\delta_2)}{L2} & 0 \\ 0 & 0 & 0 & \frac{-\delta_1}{L_0} & \frac{-(\delta_2-\delta_1)}{L_0} & \frac{-1}{L_0} \\ \frac{1-\delta_1}{C_1} & 0 & \frac{-\delta_1}{2C_1} & 0 & 0 & 0 \\ \frac{-(\delta_2-\delta_1)}{C_2} & \frac{1-\delta_2}{C_2} & \frac{\delta_2-\delta_1}{C_2}-\frac{\delta_1}{2C_2} & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{C_0} & 0 & 0 & \frac{-1}{RC_0} \end{bmatrix} \begin{bmatrix} i_{L1} \\ i_{L2} \\ i_{L0} \\ v_{C1} \\ v_{C2} \\ v_0 \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} & 0 \\ 0 & \frac{1}{L_2} \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix}$$

$$\begin{bmatrix} V_0 \\ I_0 \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & 0 & 0 & \frac{1}{R} \end{bmatrix} \begin{bmatrix} i_{L1} \\ i_{L2} \\ i_{L0} \\ v_{C1} \\ V_{C2} \\ V_0 \end{bmatrix} + \begin{bmatrix} 0 & 0 \\ 0 & 0 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} \tag{29}$$

Using (29) with the obtained model, the transfer functions are derived and shown in (30)–(32).

$$T = C[SI - A]^{-1}B + D \tag{30}$$

$$\frac{V_0}{V_1} = \frac{-8.889 \times 10^{10}s^2 - 9.877 \times 10^{19}}{s^6 + 41.67s^5 + 9.406 \times 10^7s^4 + 3.919 \times 10^9s^3 + 2.092 \times 10^{15}s^2 + 8.711 \times 10^{16}s + 3.951 \times 10^{19}} \tag{31}$$

$$\frac{V_0}{V_2} = \frac{1.333 \times 10^{12}s^2 - 3.556 \times 10^{19}}{s^6 + 41.67s^5 + 9.406 \times 10^7s^4 + 3.919 \times 10^9s^3 + 2.092 \times 10^{15}s^2 + 8.711 \times 10^{16}s + 3.951 \times 10^{19}} \tag{32}$$

These transfer functions are evaluated using MATLAB commands to eliminate manual mistakes, and the step data analysis is obtained. Figure 10 illustrates the response of the plant to a unit step input.
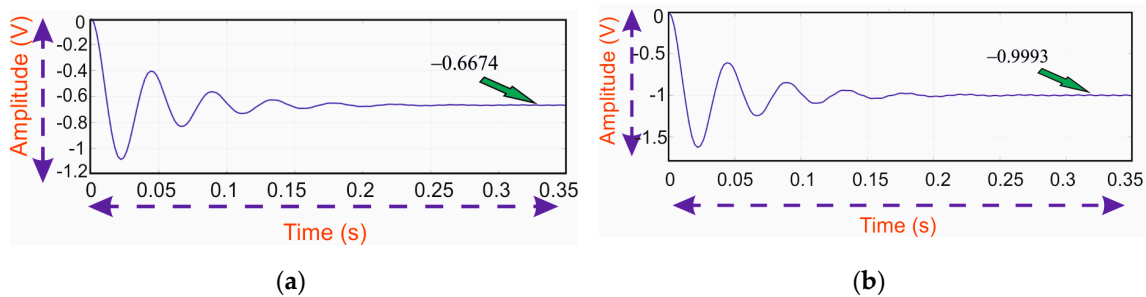

Figure 10. Step response of open loop system (**a**) with V_1 source and (**b**) with V_2 source.

Figure 10a,b depicts the step response of the converter with step change in input sources V_1 and V_2 respectively. It is clear that the response is inverted as the Cuk converter has an inverted output. The steady state value settles at -0.6674 in Figure 10a and has an error of 33.26% with a peak overshoot of 62.7284%. In Figure 10b, the response settles at -0.9993 and has an error of 0.7% with a peak overshoot of 62.64644%.

4. Design of Controller

The most popular proportional plus integral (PI) controller has been designed to eliminate the steady state error pointed in Figure 10. One can obtain the proportional and the integral output as given in (30).

$$P_{out} = K_p e(t), I_{out} = K_i \int_0^t e(t)dt \tag{33}$$

Ziegler–Nichols PI tuning was adopted to obtain the values of the proportional gain K_p and integral time T_i. The S-shaped waveform can be defined by two parameters, delay time L and time constant T as illustrated in Figure 11a.
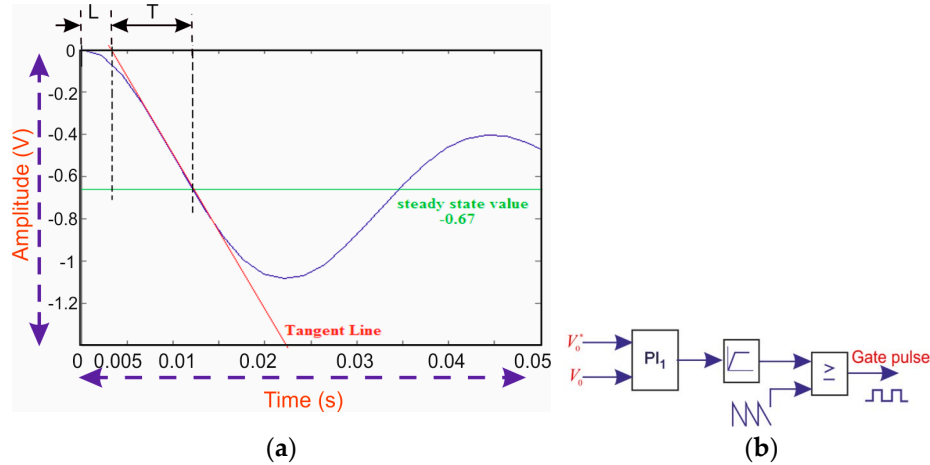

Figure 11. (**a**) S shaped curve. (**b**) Control with PI controller.

The designed PI controller has been incorporated with the plant as shown in Figure 11b. The parameters of the controller can be obtained as given in (34)

$$PI controller = K_p\left(1 + \frac{1}{T_i S}\right), K_P = 0.9\frac{T}{L}, T_i = \frac{L}{0.3}\Big\} \tag{34}$$

Figure 12a,b show the step response of the converter with PI controller for the step change in input sources V_1 and V_2 respectively. The steady state error is reduced and overshoots of 0.0013% and 0.0068% are achieved. To make both sources work effectively, with the magnitude of input voltage $V_1 > V_2$, the duty cycle is considered as $\delta_1 < \delta_2$.
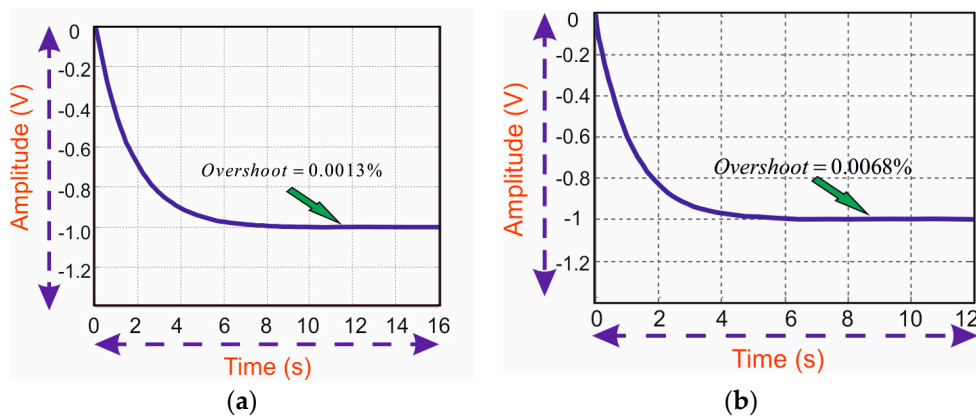

Figure 12. Step response of the system in closed loop (**a**) with V_1 source and (**b**) with V_2 source.

5. Results and Discussion

A 100 W, 20 kHz NI-TPC converter using MOSFET switches was fabricated in the laboratory (Figure 13.) with the designed values. The whole system consists of the developed converter, two DC power sources representing the renewable energy sources such as PV and fuel cell, a FPGA spartan6 controller board, and a resistive load. Triggering signals for the switches and the controller are realized using FPGA Spartan 6 controller board. The specifications of components used are listed in Table 2.
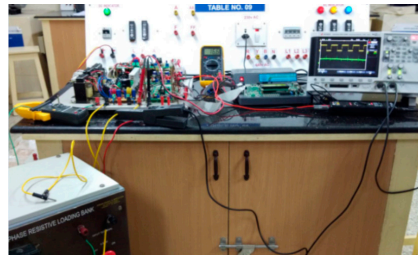
Figure 13. Hardware setup.

Experiments have been conducted using the proposed NI-TPC converter with an 18 V input voltage. Duty ratios of 60% and 40% were chosen for the boost and buck operations respectively. The results are shown in Figures 14 and 15. Also, the test has been performed with 12 V input voltage and observed that the performance is satisfying the theoretical analysis. However, these results are not provided in this paper.

Figure 14a shows the current through inductors L_1, L_2 and the load current I_0 along with gate signal applied under boost operation. It can be seen that the current ripples of inductors Δi_{L1}, Δi_{L2} and load current Δi_0 are in between (5.9 A, 5.3 A), (4.3 A, 3.4 A) and (4.2 A, 3.4 A) respectively. The average values and ripples are in close approximation with the 5.55 A, 3.71 A, and 3.6 A calculated from (2) and (3). The voltage across the capacitors C_1 and C_2 along with gate signal are shown in Figure 14b. From Figure 14b, the average voltages across the capacitors are 44 V and -26.2 V which are in agreement with the theoretical calculations from (1) and (2). The generated gate signal and source and output voltages are 15 V, 18 V, and -26.2 V, respectively, as shown in Figure 14c.
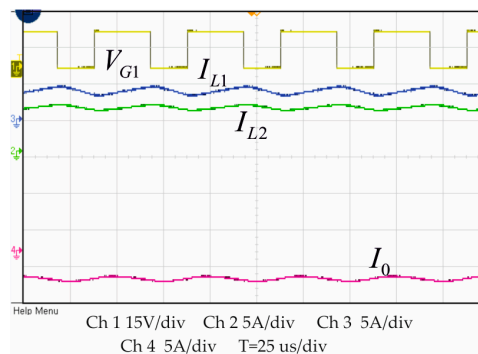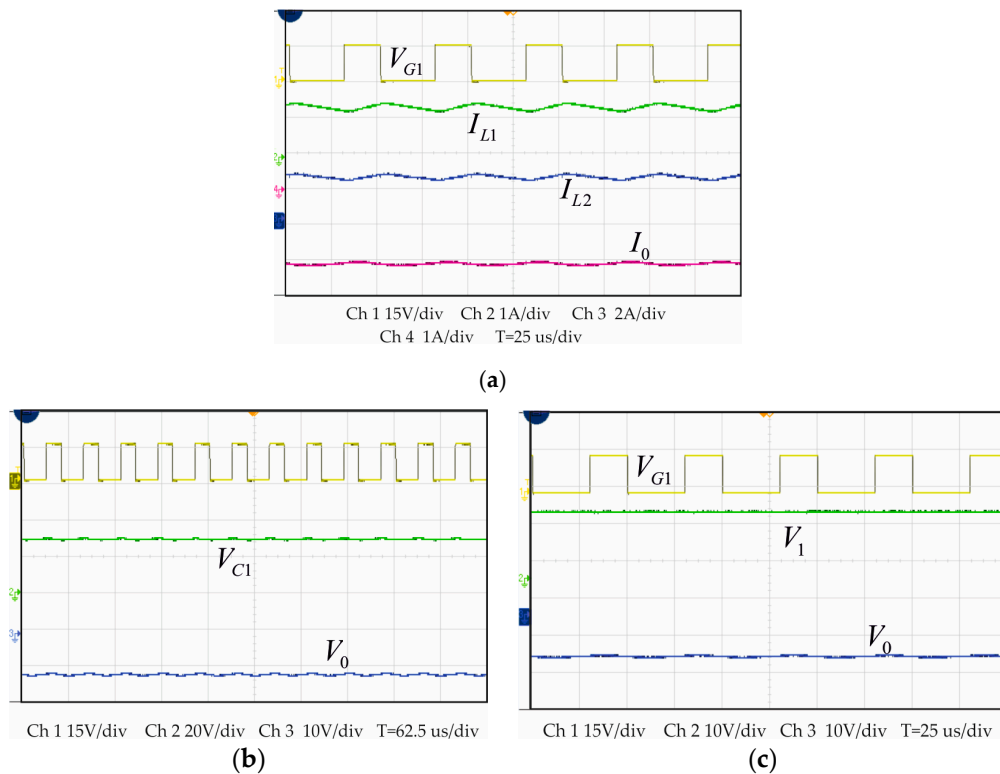

(**a**)
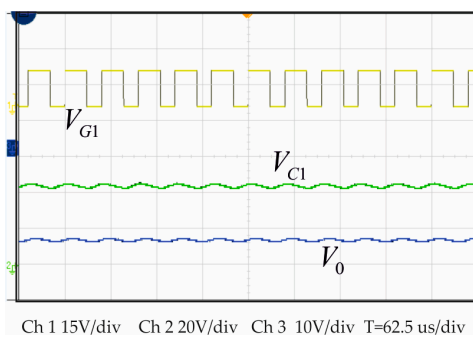
(**b**)
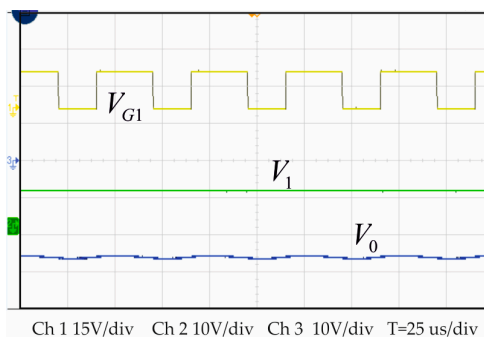
(**c**)

Figure 14. Various voltage and current measurements from experiments during Mode 1 with source 1 (Boost mode): (**a**) Gate signal, inductor currents through L_1, L_2 and Load current (CH 1–4); (**b**) Gate signal and capacitor voltages across C_1 and C_2 (CH 1–3); (**c**) Gate signal, source voltages and output voltage (CH 1–3).
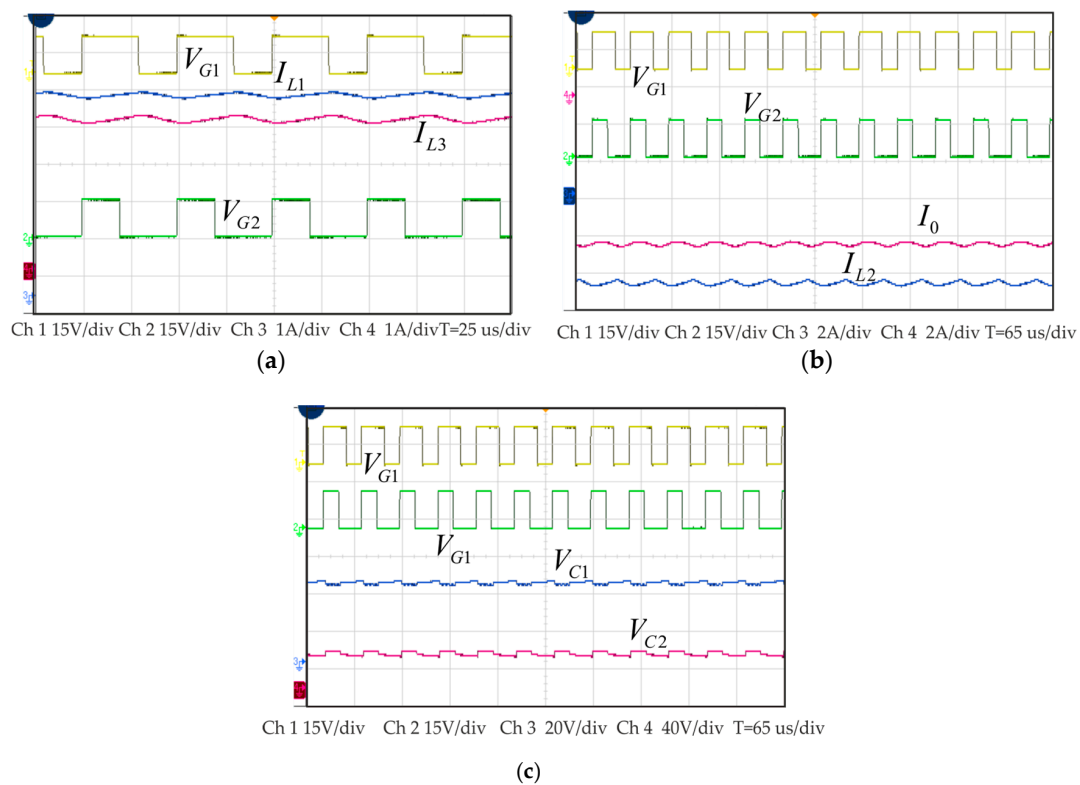
(**a**)

(**b**)

(**c**)

Figure 15. Various voltage and current measurements from experiments during Mode 1 with source 1 (Buck mode): (**a**) Gate signal, inductor currents through L_1, L_2 and load current (CH 1–4); (**b**) Gate signal and capacitor voltages across C_1 and C_2 (CH 1–3); (**c**) Gate signal, source voltages and output voltage (CH 1–3).

Figure 15a shows the current through the inductors L_1, L_2 and load current 1.4 A, 2.2 A and 2.17 A, under step down mode, which are closer to 1.39 A, 2.08 A, and 2.08 A calculated from (2) and (3). The corresponding ripples Δi_{L1}, Δi_{L2} and Δi_0 are within (1.55, 1.25 A), (2.4 and 2.0 A) and (2.3 and 2.1 A) respectively. It is found that the ripples are slightly more than the designed value of 5%. The voltage ripples of the capacitor are shown in Figure 15b. It can be seen that the ripples of capacitors are within (28.8, 29.55 V) for C_1 and (11.0 to 11.4 V) for C_2. The gate signal, source and output voltages are 15 V, 18 V and -11.2 V respectively, as shown in Figure 15c.

The performance of the converter was tested in DISO mode and the corresponding voltage and current signals are shown in Figure 16. The current through the inductors L_1 and L_3 with gate signal applied to both the switches are shown in Figure 16a. The inductor currents i_{L2} and i_0 are shown in Figure 16b. It can be observed that the average inductor currents are matching with results from (3), (14) and (15) and ripples are slightly more than the designed value of 5%. The voltage across the capacitors C_1 and C_2 are 40 V and 34 V respectively as shown in Figure 16c. It can be seen that the ripples of capacitors are within (36.5 V, 44.5 V) for C_1 and (31.5 to 39 V) for C_2. The obtained voltage ripples (approximately 10%) are more than the designed value (5%). However, it can be observed that the current of all the ports, I_{L1}, I_{L2} and I_0 are continuous with less ripples.

The response of the converter during transient load condition is shown in Figure 17. The load is varied to increase the load current from 0.6 A to 3.8 A. Approximately 20 s later, the load decreased to 0.8 A from 3.8 A. In both the cases, it is observed that the load voltage is regulated at 23.9 V which is closer to the desired value of 24 V. The load voltage magnitude is shown positive by using the probe with opposite polarity.

Ch 1 15V/div Ch 2 15V/div Ch 3 1A/div Ch 4 1A/divT=25 us/div

(**a**)

Ch 1 15V/div Ch 2 15V/div Ch 3 2A/div Ch 4 2A/div T=65 us/div

(**b**)

Ch 1 15V/div   Ch 2 15V/div   Ch 3 20V/div Ch 4 40V/div T=65 us/div

(**c**)

Figure 16. Various voltage and current measurements from experiments during Mode 2 with both sources: (**a**) Gate pulses of both switches and inductor currents through L_1 and L_3 (CH 1–4); (**b**) Gate pulses of switches, inductor currents through L_2 and L_0 (CH 1–4); (**c**) Gate signals of S_1 and S_2, and capacitor voltages across C_1 and C_2 (CH 1–4).

Ch 1 15V/div Ch 2 10A/div Ch 3 50V/div Ch 4 10A/div T=5 s/div
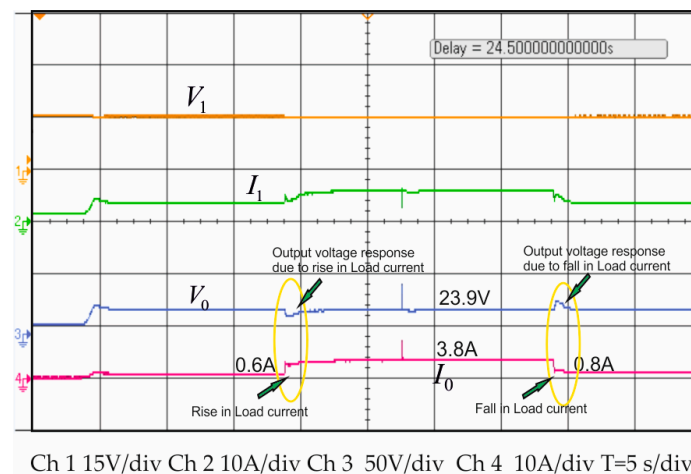
Figure 17. Voltages and currents from the experiment during transient condition. Input voltage, input current, load voltage and current (CH 1–4).

Figure 18a,b present the comparison plot between the theoretical, simulation and experimental absolute values of voltage gains as a function of duty ratio for SISO and DISO modes, respectively. It is obvious that both the theoretical and experimental voltage gains are increasing as the duty ratio increases. In addition, the voltage gain obtained from the experiment closely approximates the theoretical and the simulation results between 0.3 and 0.5, whereas a slight deviation has been observed in the duty ratio beyond 0.5 with increasing voltage difference. It is worth mentioning that this difference is due to the component losses.
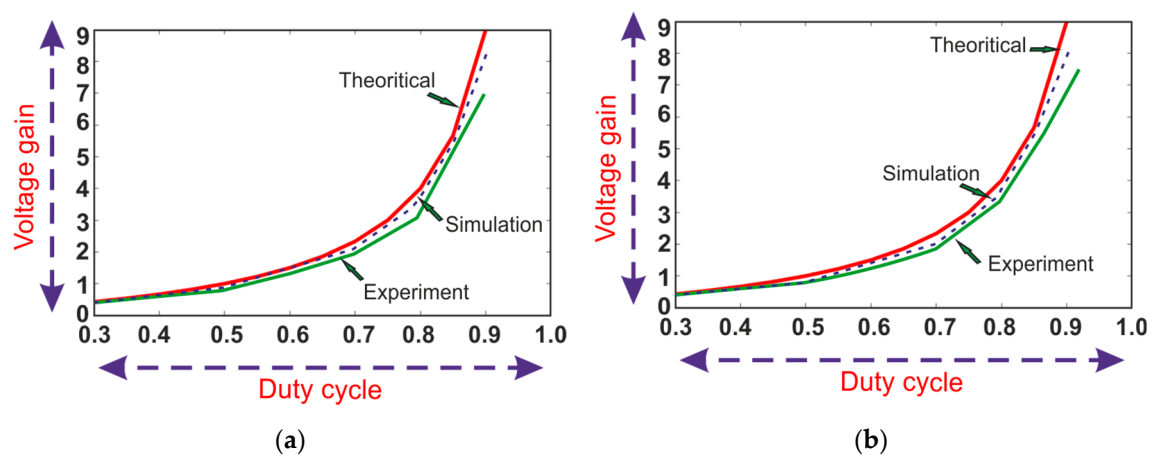
Figure 18. Voltage gain as a function of duty cycle (**a**) SISO mode (**b**) DISO mode.

Thus, the results validate the theoretical analysis and show the good feasibility of expected operation. Several tests are conducted and the maximum efficiency between the modes has been compared and plotted in a graph as shown in Figure 19, and the observed efficiencies for Mode 1 (SISO) with V_1 and V_2 sources are 92.74% and 91.15% respectively, and for Mode 2 is 90.43%. Comparing with efficiencies obtained through simulation, efficiencies for Mode 1 (SISO) with individual contribution of V_1 and V_2 sources are 94.13% and 93.66%, respectively, and for Mode 2 is 92.21%. Table 3 presents the comparison of various TP-NI converters with the proposed one. It is clear that the proposed converter provides continuous current at all the ports with a reduction in components.
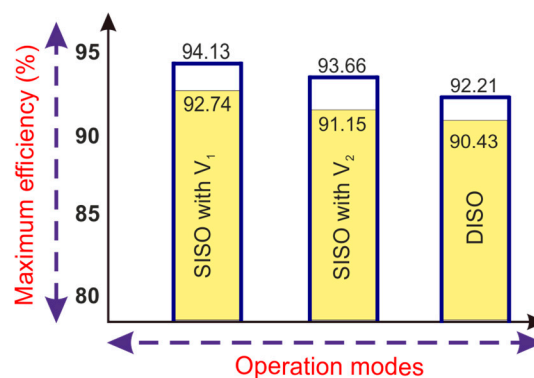

Figure 19. Maximum efficiency for various modes.

Table 3. Comparison of converters.

Circuit Elements	[5]	[10]	[22]	[30]	[31]	The Proposed Converter
Topology	Nonisolated	Nonisolated	Nonisolated	Nonisolated	Nonisolated	Nonisolated
Inductors	2	3	2	2	2 coupled	3
Capacitors	3	4	3	1	3	3
Active switches	4	3	3	4	5	2
Diodes	2	1	4	2	Nil	1
Common ground	Yes	Yes	Yes	Yes	Yes	Yes
Continuous current at all the ports	No	Yes	No	No	No	Yes
Prototype rating	400 W	1.2 kW	200 W	1 kW	200 W	100 W
Switching frequency	100 kHz	100 kHz	40 kHz	20 kHz	50 kHz	20 kHz
Maximum efficiency	96%	93.5%	92.7%	95.5%	90.1%	94.13%

6. Conclusions

In this paper a NI-TPC converter is synthesized using conventional Cuk converters to interface RS like Fuel cell and PV source. The operational modes and analysis of the converter are discussed in detail. Fewer active and passive components and a shared output inductor are the advantages of this converter. The continuous input and output currents are achieved owing to the presence of inductors. Therefore, this converter is appropriate for FC power supplies that necessitates continuous current with low ripple. The simulation and experimental results are provided to verify the feasibility of the proposed converter.

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