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An Efficient CMOS Dual Switch Rectifier for Piezoelectric Energy-Harvesting Circuits

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Abstract: In this research work, we investigated a dual switch (DS) active rectifier for the piezoelectric (PE) energy scavenging system. In the proposed DS active rectifier configuration, two extra switches are shunted across the PE transducer which helps the PE transducer's capacitor in charging and discharging which results in maximum power extraction from the PE transducer. Moreover, in the proposed rectifier configuration comparator controlled active diodes are used instead of conventional/passive diodes to minimize the threshold voltage V_{TH} drop. The proposed DS active rectifier design is fabricated in a 1-poly 6-metal 180-nm standard CMOS process. The simulation and measured results of the proposed DS active rectifier design have the better power conversion efficiency (PCE) of 91.5 %, which definitely helps in extracting more power than the conventional full bridge rectifier (FBR).

Keywords: piezoelectric transducer; active rectifier; energy harvesting; full bridge rectifier

1. Introduction

Energy Scavenging or Harvesting is a process in which energy can be derived/extracted from the various environmental sources like solar, thermal, RF, etc. [1–4]. Piezoelectric elements (PE) can be used to produce electrical energy from mechanical energy and it is quite a promising solution because of higher power density versus internal light and electromagnetic/electrostatic vibration. Usually, the PE transducers output is an irregular function of time and it needs to be rectified first to be usable. The most commonly used AC–DC converters are the conventional full bridge rectifiers (FBR) and half wave rectifiers. The drawback of these rectifiers is low power extraction and low conversion efficiency which introduced a switch only (single switch) rectifier [2,3]. It almost doubles the power extraction efficiency by the addition of a single switch across the PE transducer when it is compared with the conventional FBR circuit. In [2], the forward voltage drops across the rectifying diodes were a major source of conduction power loss and this issue is minimized by the use of the comparator based active diodes [3]. The work in [3–6] has designed the active rectifier and [3] redesign it and use it with a single switch which improves the power conversion efficiency [7–9]. In this research work, we introduce a dual switch active rectifier with high-power extraction and better conversion efficiency implemented on a 180-nm Complementary metal oxide semiconductor transistor (CMOS) process. An efficiency of 91.5% is achieved and this number is better than other reported rectifiers.

2. Proposed Rectifier and Circuit Implementation

2.1. Proposed DS Active Rectifier

The PE transducer shown in Figure 1 is usually modelled as a current source $i_p(t)$ shunted with the capacitor and a resistor i.e., C_p and R_p, where I_p is the amplitude of the current and f_p is the excitation frequency. The PE transducer output is not usable directly, as it is in a sinusoidal shape. It has to be rectified first and then it can be usable by the load circuits [1–5]. In order to increase the conversion efficiency of the conventional FBR as well as other rectifiers proposed in [1,2], we propose a CMOS dual switch (DS) active rectifier shown in Figure 1. In the proposed rectifier, two P-type (PMOS) transistors, MP1 and MP2, are configured in cross-coupled structure while other N-type (NMOS) transistors are implemented by using comparators C_1 and C_2 combined with two NMOS transistors MN1 and MN2. Two symmetrical switches in parallel with the PE transducer are used to discharge the PE transducer capacitor C_p completely. When the switch voltage Switch voltage (VSW) turns on for a brief time, it discharges the PE transducer capacitor C_p completely through the ground. C_{RECT} is the output capacitor and is used to store the harvested energy while R_{RECT} is the load resistor.

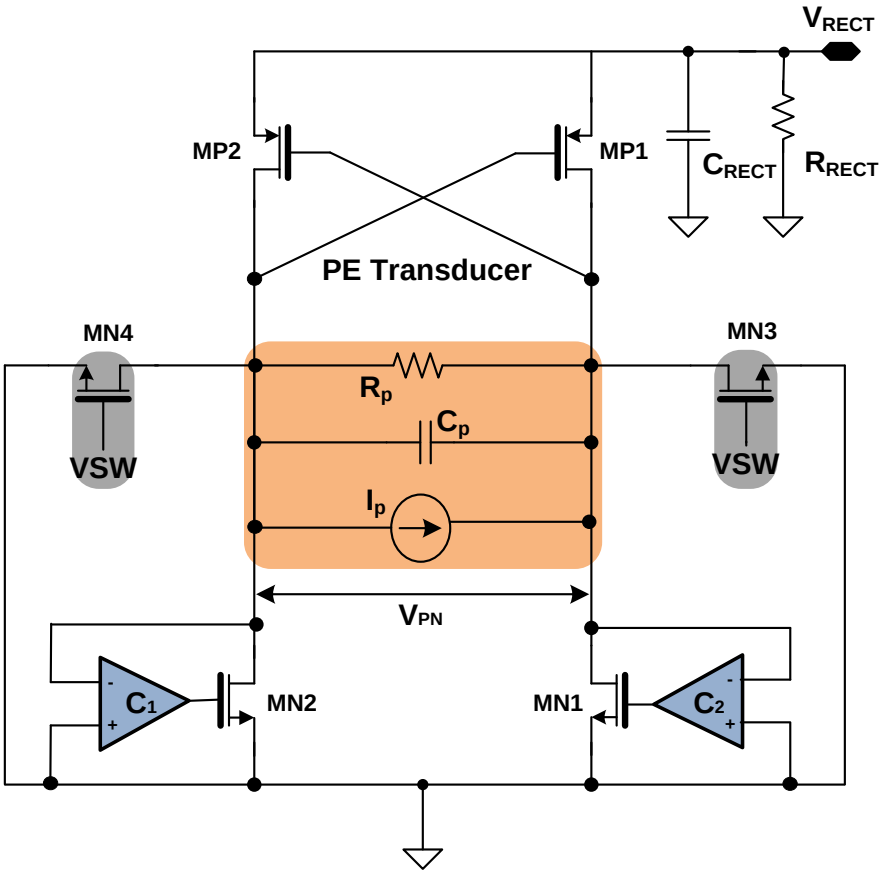


Figure 1. Schematic of the proposed DS active rectifier [3,10,11].

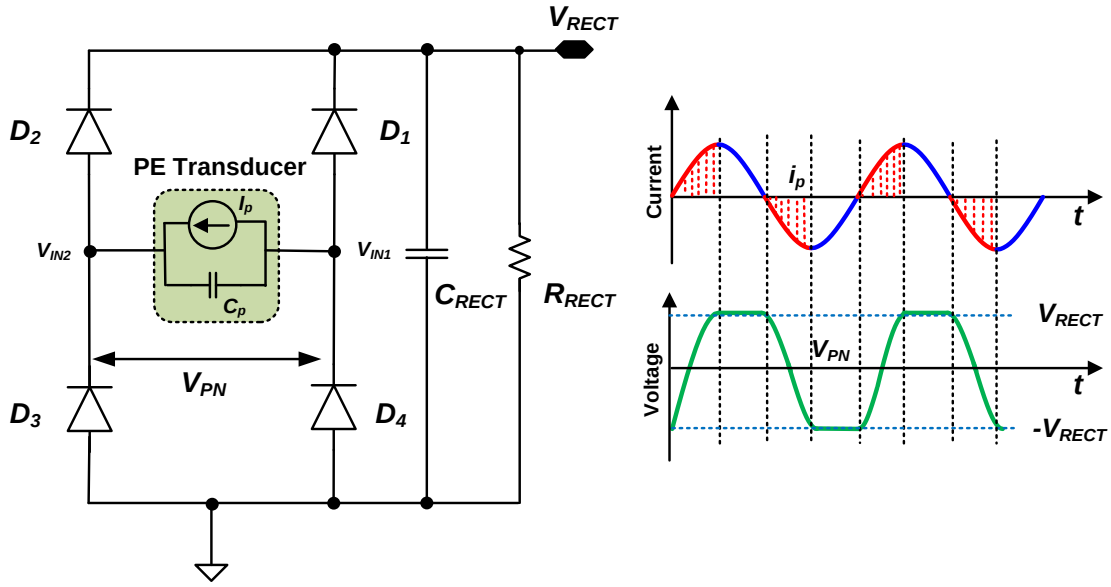
2.2. Operation Principle of Proposed DS Active Rectifier

Initially, the current I_p of PE transducer shown in Figure 1 is used to charge C_p. As I_p further increases i.e., V_{IN1} increases and V_{IN2} decreases. When the difference of V_{IN1} and V_{IN2} i.e., $V_{PN} = V_{IN1} - V_{IN2}$ is greater than the threshold voltage |Vthp| of the transistor, it turned on MP1. V_{IN1} is shorted to output V_{RECT}, further increase in V_{PN} decreases V_{IN2}, and it switched the comparators C_1 output to a high state and this turns on transistor MN2. As a result, a current path to load capacitor C_{RECT} is formed as both the transistors MP1 and MN2 are turned on. When

I_p approaches zero, the switch VSW turns on shortly and discharges completely the PE transducer capacitor C_p by shortening the nodes V_{IN1} and V_{IN2} to the ground. At this time, $V_{PN} = 0$ and both the transistor MP1 and MN2 turn off too, and the first cycle ends. In the next half cycle, the proposed DS active rectifier operates in a similar manner except that, now, MP2 and MN1 are involved. The adoption of two symmetrical switches help to charge and discharge instantly to transfer as much energy as possible.

2.3. Power Conversion and Extraction Analysis

For further understanding of the proposed rectifier, we analyze the power extraction and conversion process of the conventional full bridge rectifier (FBR). The conventional FBR with ideal diodes $D_1 - D_4$, its current pulse i_p, and waveform across the PE transducer i.e., V_{PN} is shown in Figure 2.



(**a**) (**b**)

Figure 2. (**a**) Schematic diagram of the conventional FBR; (**b**) Associated current and voltage waveforms.

Figure 2 shows that available charge in the PE transducer is not completely delivered at the output [2]. The shaded portion shows that, at every half cycle, the amount of charge is not delivered at the output, and the current waveform I_p from the PE transducer has to charge the capacitor C_p from $-V_{RECT}$ to $+V_{RECT}$ before the diodes turns on. This losted charge limits the amount of power that can be extracted using the conventional FBR. The charge that actually flows into the output capacitor C_{RECT} is just the difference between the total available charge and the lost charge [2]. The amount of charge available from the PE transducer is given as [12]

$$Q_{av/cycle} = \int_0^{\frac{2\pi}{\omega}} i_p dt = \frac{4I_p}{\omega_p} \tag{1}$$

where $i_p = I_p Sin(\omega_p t)$ and $\omega_p = 2\pi f_p$, the open circuit voltage is given as $I_p = \omega_p C_p V_p$. The Equation (1) can be written as

$$Q_{av/cycle} = 4C_p V_p \tag{2}$$

The charge per cycle lost will be

$$Q_{lost/cycle} = 4C_pV_{RECT} \tag{3}$$

The actual charge Q_{RECT} that flows into the output capacitor C_{RECT} per cycle is the difference between the total charge available and charge lost per cycle is given by

$$Q_{RECT/cycle} = Q_{av/cycle} - Q_{lost/cycle} \tag{4}$$

$$= 4V_pC_p - 4C_pV_{RECT}$$

$$= 4C_p(V_p - V_{RECT}) \tag{5}$$

The total energy per cycle is $E_{RECT/cycle} = Q_{RECT/cycle} \times V_{RECT}$

$$= 4C_pV_{RECT}(V_p - V_{RECT}) \tag{6}$$

Now the total power delivered at the output can be calculated using $P_{RECT(FBR)} = E_{RECT}/cycle \times f_P$

$$= 4C_pV_{RECT}f_p(V_p - V_{RECT}) \tag{7}$$

It is obvious that power vary with V_{RECT} and at $V_{RECT} = V_p/2$, it reach at its maximum value, than maximum power is

$$P_{RECT(FBR)}(max) = 4C_pV_p^2f_p \tag{8}$$

$$Q_{loss/cycle} = 2C_pV_{RCET} \tag{9}$$

The actual charge Q_{RECT} that flows at the

$$Q_{RECT/cycle} = 2C_p(2V_p - V_{RCET}) \tag{10}$$

The total energy delivered to C_{RECT} every cycle is given by

$$E_{RECT/cycle} = 2C_pV_{RECT}(2V_p - V_{RCET}) \tag{11}$$

The power delivered to the output by DS active rectifier is the product of the charge delivered V_{RECT} and frequency f_p as

$$P_{RECT/cycle} = 2C_pV_{RECT}f_p(2V_p - V_{RCET}) \tag{12}$$

The maximum power can be extracted by using DS active rectifier is

$$P_{RECT/DS}(max) = 2C_pV_{RECT}f_p(2V_p - V_{RCET}) \tag{13}$$

There are two major issues in conventional FBR. The first is its very poor power extraction capability and other one is the voltage drop across the diodes which results power losses. To overcome these issues, we propose DS active rectifier. The DS active rectifier combines the advantages of both conventional FBR and switch only rectifier in [2]. Figure 3 shows the current and voltage waveforms associated with the DS active rectifier. The switches across the PE transducer turned on for a brief time to discharge its capacitor C_p to ground at every zero crossing of the PE transducer current I_p.

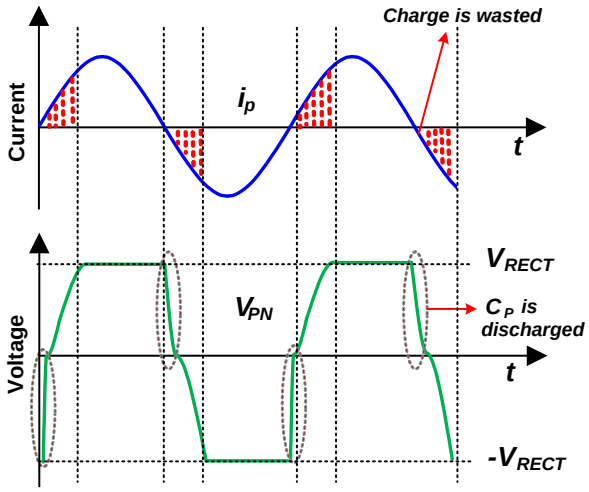


Figure 3. Current and voltage waveforms associated with the proposed DS active rectifier.

3. Results and Discussion

The proposed DS active rectifier shown in Figure 1 is implemented in 180-nm CMOS technology and is simulated and measured with the following transducer parameters, I_p = 490 µA, C_p = 130 nF, f_p = 200 Hz, and R_p = 1 MΩ. The values of load resistor R_{RECT} and capacitor C_{RECT} are 200 KΩ and 1 µF, respectively.

For comparison, a cross-coupled rectifier is implemented too. The transient voltages at the input and output of the proposed DS active rectifier and cross-coupled rectifier is shown in Figure 4. It is obvious that the use of two switches in parallel with the PE transducer, discharges the capacitor C_p to ground twice in a cycle, when current I_p crosses zero which results in higher value and higher power extraction compared to the cross-coupled active rectifier. It also shows the comparison of rectified output voltage V_{RECT} and the input voltage $V_{PN} = V_{IN1} - V_{IN2}$ of the DS active rectifier and cross-coupled rectifier. The V_{RECT} in flipping case is higher than the conventional one.

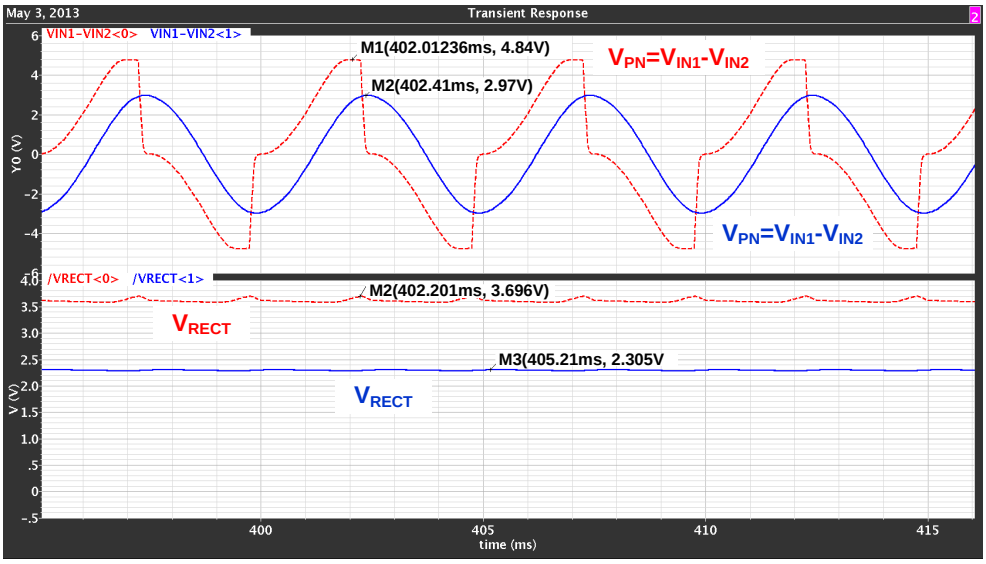


Figure 4. Comparison of transient voltage at the input and output of the proposed DS active rectifier and conventional cross-coupled rectifier.

Figure 5 shows the rectified output voltage V_{RECT} of the DS active rectifier and cross-coupled rectifier is 3.91 and 2.15 V, respectively. It starts from zero, when the PE-transducer is at rest. The output voltage increases when the traducer starts vibrating and reached at its steady state. The proposed

DS rectifier is simulated at different corners (tt, ff, ss) as well as for the verification of the design functionality are shown in Figure 6. It is shown that the maximum rectified output voltage can be seen at 'tt', while comparable rectified out voltage can be seen at 'ff' and 'ss'. This is because at 'ss' the threshold voltages of NMOS/PMOS becomes low which results in a low rectified output voltage. The same will happen at 'ff' corner as NMOS/PMOS transistors threshold voltage becomes high [13]. The theoretical maximum output power P_{RECT} of the proposed and conventional cross-coupled rectifier is 468 and 234 µW, respectively, and the calculated power of proposed and cross-coupled rectifier is 427 and 189 µW, respectively. The active area of the proposed DS active rectifier is 53 × 18 µm^2 and is shown in Figure 7. The efficiency of the proposed DS active rectifier is 91.5%. The performance summary of the proposed DS active rectifier and its comparison with other reported rectifiers is shown in Table 1. It is shown that the voltage and efficiency is the best when it is compared with the other reported designs in the literature [14–19]. The measured results of the proposed DS active rectifier are shown in Figure 8. For the measurement the PE transducer's equivalent model circuit is used instead of the actual PE transducer. It consists of an AC voltage source in series with a capacitor C_p is used. A sine wave of 200 Hz with 3-V pk-pk is placed in series with the C_p = 130 nF. The measured waveform V_{PN}, the control signal VSW and the rectified output voltage V_{RECT} is shown in Figure 8. The measured output voltage is 3.61 V while in simulation it is 3.91 V.

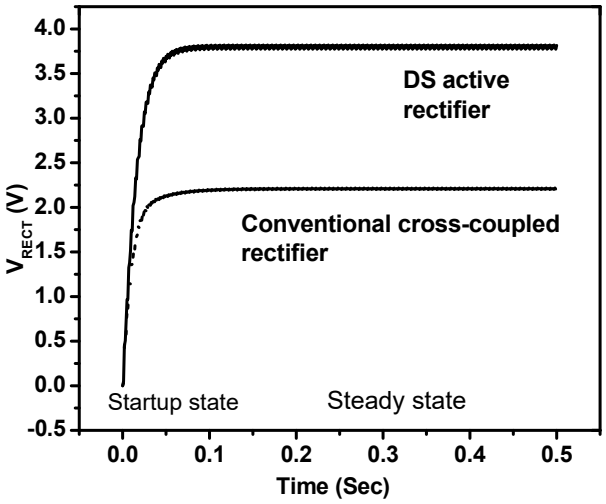


Figure 5. Comparison of transient voltage at the input of the proposed DS active rectifier and conventional cross-coupled rectifier.

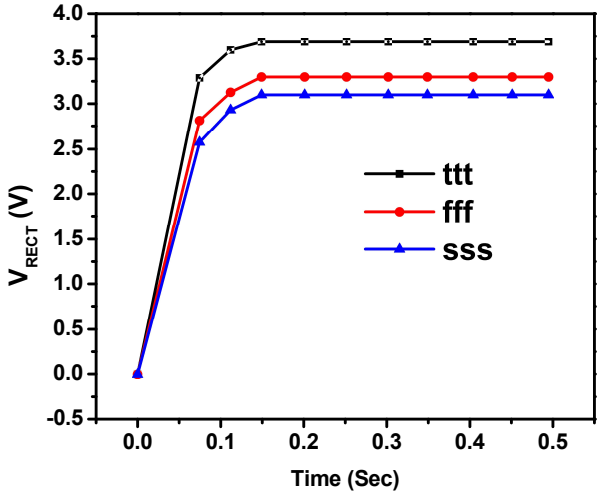


Figure 6. Proposed DS active rectifier simulations at different corners.

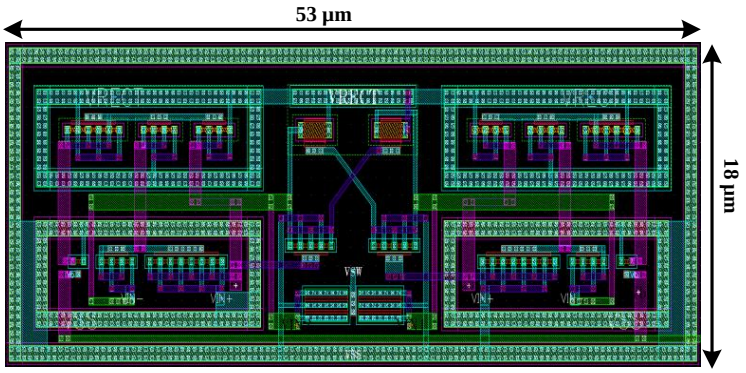


Figure 7. Layout of the proposed DS active rectifier.

Table 1. Performance Summary and Comparison of Different Rectifiers.

	TPE-15 [6]	TPE-11 [4]	ASSCC-13 [14]	JSSC-10 [2]	TPE-12 [3]	VLSI-11 [17]	This Work
Process	Discrete	Discrete	0.18 µm	0.35 µm	0.18 µm	0.35 µm	0.18 µm
Architecture	P-SSHI	Self Resonant	SSHI	Bias Flip	SW-Only	Comparator based	DS
V_{PN} (V)	2.47	20	2.23	2.4	2.8	1.8/3.2	3
f_o (Hz)	225	185	200	225	200	200	200
V_{RECT} (V)	1.9	1.81	3.6	3.2	2.78	NA	3.91
POUT-max (µW)	48	636	74	68	81	@Vs = 1.8 V 86.5/175 @Vs = 3.2 V 21/261	427
Efficiency (%)	58	NA	89	58	90	@Vs = 1.8 V 98.6 @Vs = 3.2 V 66	91.5

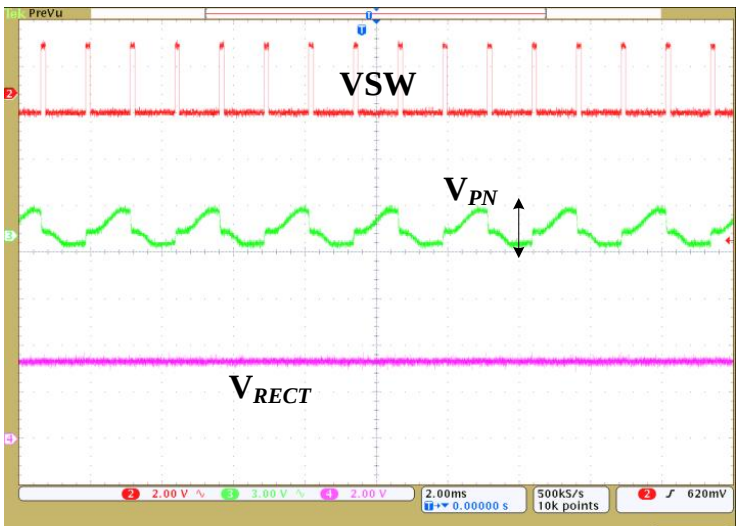


Figure 8. Measured results of the proposed DS active rectifier.

4. Conclusions

In this research, we show that a dual switch (DS) active rectifier for a piezoelectric (PE) energy scavenging system becomes more efficient by shunting two extra switches with the PE transducer. These switches can significantly increase power extraction from a PE transducer by discharging

the transducer capacitor in each half cycle. Moreover, in the proposed dual switch active rectifier configuration, passive diodes are swapped with the comparator-controlled active diodes to minimize the threshold voltage drop V_{TH}. The chip is fabricated using 0.18 µm CMOS process with an active area of 53 × 18 mm^2. The results show that the PCE of 91.5% is achieved. This figure is 4-times more, when it is compared with the conventional full bridge rectifier (FBR) circuit.

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Conflicts of Interest: The authors declare no conflict of interest.

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