

## Article

# Design of Lossless Negative Capacitance Multiplier Employing a Single Active Element

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**Abstract:** In this paper, a new negative lossless grounded capacitance multiplier (GCM) circuit based on a Current Feedback Operational Amplifier (CFOA) is presented. The proposed circuit includes a single CFOA, four resistors, and a grounded capacitor. In order to reduce the power consumption, the internal structure of the CFOA is realized with dynamic threshold-voltage MOSFET (DTMOS) transistors. The effects of parasitic components on the operating frequency range of the proposed circuit are investigated. The simulation results were obtained with the SPICE program using 0.13  $\mu\text{m}$  IBM CMOS technology parameters. The total power consumption of the circuit was 1.6 mW. The functionality of the circuit is provided by the capacitance cancellation circuit. PVT (Process, Voltage, Temperature) analyses were performed to verify the robustness of the proposed circuit. An experimental study is provided to verify the operability of the proposed negative lossless GCM using commercially available integrated circuits (ICs).

**Keywords:** capacitance multiplier; multiplication factor; active element; spice; Monte Carlo



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## 1. Introduction

High-value capacitors in IC technology require a large silicon area. To address this issue, capacitance multiplier (CM) circuits capable of multiplying capacitance have been proposed to obtain large capacitance from small capacitance values. Therefore, CM circuits play an essential role in obtaining high-value capacitances.

CM circuits can be classified as grounded [1–8] and floating [9–18] according to the type of the simulated capacitance, and positive [1–7] and negative [19–28] according to the value of the simulated capacitance.

A literature survey reveals that there are various CM circuits are reported using numerous versatile active building blocks (ABBs). However, upon careful examination of the circuit configurations published in the literature, they are considered to suffer from some of the limitations given below.

1. The circuits implemented with two or more active and passive elements have higher power consumption and a larger area on the chip.
2. They are practically not applicable with commercially available ICs.
3. The multiplication factor is not electronically adjustable.

Four negative CFOA-based CM circuit topologies have been proposed by Lahiri and Gupta [19]. While the first two proposed circuits contain two CFOAs, the other circuits consist of a single CFOA. All circuits are designed using two resistors and a single capacitor. Additionally, the circuits do not require any critical component matching conditions. All of the circuits in SPICE have been tested using the AD844 macro model. A capacitance cancellation circuit and a quadratic oscillator circuit are given as application examples. The resistance-controlled negative capacitance multiplier circuit presented by Abuelma'atti

and Dhar consists of two CFOAs, two floating resistors, and a floating capacitor [20]. The negative CM circuit proposed by Dogan and Yuce includes a single CFOA, three resistors, and a capacitor [21]. The circuit proposed by Al-Absi and Abuelma'atti includes one CFOA and two OTAs. It is configured as an OTA-negative resistor to achieve an adjustable negative impedance multiplier [22]. The resistor-free circuit presented by Stornelli et al. consists of an E-VCII- and a capacitor [23].

Many of the negative CMs available in the literature contain two or more ABBs [19,20,22,24,25,27,28]. There are also circuits that contain only one active device [19,21,23,26,29–31]. When designing negative CMs, excessive use of active and passive elements should be avoided as this will increase power consumption. Negative CMs presented by researchers have generally been realized through the use of three or more passive elements [19–21,24,25,28,30,31]. Negative CMs containing a single capacitor have also been proposed, but each of these circuits operates with two or more active components [22,27].

The aim of this work was to design a negative lossless GCM circuit using currently commercially available ICs, namely the AD844 [32]. The proposed circuit is designed with a single CFOA, four resistors and a grounded capacitor. The internal structure of the CFOA is built with DTMOS transistors to reduce power consumption. The total power consumption of the circuit is 1.6 mW. The non-ideal analysis for the proposed circuit has been investigated in detail. A capacitance cancellation circuit is presented as an application example. To verify the operability of the proposed circuit, it has been experimentally tested using commercially available ICs, namely AD844s.

The paper is structured as follows: Section 2 introduces the proposed circuit utilizing a CFOA. The non-ideal analysis is given in Section 3. SPICE simulation results and discussions are given in Section 4. An application example is presented in Section 5. Finally, Section 6 concludes the paper.

## 2. The Proposed Circuit

The terminal relations of CFOAs, whose circuit symbol and equivalent circuit are given in Figures 1 and 2, respectively, can be represented in the following matrix equation:

$$\begin{bmatrix} I_Y \\ I_Z \\ V_X \\ V_W \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ \alpha(s) & 0 & 0 & 0 \\ 0 & \beta(s) & 0 & 0 \\ 0 & 0 & \eta(s) & 0 \end{bmatrix} \begin{bmatrix} I_X \\ V_Y \\ V_Z \\ I_W \end{bmatrix} \quad (1)$$

where  $\alpha(s)$  represents the current gain which is ideally equal to unity. Also, the  $\beta(s)$  and  $\eta(s)$  correspond to voltage gains and ideally both of them are equal to unity. Furthermore,  $\alpha(s)$ ,  $\beta(s)$ , and  $\eta(s)$  can be given by

$$\alpha(s) = \frac{\omega_\alpha(1 - \varepsilon_\alpha)}{s + \omega_\alpha} \quad (2)$$

$$\beta(s) = \frac{\omega_\beta(1 - \varepsilon_\beta)}{s + \omega_\beta} \quad (3)$$

$$\eta(s) = \frac{\omega_\eta(1 - \varepsilon_\eta)}{s + \omega_\eta} \quad (4)$$

Herein,  $\varepsilon_\alpha$  represents the current-tracking error, ideally equal to zero, while  $\varepsilon_\beta$  and  $\varepsilon_\eta$  denote the voltage tracking errors, also ideally equal to zero. It is assumed that  $|\varepsilon_\alpha|$ ,  $|\varepsilon_\beta|$ , and  $|\varepsilon_\eta|$  are significantly smaller than one.

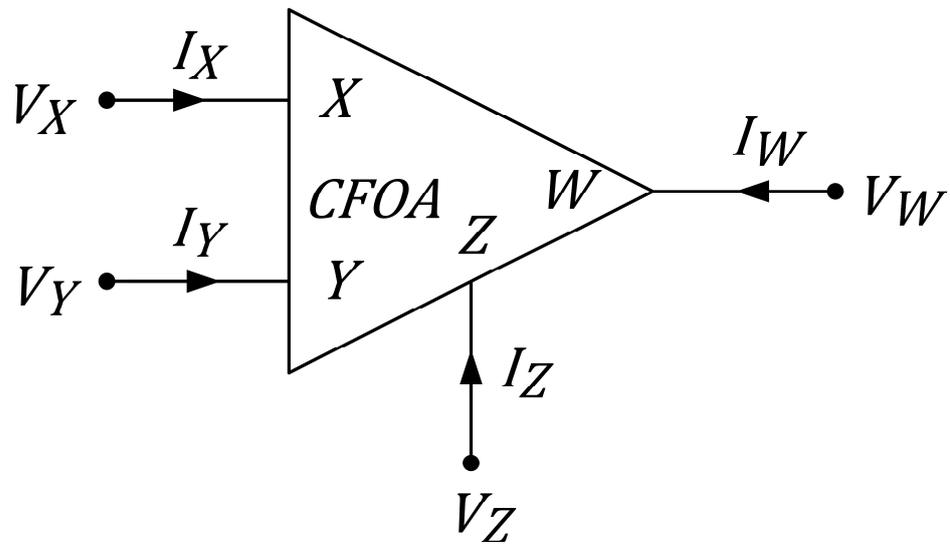


Figure 1. Circuit symbol of the CFOA.

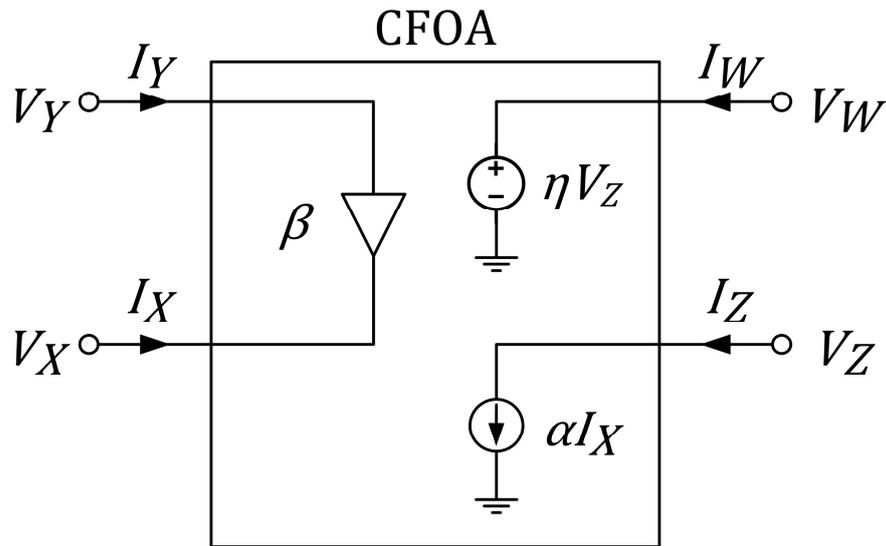


Figure 2. Equivalent circuit of the CFOA.

In addition,  $\omega_\alpha$ ,  $\omega_\beta$ , and  $\omega_\eta$  denote corner frequencies of the relevant parameter. Furthermore, in an ideal case,  $R_{in}$  is infinity and the port relationships of the CFOA are expressed by the following equations:  $V_X = V_Y$ ,  $I_Y = 0$ ,  $I_Z = I_X$ , and  $V_W = V_Z$ .

The proposed negative lossless GCM is depicted in Figure 3. Without passive element matching conditions, the input admittance ( $Y_{in}$ ) of the circuit is obtained as follows:

$$Y_{in}(s) = \frac{I_{in}}{V_{in}} = -\frac{(R_3 + R_4)(R_2 - R_1 + sCR_1R_2)}{R_1R_3(R_2 + R_4)} \tag{5}$$

If  $R_2 = R_1$  is selected for the circuit in Figure 3, the input admittance is simplified as follows. When this condition is met, the circuit can simulate negative lossless GCM. The equivalent capacitance ( $C_{eq}$ ) and the multiplication factor ( $K$ ) are given by

$$Y_{in}(s) = \frac{I_{in}}{V_{in}} = sC_{eq} = sCK = sC \left[ -\frac{R_1(R_3 + R_4)}{R_3(R_1 + R_4)} \right] \tag{6}$$

$$C_{eq} = CK = C \left[ -\frac{R_1(R_3 + R_4)}{R_3(R_1 + R_4)} \right] \tag{7}$$

$$K = -\frac{R_1(R_3 + R_4)}{R_3(R_1 + R_4)} \tag{8}$$

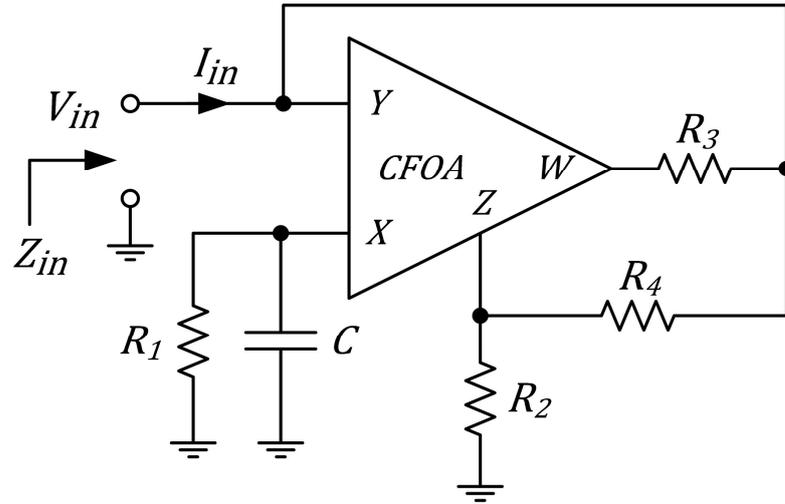


Figure 3. The proposed negative lossless grounded capacitance multiplier.

As can be seen from Equation (8), if one of the resistors  $R_3$  or  $R_4$  is replaced with an MOS-based voltage-controlled resistor, the multiplication factor becomes electronically controllable.

The sensitivity of the  $K$  with respect to the tuning resistors is given below.

$$S_{R_1}^K = \frac{R_4}{R_1 + R_4} \tag{9}$$

$$S_{R_3}^K = -\frac{R_4}{R_3 + R_4} \tag{10}$$

$$S_{R_4}^K = \frac{R_4(R_1 - R_3)}{(R_1 + R_4)(R_3 + R_4)} \tag{11}$$

### 3. Non-Ideal Analysis

The non-ideal equivalent circuit of a CFOA is shown in Figure 4. Here,  $R_X$ ,  $R_Z$ , and  $R_W$  indicate parasitic resistors. Also,  $C_Y$  and  $C_Z$  demonstrate the parasitic capacitors. Ideally, these parasitic elements are  $R_X = R_W = C_Z = C_Y = 0$  and  $R_Z = \infty$ . The terminal relations of the CFOA in non-ideal conditions are given in Equation (12).

$$\begin{bmatrix} I_Y \\ I_Z \\ V_X \\ V_W \end{bmatrix} = \begin{bmatrix} 0 & sC_Y & 0 & 0 \\ \alpha(s) & 0 & sC_Z + 1/R_Z & 0 \\ R_X & \beta(s) & 0 & 0 \\ 0 & 0 & \eta(s) & R_W \end{bmatrix} \begin{bmatrix} I_X \\ V_Y \\ V_Z \\ I_W \end{bmatrix} \tag{12}$$

Taking into account the effects of the non-ideal gains of the CFOA, the input admittance of the circuit is obtained as follows.

$$Y_{in}(s) = \frac{R_3(1 - \alpha\beta) + R_4(1 - \alpha\beta\eta) + R_1(1 - \eta) - \alpha\beta R_1(R_3 + \eta R_4)sC}{R_3(R_1 + R_4)} \quad (13)$$

Considering the non-ideal gains of the CFOA, the equivalent circuit of the proposed circuit is given in Figure 5; the values of the equivalent components are given in Equations (14)–(16).

$$R_{eq} = \frac{R_3(R_1 + R_4)}{R_3(1 - \alpha\beta) + R_4(1 - \alpha\beta\eta) + R_1(1 - \eta)} \quad (14)$$

$$C_{eq} = CK = -\frac{\alpha\beta R_1(R_3 + \eta R_4)}{R_3(R_1 + R_4)} C \quad (15)$$

$$K = -\frac{\alpha\beta R_1(R_3 + \eta R_4)}{R_3(R_1 + R_4)} \quad (16)$$

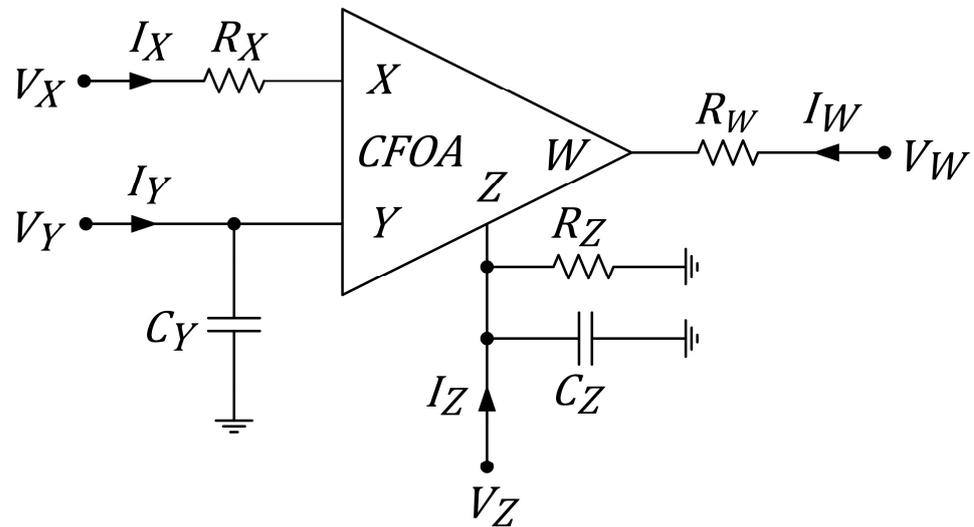


Figure 4. Parasitic impedances of the CFOA.

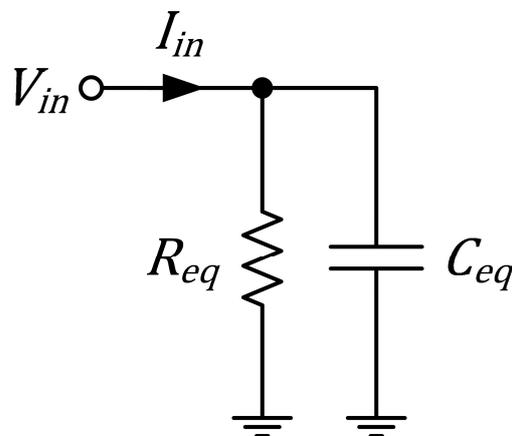


Figure 5. Equivalent circuit taking into account the non-ideal gains of the CFOA.

The sensitivity analysis is given below.

$$S_{\alpha}^K = S_{\beta}^K = 1 \quad (17)$$

$$S_{\eta}^K = \frac{\eta R_4}{(R_3 + \eta R_4)} \quad (18)$$

$$S_{R_1}^K = \frac{R_4}{R_1 + R_4} \quad (19)$$

$$S_{R_3}^K = -\frac{\eta R_4}{(R_3 + \eta R_4)} \quad (20)$$

$$S_{R_4}^K = -\frac{R_4(R_3 - \eta R_1)}{(R_1 + R_4)(R_3 + \eta R_4)} \quad (21)$$

Under the specified condition where only the parasitic impedances of the X, Y, Z, and W terminals are considered, the input admittance is derived in the form presented in Equation (22).

$$Y_{in}(s) = \frac{a_0 + a_1s + a_2s^2}{b_0 + b_1s + b_2s^2} \quad (22)$$

In this context,  $a_i$  and  $b_i$  represent the real coefficients of the driving point admittance  $Y_{in}(s)$ .

$$a_0 = ((R_3 + R_W) + R_4)[R_1 + R_X - (R_1 \parallel R_Z)] \quad (23)$$

$$a_1 = R_4(R_3 + R_W)[CR_1(R_X - (R_1 \parallel R_Z)) + C_Z(R_1 + R_X)] \quad (24)$$

$$a_2 = CC_Z R_1 R_X (R_1 \parallel R_Z) ((R_3 + R_W) + R_4) \quad (25)$$

$$b_0 = (R_1 + R_X)(R_3 + R_W)(R_4 + (R_1 \parallel R_Z)) \quad (26)$$

$$b_1 = [CR_1 R_X (R_3 + R_W)(R_4 + (R_1 \parallel R_Z)) + C_Z R_4 (R_3 + R_W)(R_1 \parallel R_Z)(R_1 + R_X)] \quad (27)$$

$$b_2 = CC_Z R_1 R_4 R_X (R_3 + R_W)(R_1 \parallel R_Z) \quad (28)$$

In the ideal case, the input admittance of the capacitor is of the form  $Y_{in}(s) = a_1s/b_0$ . To obtain a lossless capacitor, the terms other than  $a_1s$  and  $b_0$  need to be small enough. In other terms, when  $s$  is substituted with  $j\omega$ , the following inequalities must be concurrently fulfilled to approximate the ideal capacitor admittance:

$$|a_0| \ll |a_1 \times (j\omega)| \Rightarrow f \gg f_L = \frac{1}{2\pi} \left( \frac{a_0}{a_1} \right) \quad (29)$$

$$|a_2 \times (j\omega)^2| \ll |a_1 \times (j\omega)| \Rightarrow f \ll f_{H1} = \frac{1}{2\pi} \left( \frac{a_1}{a_2} \right) \quad (30)$$

$$|b_1 \times (j\omega)| \ll |b_0| \Rightarrow f \ll f_{H2} = \frac{1}{2\pi} \left( \frac{b_0}{b_1} \right) \quad (31)$$

$$|b_2 \times (j\omega)^2| \ll |b_0| \Rightarrow f \ll f_{H3} = \frac{1}{2\pi} \sqrt{\frac{b_0}{b_2}} \quad (32)$$

According to the inequalities given above, the operating frequency range of the proposed circuit is calculated approximately as follows.

$$f \gg f_L = \frac{1}{2\pi} \left( \frac{a_0}{a_1} \right) \tag{33}$$

$$f \ll f_H = \frac{1}{2\pi} \min \left\{ \frac{a_1}{a_2}, \frac{b_0}{b_1}, \sqrt{\frac{b_0}{b_2}} \right\} \tag{34}$$

#### 4. Simulation Results

In order to reduce the power consumption of analog integrated circuits, operations with lower supply voltages can be provided by DTMOS technology [33–37]. To obtain a DTMOS transistor, the body and gate terminals of the MOSFET are short-circuited as shown in Figure 6. The DTMOS-based implementation of the CFOA, derived from the CCII+ presented in reference [38], is depicted in Figure 7.

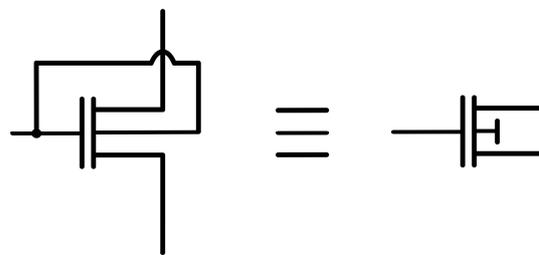


Figure 6. DTMOS transistor and its circuit symbol [39].

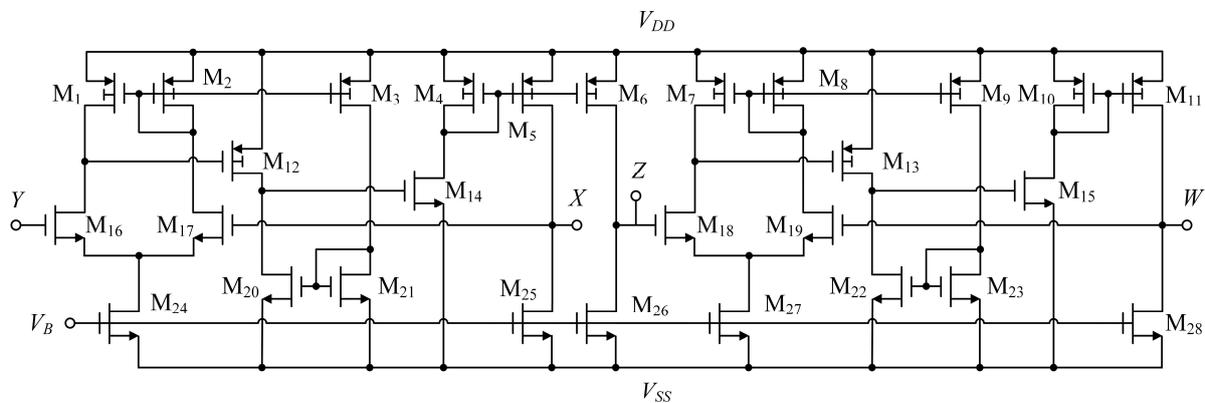


Figure 7. Internal structure of the CFOA using DTMOS transistors [8].

The simulation results have been obtained utilizing the SPICE program, employing 0.13 μm IBM CMOS technology parameters. The power supply and bias voltage were chosen as  $V_{DD} = -V_{SS} = 0.6$  V and  $V_B = -0.2$  V, respectively. The transistor dimensions are detailed in Table 1. The parasitic impedances and non-ideal gains of the CFOA are delineated in Table 2.

Table 1. The transistor dimensions.

Transistors	W (μm)/L (μm)
M <sub>1</sub> –M <sub>13</sub>	130/0.65
M <sub>14</sub> , M <sub>15</sub> , M <sub>20</sub> –M <sub>23</sub> , M <sub>25</sub> , M <sub>26</sub> , M <sub>28</sub>	13/0.65
M <sub>24</sub> , M <sub>27</sub>	26/0.65
M <sub>16</sub> –M <sub>19</sub>	15.6/0.26

**Table 2.** Parasitic impedances and non-ideal gains of the CFOA.

Parasitic Impedances	Values
$R_X$	0.637 $\Omega$
$R_W$	0.637 $\Omega$
$R_Z$	20.04 k $\Omega$
$C_Z$	66 fF
$C_Y$	8.23 fF
$\alpha$	0.999972
$\beta$	1.000009
$\eta$	1.000009

The functionality of the proposed negative GCM was examined under the following simulation conditions. Detailed simulation settings are included in Table 3.

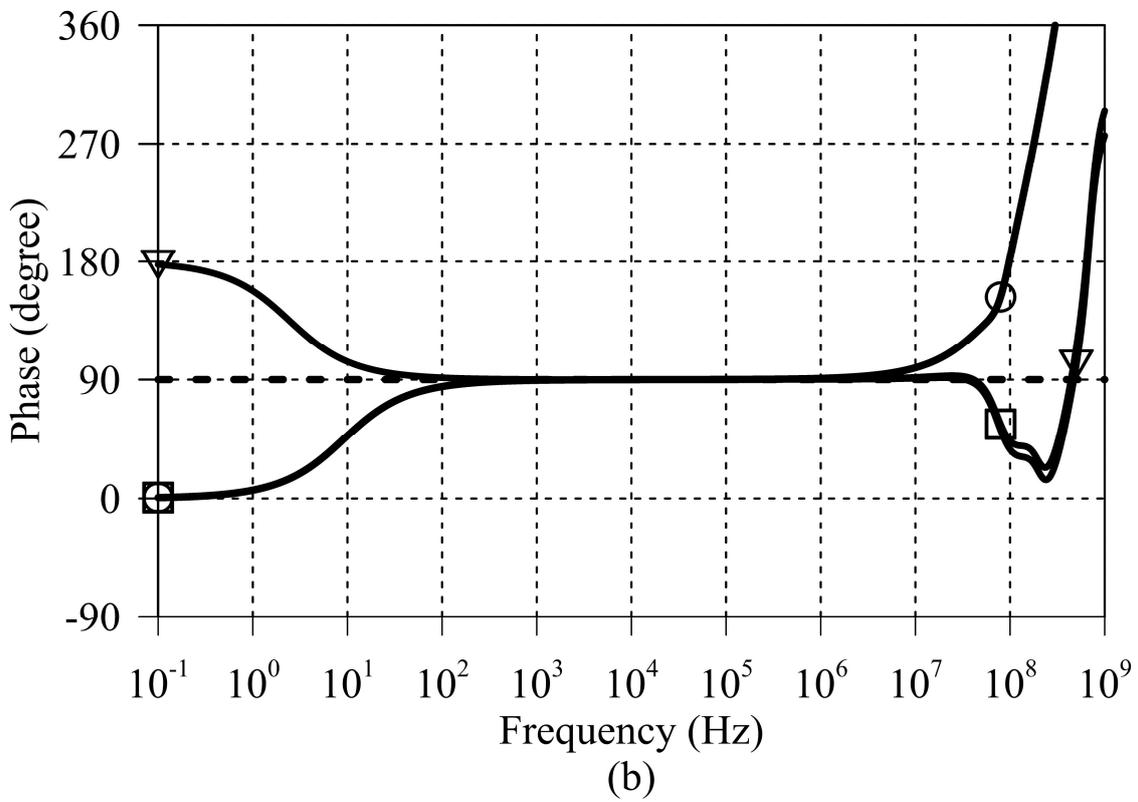
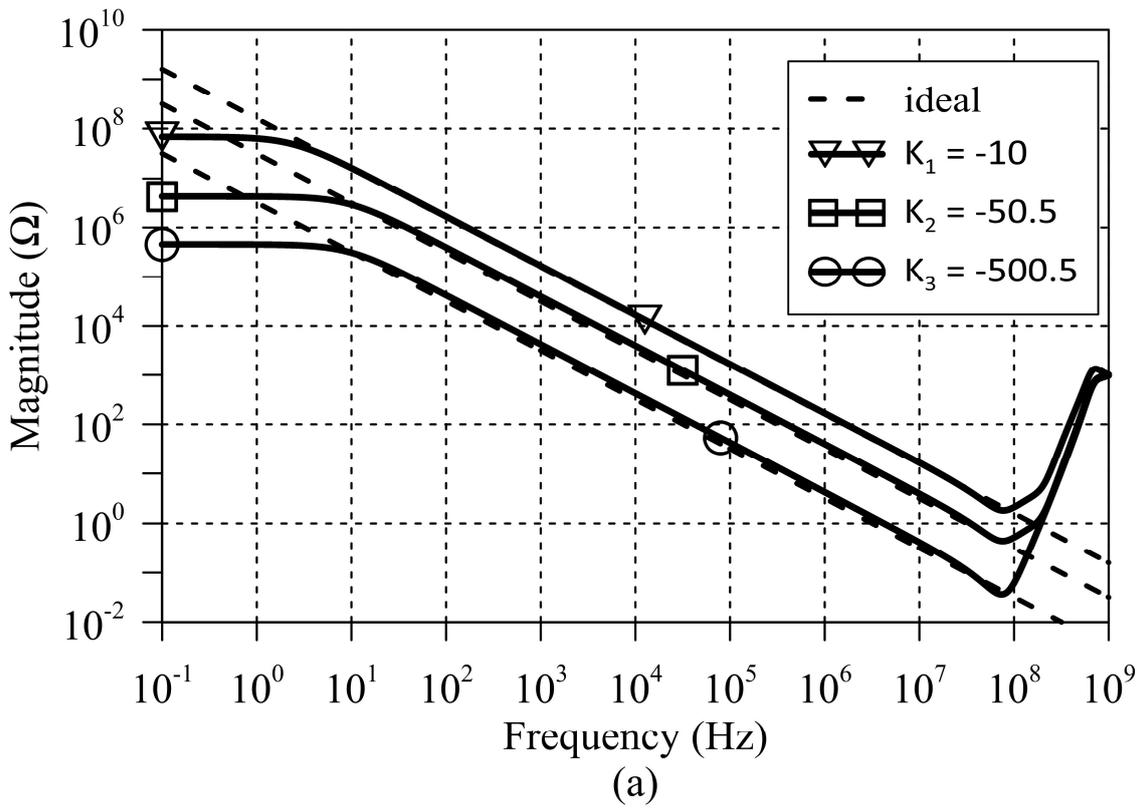
- (i) Multiplication factor ( $K$ ) is constant while  $C$  is variable;
- (ii)  $C$  is constant while  $K$  is variable.

**Table 3.** Detailed simulation results and passive component settings.

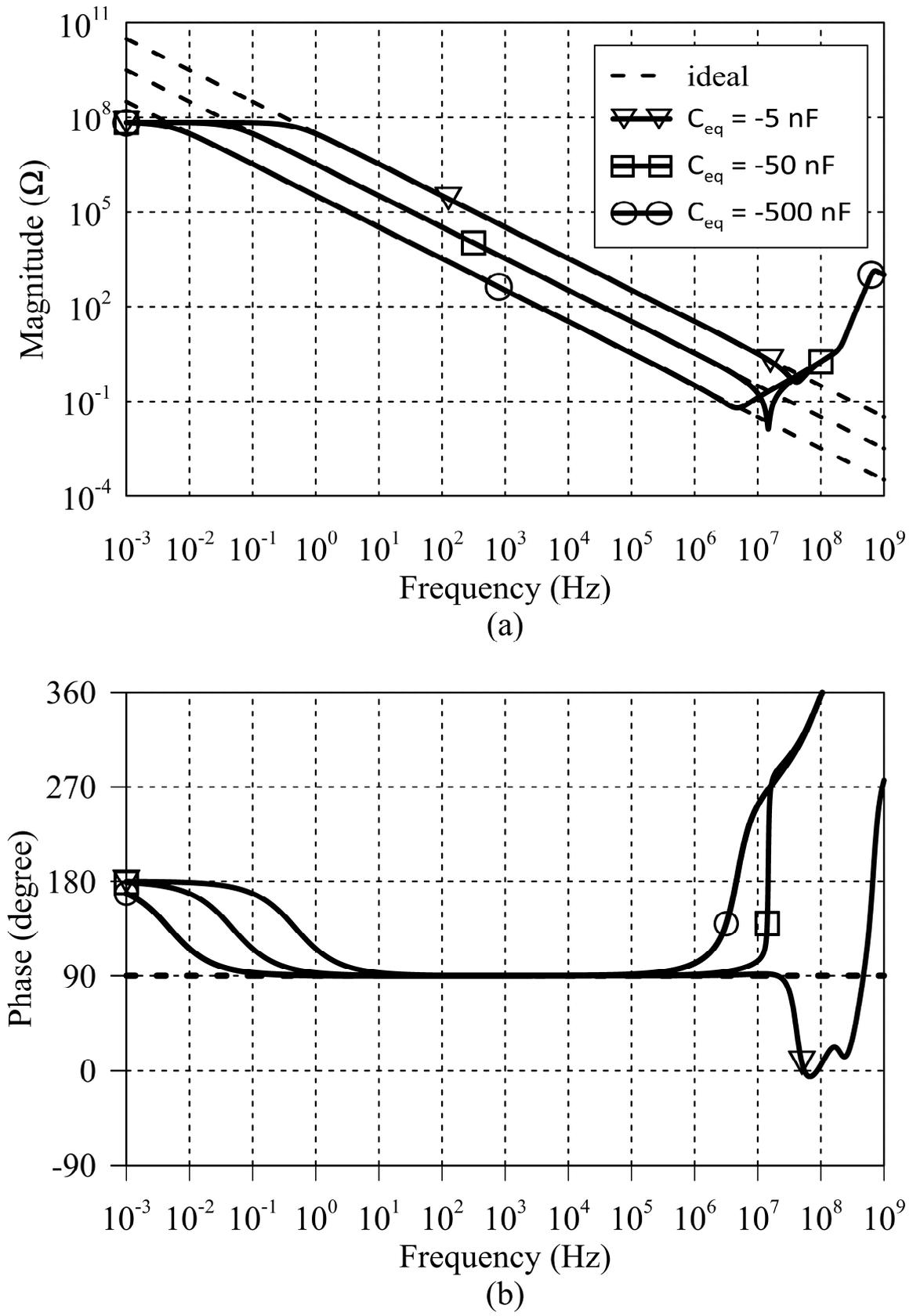
Case	Passive Components					$K$	$C_{eq}$ (nF)	Frequency Response	
	$C$ (nF)	$R_1$ (k $\Omega$ )	$R_2$ (k $\Omega$ )	$R_3$ ( $\Omega$ )	$R_4$ (k $\Omega$ )			Magnitude within 10% Error	Phase within 10° Error
1	0.1	10	10	100	1	-10	-1	4 Hz to 80 MHz	14 Hz to 53 MHz
		10	10	100	10	-50.5	-5.05	9 Hz to 35 MHz	52 Hz to 47 MHz
		10	10	10	10	-500.5	50.05	9 Hz to 32 MHz	53 Hz to 11 MHz
2	0.5	10	10	100	1	-10	-5	1 Hz to 52 MHz	3 Hz to 30 MHz
	5						-50	1 Hz to 20 MHz	1 Hz to 15 MHz
	50						-500	1 Hz to 4.5 MHz	1 Hz to 4.5 MHz

The frequency response of the input impedance of the proposed negative lossless GCM is given in Figure 8 for various multiplication factors ( $K$ ). By selecting the passive elements as  $C = 100$  pF,  $R_1 = R_2 = 10$  k $\Omega$ ,  $R_3^1 = R_3^2 = 100$   $\Omega$ ,  $R_3^3 = 10$   $\Omega$ ,  $R_4^1 = 1$  k $\Omega$ , and  $R_4^2 = R_4^3 = 10$  k $\Omega$ , the multiplication factors are set to  $K_1 = -10$ ,  $K_2 = -50.5$ , and  $K_3 = -500.5$ , resulting in  $C_{eq} = -1$  nF,  $-5.05$  nF, and  $-50.05$  nF, respectively. In Figure 9, a comparison of the proposed negative GCM with the ideal capacitor for  $C_{eq} = 5, 50$ , and  $500$  nF is given by selecting  $K = 10, C = 0.5, 5$ , and  $50$  nF, respectively. The frequency responses of the proposed circuit to various supply voltages are shown in Figure 10. Monte Carlo (MC) simulations were conducted for 100 runs. The simulation results for a 10% change in the threshold voltages and gate oxide thicknesses of all MOS transistors and a 5% change in the width of all MOS transistors are shown in Figures 11 and 12, respectively. A temperature analysis of the circuit is also depicted in Figure 13.

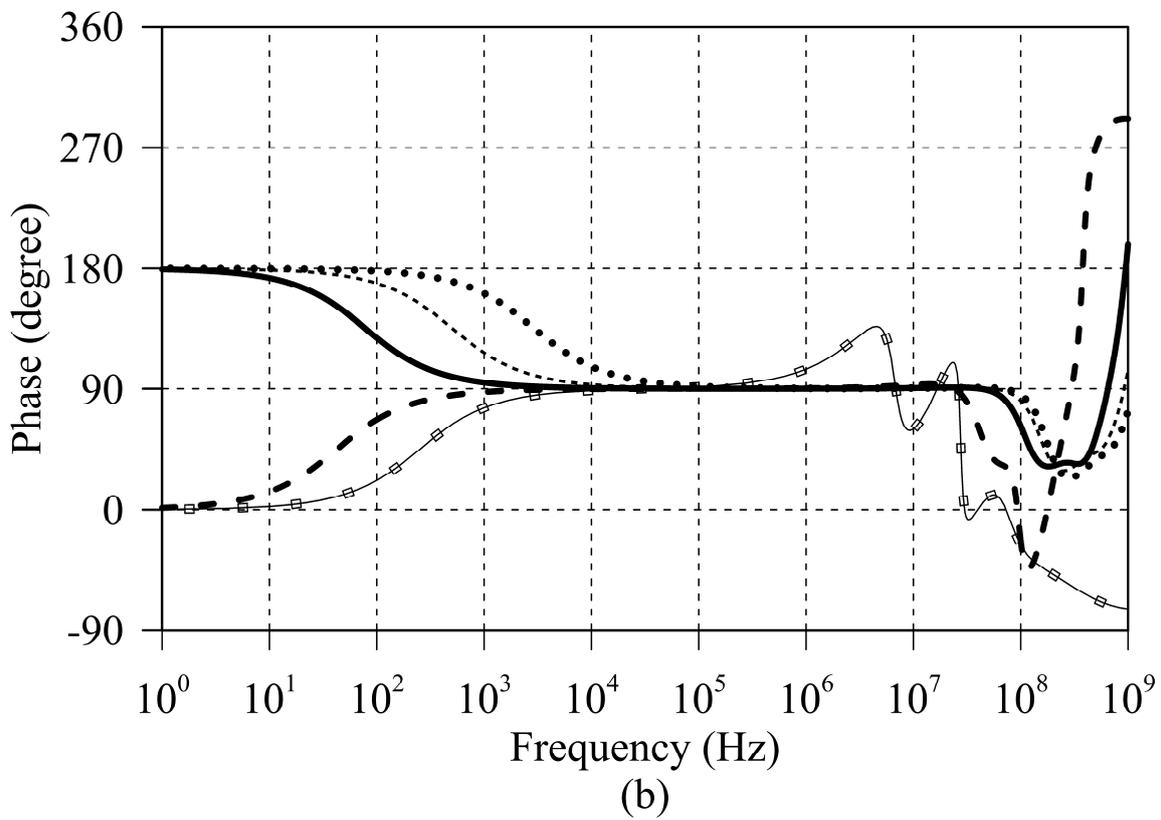
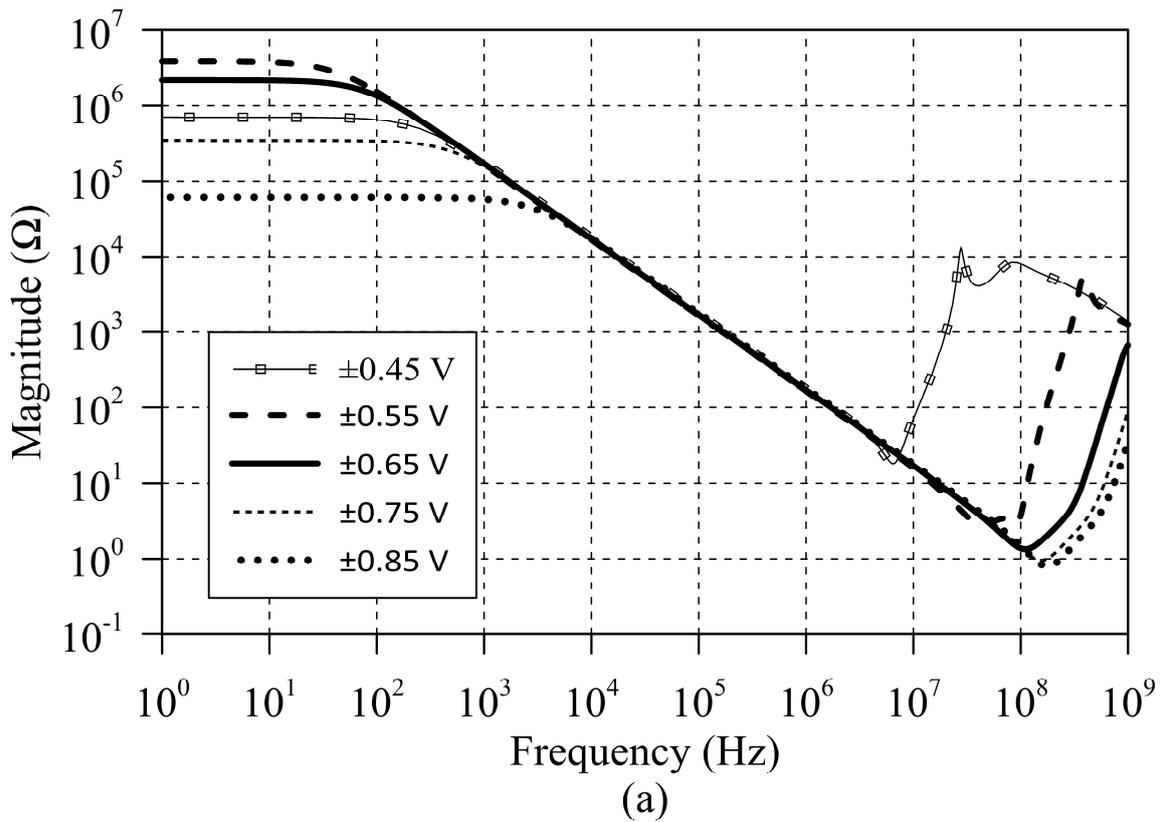
A table of comparisons of previously reported negative CM circuits using various ABBs can be seen in Table 4. The proposed circuit contains a single CFOA. Compared to other circuits implemented with a single active component, the number of passive elements is relatively high. However, to reduce power consumption, the internal structure of the CFOA is designed using the DTMOS technique. Power consumption can be reduced by using MOS-based resistors. The multiplication factor of the circuit can be adjusted up to 500. In addition, according to Figure 8, the operating frequency reaches 80 MHz. Considering its simplicity, operating frequency, and multiplication factor, it is clear that the proposed circuit is superior to the circuits in the literature.



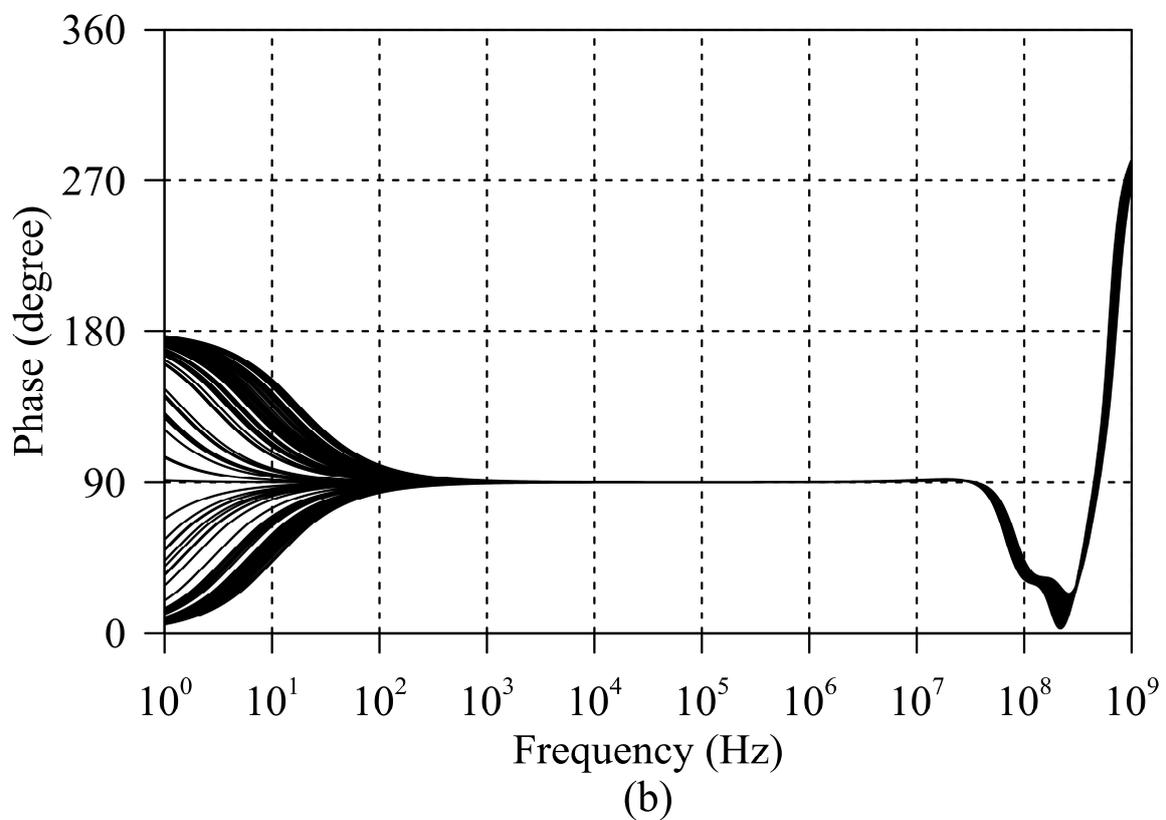
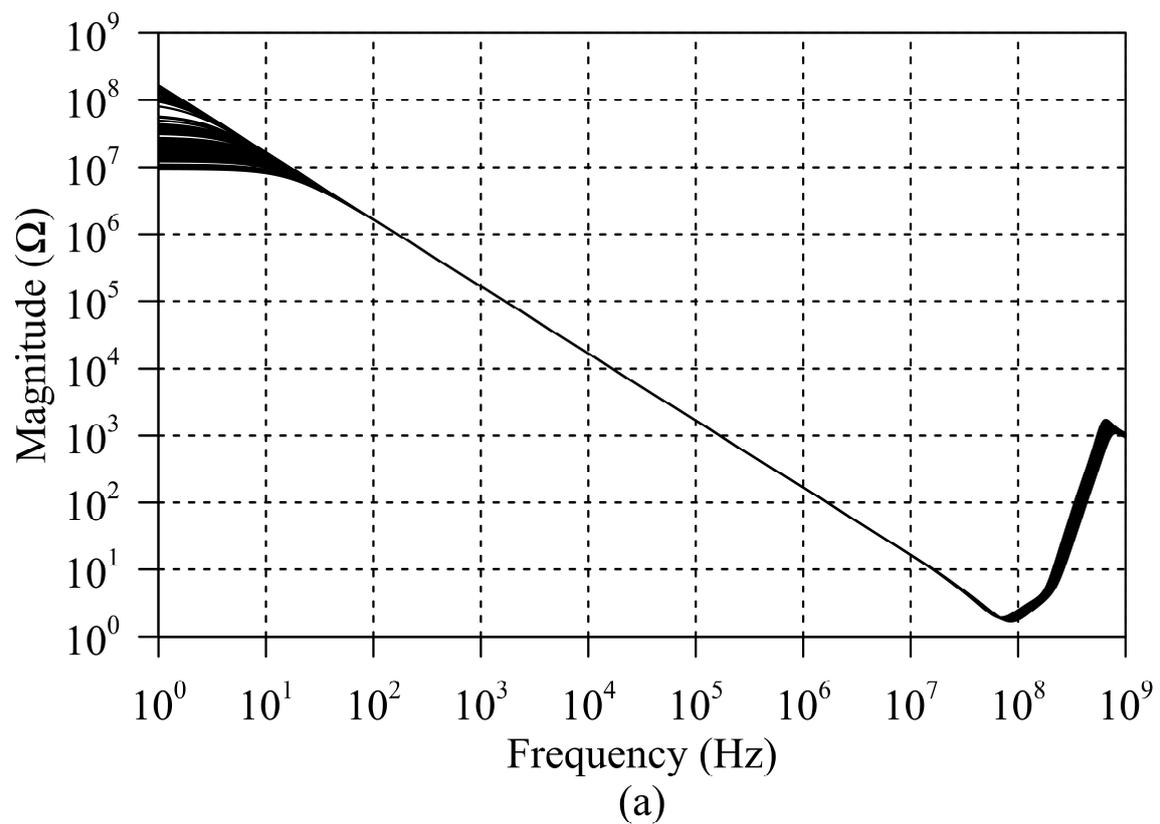
**Figure 8.** Frequency response of the proposed negative lossless GCM and ideal capacitor for  $K = -10$ ,  $-50.5$ , and  $-500.5$  by selecting  $C = 100$  pF; (a) magnitude and (b) phase responses.



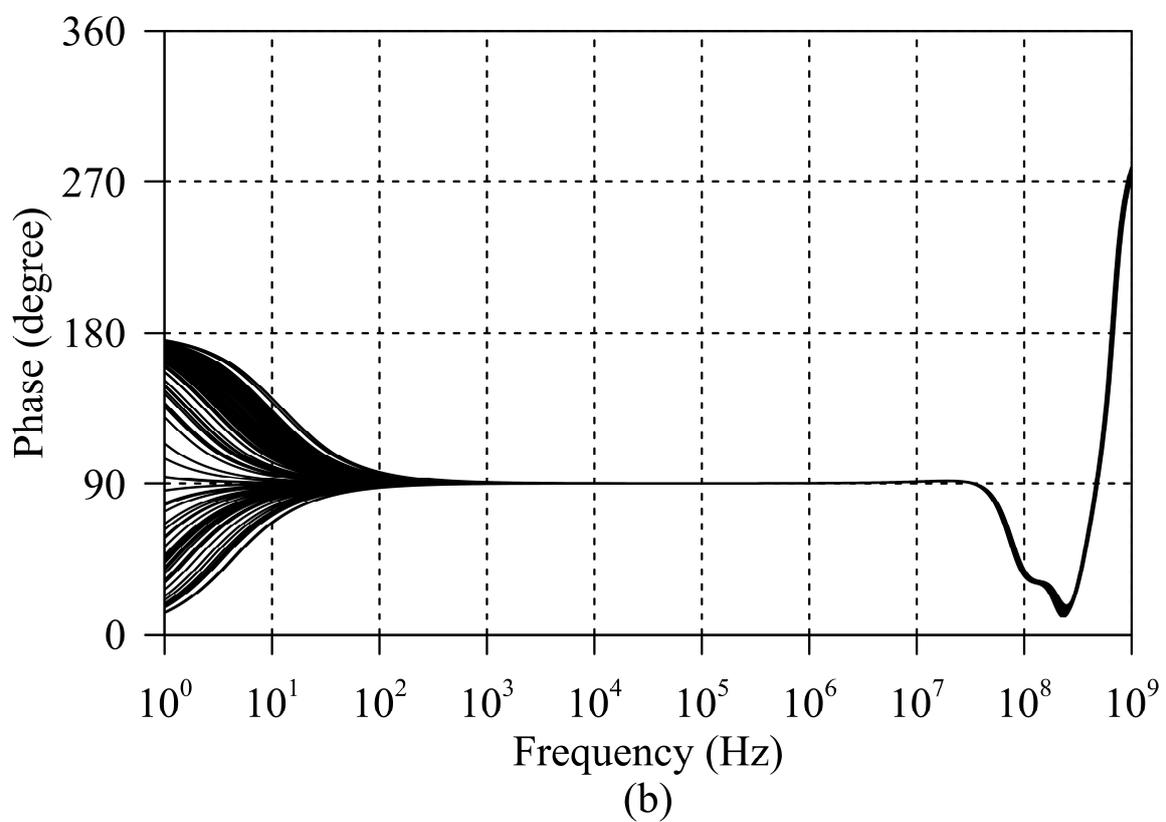
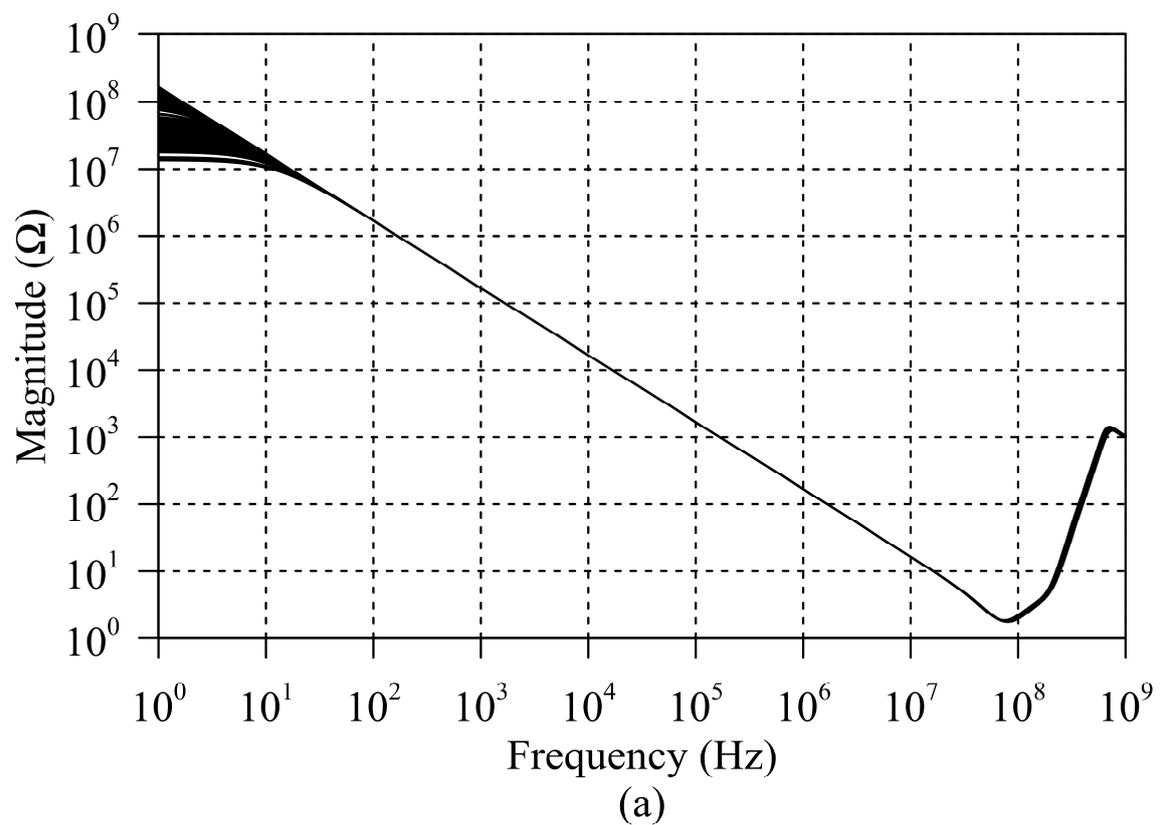
**Figure 9.** Frequency response of the proposed negative lossless GCM and ideal capacitor for  $C_{eq} = -5$ ,  $-50$ , and  $-500$  nF by selecting  $K = 10$ ,  $C_1 = 0.5, 5$ , and  $50$  nF; (a) magnitude and (b) phase responses.



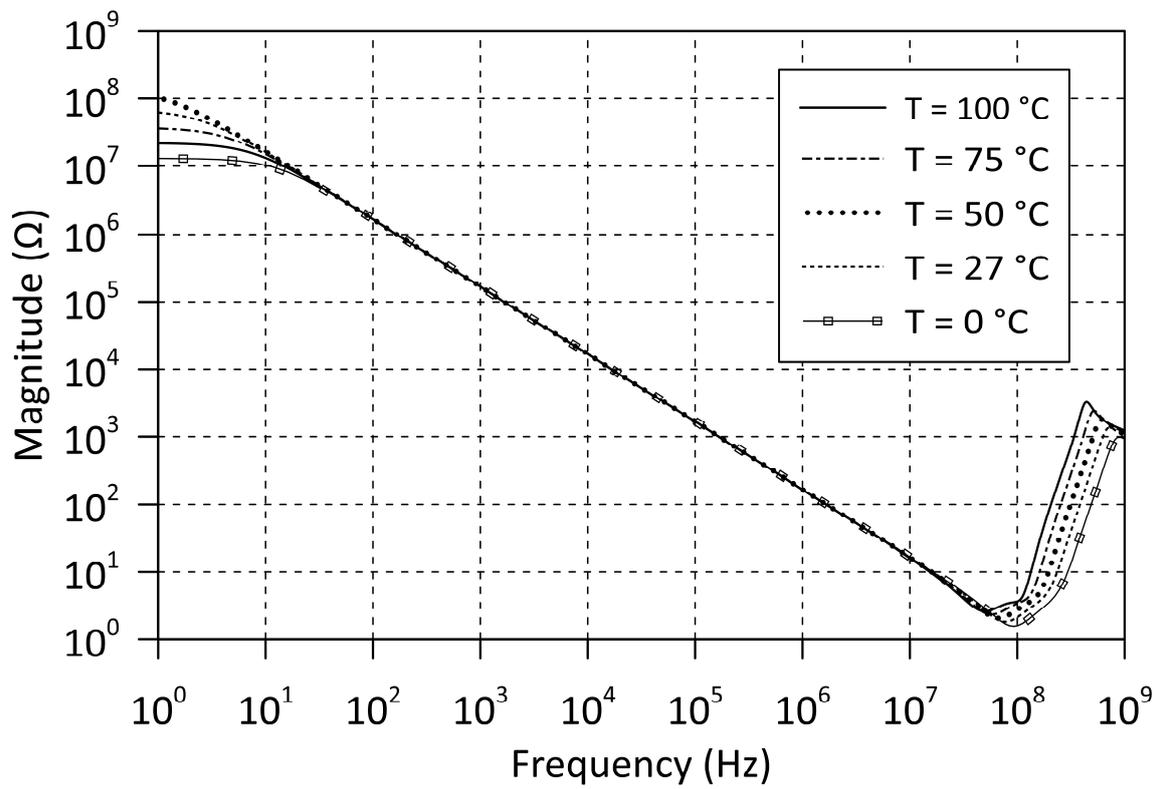
**Figure 10.** Frequency responses of the proposed negative lossless GCM for various supply voltages; (a) magnitude and (b) phase responses.



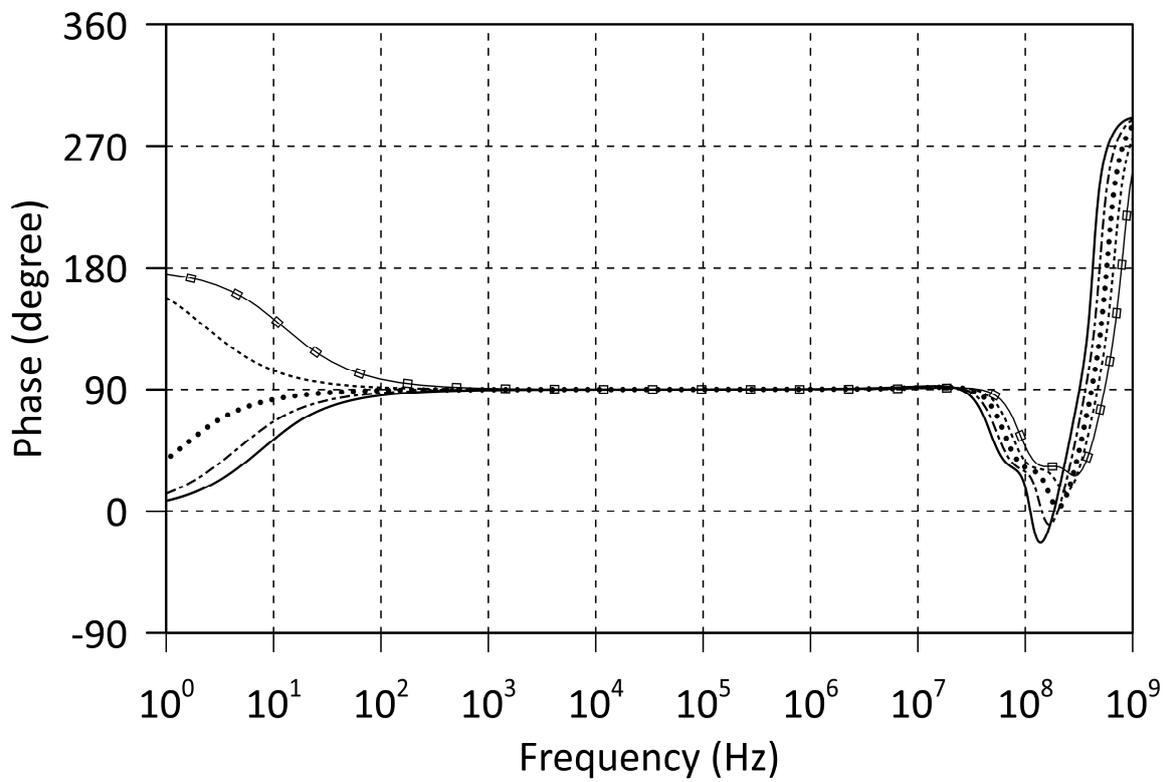
**Figure 11.** Monte Carlo simulation results for 10% variation in the threshold voltages ( $V_{TH}$ ) and gate oxide thickness ( $t_{ox}$ ) of all the MOS transistors; (a) magnitude and (b) phase responses.



**Figure 12.** Monte Carlo simulation results for 5% variation in width of all the MOS transistors; (a) magnitude and (b) phase responses.



(a)



(b)

Figure 13. Temperature analysis for the proposed negative lossless GCM; (a) magnitude and (b) phase responses.

**Table 4.** Comparison of negative CM circuit.

References	# and Type of ABB	# of Resistors		# of Capacitors		Electronic Tuning	Multiplication n Factor	Matching Condition	Technology	Operation Frequency	Power Dissipation
		F	G	F	G						
[19] in Figure 2	2 CFOA	0	2	0	1	No	0.5	No	0.35 $\mu\text{m}$	NA	NA
[19] in Figure 3	2 CFOA	0	2	0	1	No	0.5	No	0.35 $\mu\text{m}$	NA	NA
[19] in Figure 4	1 CFOA	1	1	1	0	No	0.5	No	0.35 $\mu\text{m}$	1 kHz to 5 MHz	NA
[19] in Figure 5	1 CFOA	2	0	0	1	No	0.5	No	0.35 $\mu\text{m}$	NA	NA
[20] in Figure 1	2 CFOA	2	0	1	0	No	NA	No	AD844	NA	NA
[21] in Figure 8	1 CFOA	1	2	0	1	No	NA	Yes	0.13 $\mu\text{m}$	NA	NA
[22] in Figure 11	1 CFOA, 2 OTA	0	0	0	1	Yes	NA	No	AD844, LM13700N	2 Hz to 7 MHz	NA
[23] in Figure 1	1 EVCII–	0	0	1	0	Yes	100	No	0.18 $\mu\text{m}$	80 Hz to 40 kHz	67 nW
[24] in Figure 4	2 VCII+	1	1	1	0	No	50	No	0.35 $\mu\text{m}$	10 MHz	1.5 mW
[25] in Figure 6	2 CFTA	0	2	1	0	Yes	20.3	No	0.13 $\mu\text{m}$	10 kHz to 100 MHz	NA
[25] in Figure 7	2 CFTA	0	2	1	0	Yes	20.3	No	0.13 $\mu\text{m}$	10 kHz to 100 MHz	NA
[26] in Figure 7	1 CFTA	0	1	1	0	Yes	10	No	0.18 $\mu\text{m}$	280 Hz to 4.15 MHz	NA
[27] in Figure 2	1 VCII $\pm$ , 1 E-DVCC	0	0	0	1	Yes	25.4	No	0.18 $\mu\text{m}$	10 kHz to 1 MHz	3.184 mW
[28] in Figure 2	1 OTRA, 1 VF	3	0	1	0	Yes	99	Yes	0.18 $\mu\text{m}$	100 Hz to 1 MHz	NA
[29] in Figure 1	1 VDTA	0	1	1	0	Yes	20	No	0.18 $\mu\text{m}$	100 Hz to 100 MHz	0.89 mW
[30] in Figure 1	1 CFOA	3	0	1	0	No	26	No	AD844	1 kHz to 100 kHz	NA
[31] in Figure 2	1 CFOA	2	0	0	1	No	2001	No	AD844	4 kHz to 1 MHz	NA
[31] in Figure 2	1 CFOA	2	0	0	1	Yes	201	No	AD844	4 kHz to 1 MHz	NA
[31] in Figure 2	1 CFOA	2	0	0	1	No	400	No	AD844	4 kHz to 1 MHz	NA
<b>Proposed</b>	<b>1 CFOA</b>	<b>2</b>	<b>2</b>	<b>0</b>	<b>1</b>	<b>Yes</b>	<b>500.5</b>	<b>Yes</b>	<b>0.13 <math>\mu\text{m}</math></b>	<b>8 Hz to 80 MHz</b>	<b>1.6 mW</b>

Abbreviations: ABB: active building block; CFOA: current feedback operational amplifier; CFTA: current follower transconductance amplifier; E-DVCC: electronically tunable differential voltage current conveyor; F: floating; G: grounded; NA: not available; OTA: operational transconductance amplifier; VCII: second generation voltage conveyor; VF: voltage follower.

### 5. Application Example

This section presents an application example to demonstrate the robustness and workability of the proposed GCM. The application example shown in Figure 14 is the capacitive cancellation circuit in which the parasitic capacitors in the output circuits are eliminated. Here, the negative capacitor ( $C_{eq}$ ) is obtained with the proposed negative lossless GCM. The resistance currents  $I_{R_a}$  and  $I_{R_b}$  in the circuit are given below. If the condition  $C_{eq} = -C_c$  is satisfied,  $I_{R_a}$  and  $I_{R_b}$  will be equal.

$$I_{R_a} = \frac{1 + s(C_c + C_{eq})R_b}{R_a + R_b + s(C_c + C_{eq})R_aR_b} V_s \tag{35}$$

$$I_{R_b} = \frac{1}{R_a + R_b + s(C_c + C_{eq})R_aR_b} V_s \tag{36}$$

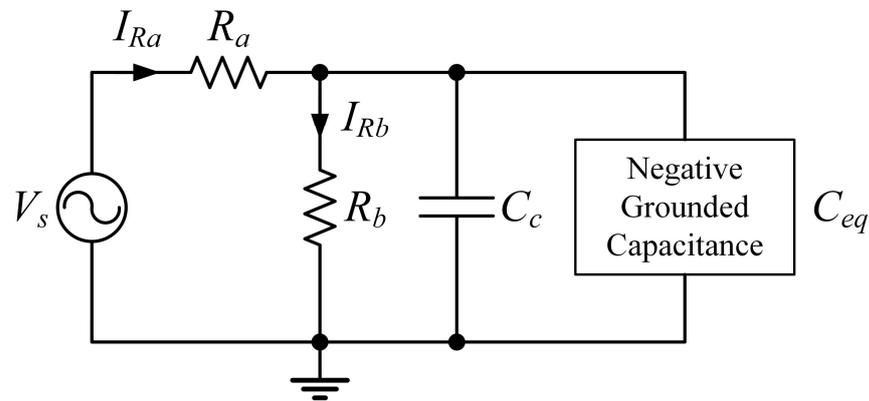


Figure 14. The capacitance cancellation circuit [8,19].

The simulation result was obtained by choosing  $R_a = R_b = 1 \text{ k}\Omega$  and  $C_c = 0.5 \text{ nF}$ . The proposed negative GCM is designed to have  $C_{eq} = -0.5 \text{ nF}$  in the circuit by choosing  $K = 10$  and  $C = 50 \text{ pF}$ . The frequency performance of the capacitance cancellation circuit, for the output current  $I_{R_b}$ , is given in Figure 15. According to the results, the circuit is compatible with ideal results up to 10 MHz.

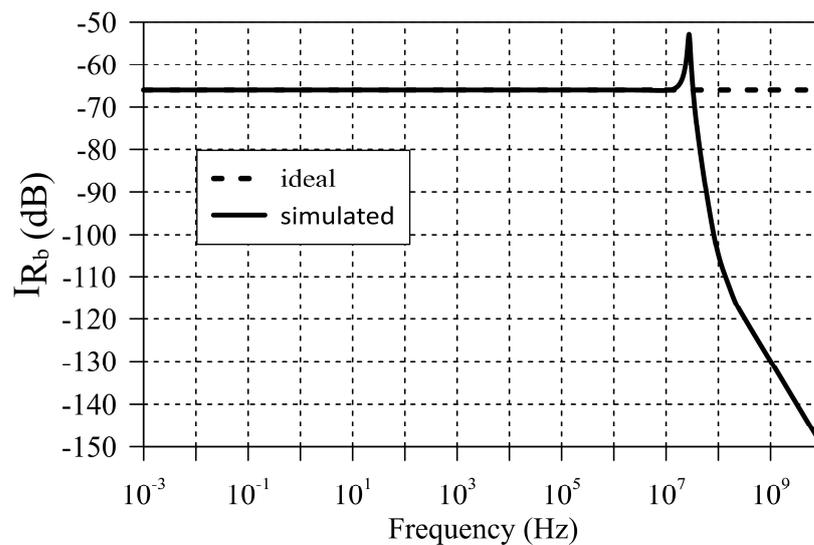


Figure 15. Frequency performance of the capacitance cancellation circuit.

A sinusoidal waveform of 300 mV amplitude and 100 kHz frequency was applied to the input of the circuit. Waveforms of  $I_{R_a}$  and  $I_{R_b}$  currents are given in Figure 16.

The current waveforms have the same amplitude and phase, indicating that the parasitic capacitance is eliminated in the proposed circuit.

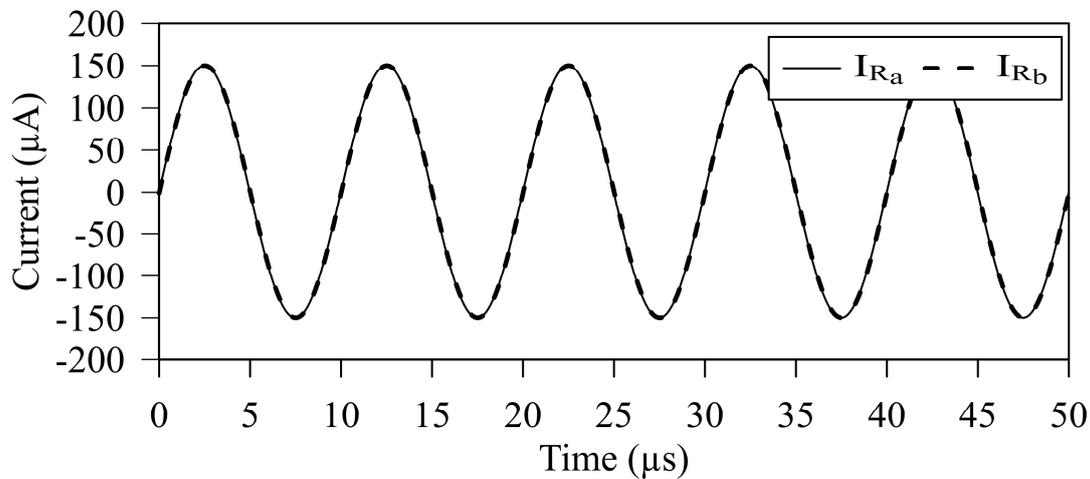


Figure 16. The current waveforms of  $I_{R_a}$  and  $I_{R_b}$  for the circuit in Figure 14.

### 6. Experimental Study

An experimental setup has been designed with the commercially available AD844 ICs to verify the operation of the proposed negative lossless GCM. The capacitance cancellation circuit is shown in Figure 17. Supply voltages of  $\pm 15$  V were selected. The experimental results have been obtained out by selecting  $R_a = R_b = 1$  k $\Omega$  and  $C_c = 1$  nF. By choosing the passive components of the proposed GCM to eliminate the parasitic capacitor,  $C_c = 1$  nF,  $R_1 = 10$  k $\Omega$ ,  $R_2 = 10$  k $\Omega$ ,  $R_3 = 100$   $\Omega$ ,  $R_4 = 1$  k $\Omega$  and  $C = 100$  pF,  $K = -10$  and  $C_{eq} = -1$  nF were obtained. A sinusoidal input voltage ( $V_x$ ) with an amplitude of 2 V at frequencies of 1 kHz, 10 kHz and 100 kHz was applied to the input of the circuit. The input voltage ( $V_x$ ) and the voltage waveforms of the compensated capacitor ( $V_y$ ) are shown in Figures 18–20. According to the test results, it can be seen that the voltages  $V_x$  and  $V_y$  are approximately in the same phase. The phase difference between the voltages was measured as  $2.2^\circ$  at most. As a result, the effect of the parasitic capacitor  $C_c$  is compensated for by the proposed GCM. Since the resistances  $R_a$  and  $R_b$  are chosen to be equal, the circuit works as a voltage divider and the voltage  $V_y$  is approximately half of the voltage  $V_x$ .

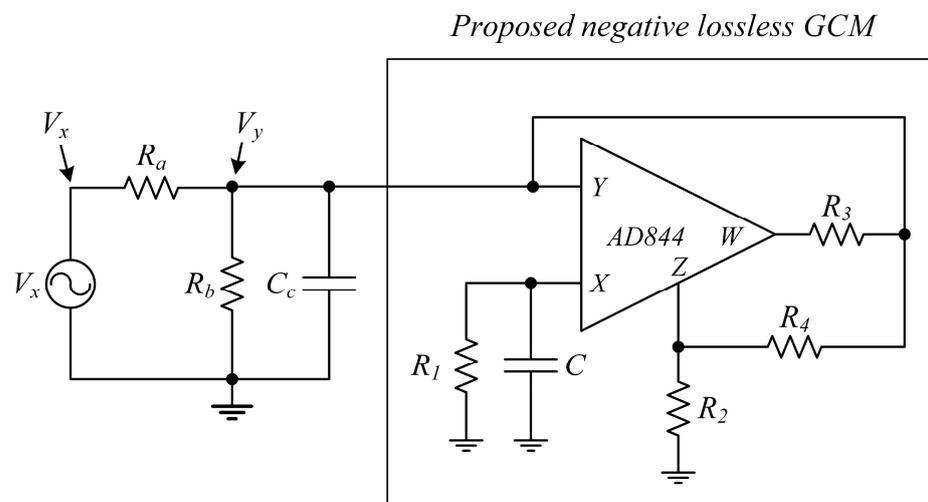


Figure 17. Experimental setup.

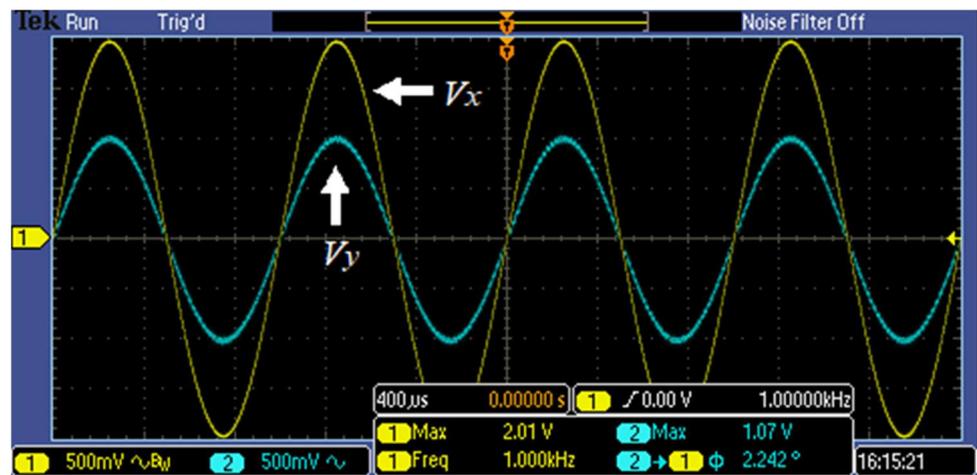


Figure 18.  $V_x$  and  $V_y$  voltage waveforms at  $f = 1$  kHz.

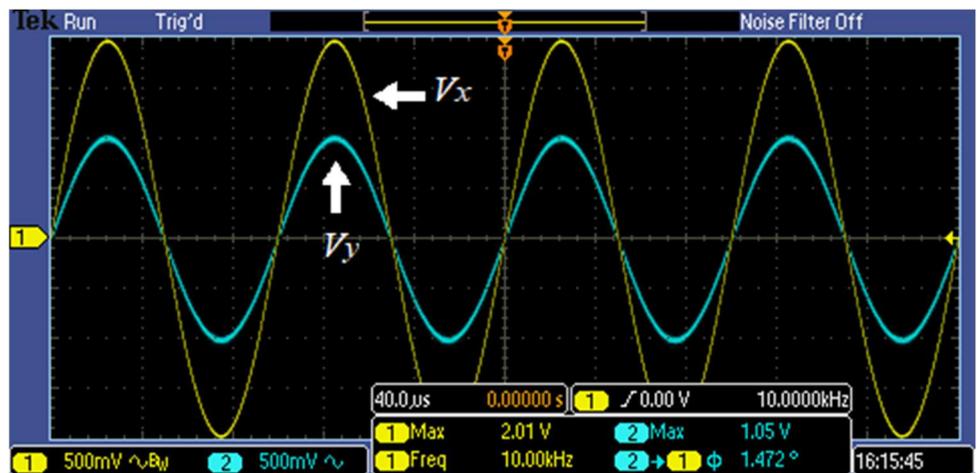


Figure 19.  $V_x$  and  $V_y$  voltage waveforms at  $f = 10$  kHz.

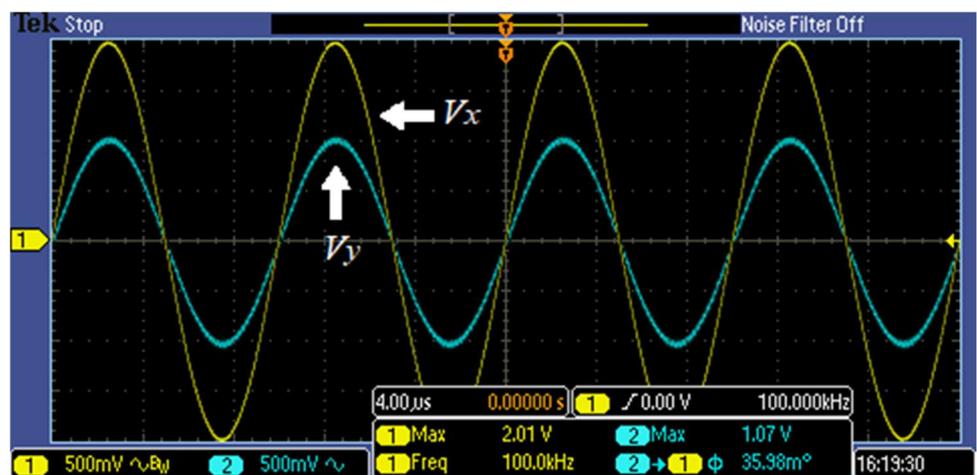


Figure 20.  $V_x$  and  $V_y$  voltage waveforms at  $f = 100$  kHz.

## 7. Conclusions

In this study, a new circuit configuration was introduced to realize the negative lossless GCM. The proposed circuit contains a single CFOA, four resistors, and a grounded capacitor. A detailed analysis of the circuit has been carried out. The factors affecting

the frequency range have been investigated through mathematical analyses. In order to reduce the power consumption of the circuit, a CFOA was obtained by using DTMOS transistors. The simulation results were obtained with the SPICE program using 0.13  $\mu\text{m}$  IBM CMOS technology parameters. The total power consumption of the circuit was 1.6 mW. The workability of the circuit has been shown by providing a capacitive cancellation circuit application and an experimental study.

**Author Contributions:** Conceptualization of this manuscript was by M.V.; the methodology by M.V., E.Ö. and F.K.; software verifications in SPICE by M.V.; validation by M.V., E.Ö. and F.K.; formal checking of the analysis by E.Ö. and F.K.; investigation by M.V.; resources by M.V., E.Ö. and F.K.; data curation by M.V.; writing—original draft preparation by M.V.; writing—review and editing by M.V., E.Ö. and F.K.; visualization by M.V.; supervision by E.Ö. and F.K.; project administration by M.V., E.Ö. and F.K. All authors have read and agreed to the published version of the manuscript.

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