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# Input Voltage-Level Driven Split-Input Inverter Level Shifter for Nanoscale Applications

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**Abstract:** A level shifter (LS) appears to be highly efficient and effective in solving voltage contentions between deep sub-threshold and core voltage levels. An input voltage-level driven split-input inverter that can create common unconnected PMOS and NMOS transistors for the input inverter is proposed, which is powered and used at the input stage to achieve maximum conversion efficiency. Layout and simulation results across different corners have demonstrated that the proposed LS is highly useful for cutting-edge nanoscale applications. It can up-convert voltage from 0.2 V to 1.2 V and down-convert from 1.2 V to 0.2 V @ 1 MHz input pulse, with a level-up or level-down mean switching delay of 1.3 ns, and a power of 9.5 nW. Moreover, the LS occupies an area of 8 $\mu m^2$, which is a reasonably compact size compared to the typical LS designs. Overall, the proposed voltage LS design is an efficient and effective solution that could have an ample range of applications in IoT and biomedical, wireless sensor networks.

**Keywords:** propagation delay; power consumption; voltage-level driven-input inverter; Internet of Things (IoT); System-on-Chip (SoC)



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## 1. Introduction

Portable devices, such as cell phones, computers, laptops, and various sophisticated electronic devices, are very popular with a variety of applications. The demand for hand-held devices has led to numerous reductions in the size of devices, their weight, and the recharge intervals of these devices. Designing for lower power is the essential element for lighter and longer-lasting batteries. Thus, power reduction is the most essential design issue that today's VLSI design engineers must face when dealing with the design of integrated circuits. Supply voltage scaling can be the most efficient method of reducing the dynamic power of switching because both the voltage of supply and its voltage fluctuation are decreased by reducing the supply voltage, leading to a quadratic decrease in dynamic power, whereas the speed decreases [1–3].

Integrated System-on-Chip (SoC) architectures are a composition of dissimilar blocks of intellectual property (IP) cores that operate at different levels of input voltage to meet the required time-related criteria [4–6]. Non-critical blocks consume less energy by operating at lower supply voltages (VDDL), sometimes in the sub-threshold region, while time-critical blocks require higher supply voltages (VDDH) to achieve the desired performance [7–9]. To ensure proper interaction between different voltage domains/cores, reliable LS circuits are necessary to maintain the signal integrity of the design, as depicted in Figure 1.

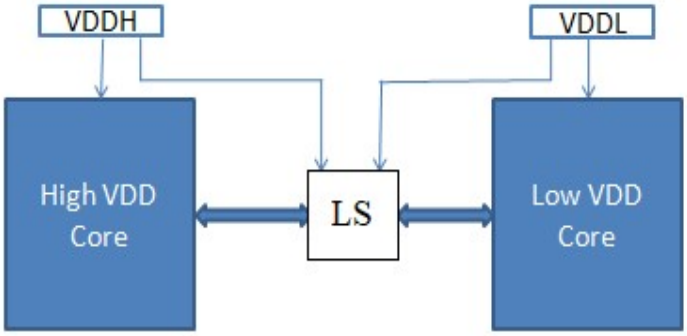


**Figure 1.** Level shifter position.

Current state-of-the-art LSs are categorized into two types: circuit topologies using cross coupled (CC) and current mirror (CM) techniques. While LSs that utilize CC techniques (Figure 2) have less standby power consumption, they are limited by a trade-off between their pull-up and pull-down networks, which affects their speed and energy consumption during switching. LSs face a challenge when up-converting sub-threshold voltages, as it causes the pull-down network areas to be too large and complex in practice [10–13].

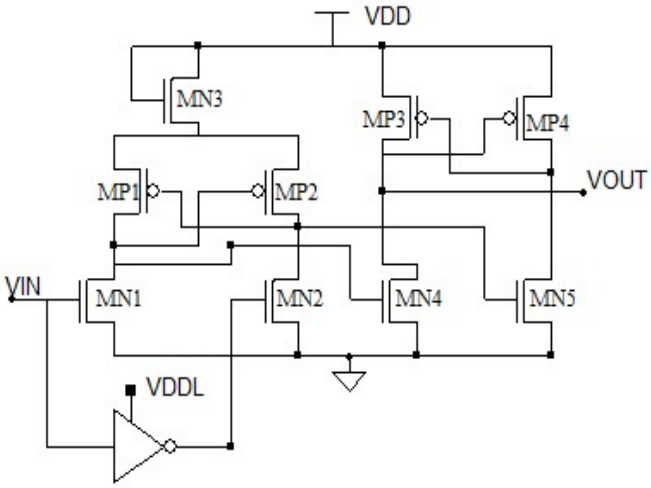


**Figure 2.** Cross coupled LS.

Current-mirror-based architectures [7,10,14] perform better when a wide range of up-conversion is required, as they face more contention among pull-up and pull-down networks, which results in increased speed and reduced energy consumption. However, they tend to consume more static power. To overcome the limitations of cross-coupled and current-mirror-based topologies, recent studies have presented several options. For example, adaptive/regulated pull-up networks have been recommended in some studies to reduce current contention in cross-coupled-based systems and improve energy efficiency.

An improved Wilson current mirror that utilizes mixed-threshold voltage devices has also been reported to address issues with conventional current-mirror-based LSs. In order to achieve even greater energy efficiency, the output stage of an inverting buffer includes a split-input configuration, which is employed in conjunction with an improved Wilson CM that uses mixed-threshold voltage devices [7,15–19].

This study introduces a new short circuit aware inverter that can create common unconnected PMOS and NMOS for a split-input inverter LS design that has been validated through layout and simulation measurements, which the authors believe to be the first of its kind. The designed circuit was laid out using 65 nm CMOS and tested on five different PVT corners. Section 2 of the paper outlines the split-input inverter level shifter (SILS), which

is then assessed based on measurement results in Section 3. Conclusions are presented in Section 4.

## 2. Proposed Input Voltage-Level Driven Split-Input Inverter Level Shifter

Figure 3 shows the invented input voltage-level driven-input inverter level shifter design, which is based on a short-circuit-aware inverter that can create common unconnected PMOS and NMOS for the "split-input inverting buffer LS" design. Unlike previous designs, the circuit utilizes a split-input inverting buffer (MP2-MN2) to reduce power consumption. However, the output stage driving method is unique and involves a boosting inverter and additional feedback connected to MN4-MP4. The split inverter MP2-MN2 eliminates the short circuit when VIN is equal to VDDL. The boosting inverter MP3-MN3 ensures the full swing at VOUT for both logic 0 and 1. The W/L ratio of NMOS is 1:1 and PMOS is 3:1,which are maintained at the level shifting stage, and 4:1 for MP1 and 2:1 for MN1 at the $2 \times 1$ multiplexer stage at the 65 nm techno logy node.

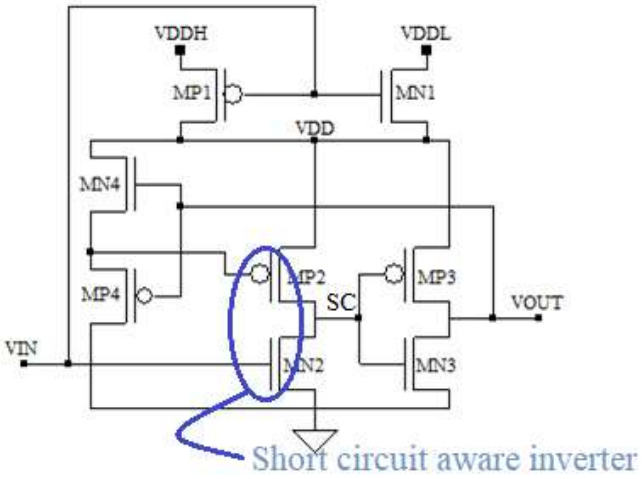


**Figure 3.** Proposed SILS.

The proposed SILS design is different from other solutions presented in previous studies. Compared to previous designs, this split-input inverter enables the proposed design features and a larger voltage differential. This results in a reduction in the short circuit power of the driving stage and improved energy efficiency during both VDDL to VDDH and VDDH to VDDL transitions, particularly for up-conversion from the sub-threshold region. Figure 5 demonstrates the transitory behavior of SILS as the input pulse amplitude voltage is up-converted from 0.2 V to 1.2 V for output transitions.

$$\begin{aligned} V_{SC}(t) = 0.5\left[\frac{\tau G_{mMP2}}{C_L}(\mathrm{VDDH} - |V_{thMP2}|) - \frac{\tau I_{MP2}}{C_L}|V_{thMP2}|\right]e^{\frac{t}{\tau}} + \\ 0.5\left[\frac{\tau G_{mMN2}}{C_L}(\mathrm{VDDH} - |V_{thMN2}|) - \frac{\tau I_{MN2}}{C_L}|V_{thMN2}|\right]e^{\frac{t}{\tau}} + \\ (\mathrm{VDDH} - |V_{thMN2}|) \ \ When \ \mathrm{VIN} > \mathrm{VDDL} \end{aligned} \quad (1)$$

where $V_{SC}$ is the voltage at node SC, $G_{mMP2}$ is the transconductance of the MP2, $G_{mMN2}$ is the transconductance of the MN2, $V_{thMP2}$ is the nominal $V_t$ of the MP2, $V_{thMN2}$ is the nominal $V_t$ of the MN2, $C_L$ is the total capacitances of the VOUT and gate capacitance of MP3-MN3, and $I_{MP2}$ and $I_{MN2}$ represent the currents of MP2 and MN2, respectively. Voltage at node $V_{SC}$ is a function of rise time and fall time, which will be negligible as the inverter creates common unconnected PMOS and NMOS transistors. In Figure 3, a short circuit aware inverter is shown in a circuit comprising MP3 and MN3 devices, which are never simultaneously ON or OFF, and the node voltage at SC is influenced by Equation (1) when the VIN is equal to VDDL. When the VIN is less than or equal to VDDH, the level transition of $V_{SC}$ involves the supply level rails from VDDH to VSS. Therefore, due to a

considerable fall time, VOUT reaches 0. The difference between the first-order and second-order terms leads to a fractional value and means the node voltage SC is stronger than zero, and the driving inverter produces VDDL equal to VOUT as per the mathematical model in Equation (2).

$$\mathrm{V_{SC}(t)} = 0.5\left[\frac{\tau G_{mMP2}}{C_L}(\mathrm{VDDH} - |V_{thMP2}|) - \frac{\tau I_{MN2}}{C_L}|V_{thMN2}|\right] When\ \mathrm{VIN} \leq \mathrm{VDDH} \quad (2)$$

When the VIN is equal to VDDL, MP1 turns ON, which will make VDDH available at VDD. LS acts as a level up-converter, and MN2 ON and MP2 OFF and node voltage SC cause the pull-down and driving inverter (MP3-MN3) to produce a strong VOUT (VDDH). The feedback path ensures MP2 OFF, and when the VIN is equal to VDDH, MN1 turns ON, which will make VDDL available at VDD. LS acts as a level down-converter, and MN2 ON and MP2 OFF and node voltage SC cause the pull-down and driving inverter (MP3-MN3) to produce a strong VOUT (VDDL). The feedback path ensures MP2 OFF, and when the input signal VIN is equal to VSS, MP1 turns ON, which will make VDDH available at VDD. MN2 OFF and MP2 ON and node voltage SC cause the pull-up and driving inverter (MP3-MN3) to produce a strong VSS. The performance of SILS is depicted in the measurements and results sections.

The current flowing through the MP2-MN2 branch is low for both VDDL and VDDH inputs, indicating that the node SC is either VDD or VSS when fully charged, and it triggers the MP3 or MN3 to switch ON or OFF. The activation of MP1 and the reduction in conflict at the SC node cause the SC node to rise and turn on MN3, the MN3 component can be turned OFF by fully discharging the SC to 0 V. From Figure 2, the proposed LS is used during the conversion of the input signal from high to low. To charge the SC and discharge the VOUT node to VSS, the charging current $\mathrm{I_{RISE}}$ is mirrored as $\mathrm{I_{FALL}}$ and the sum of $C_L$ with the rate of change of VOUT. Consequently, the rise and fall times of VOUT are made to be symmetrical, as shown in (3). The specifications of the proposed SILS are compared in the results and discussion sections.

$$\mathrm{I_{RISE}} = \mathrm{I_{FALL}} + C_L \frac{d}{\mathrm{dt}}\mathrm{VOUT} \quad (3)$$

To enhance the switching performance and ensure a small area and low VDDL robustness, a dual $\mathrm{V_{TH}}$ design technique was utilized along with appropriate transistor scaling. Specifically, LVT devices were used for MN3-MN4, while RVT devices were employed for the remaining transistors. An important point to consider is that the voltage shifting range of the SILS can be extreme between VDDL and VDDH. Figure 4 depicts the proposed LS layout. The LS design utilized only two metal wires.

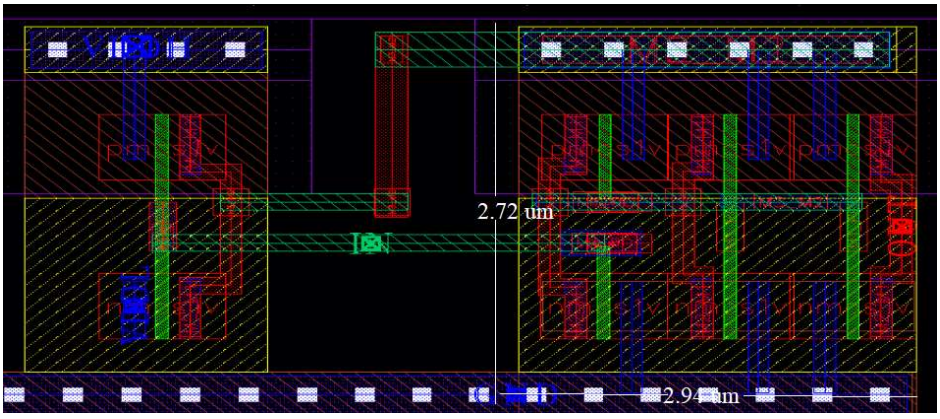


**Figure 4.** Layout of SILS.

The layout comprises metal layers, an n wire, and p-wires with the adaptive biasing system for a split-input inverter with 2.72 μm × 2.94 μm implementations, and it needs approximately the same space in length and width as CMOS devices. It is apparent that the layouts in the size of the MP2 transistor are the largest because it covers nearly one half of the area of MN1. Its size is rather small in comparison to the available LS, and it becomes negligible in large arrays of the LS interface. The resulting LS occupies approximately an 8 $\mu m^2$ area.

The transient waveforms of SILS for 0.2 V and 1.2 V for VDDL and VDDH, respectively, are depicted in Figure 5. A short-circuit-aware inverter that can create common unconnected PMOS and NMOS for the split-input inverter buffer LS is utilized to decrease the short circuit current during VDDL to VDDH and VDDH to VDDL transitions. The voltage variation between VDDL and VDDH nodes ensures the required impedance of the pull-up and pull-down of the MN2 and MP2 inverter, allowing for it to be turned on at extreme levels of VDDLs, thereby reducing the short circuit current and reducing the power of SILS. As mentioned in Figure 3, by adding up MP1, MN1 results in a 2 × 1 multiplexer that enables the LS to be an up shifter or a down shifter, suitable for a sub-threshold and super threshold LS circuit, where VDDL is lower than the $V_t$ of the MOSFET. Figure 5 illustrates the VDDL-to-VDDH switching characteristics where VDDH is 1.2 V and VDDL is set at 0.2 V. The $I_{RISE}$ and $I_{FALL}$ are produced alternately, in contrast with logic mismatches. The proposed SILS have no contention between VDDL and VDDH level shifting.

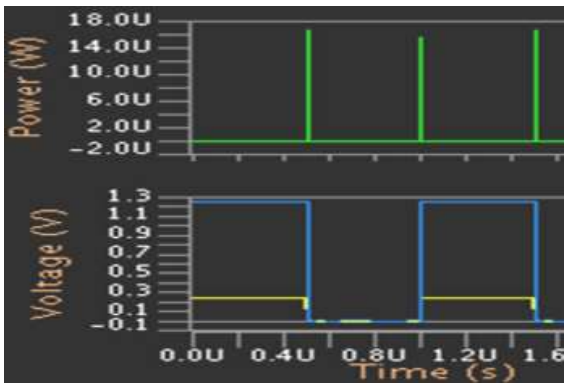


**Figure 5.** Functional output of SILS.

## 3. Measurement and Results

### *3.1. Power and Delay as Functions of VDDL*

Figures 6 and 7 show the relationship between the measured average power and delay for different VDDLs while up shifting, as it shifts voltage from 0.2 V to 1.2 V @ 1 MHz and the SILS temperature is at 27 °C. Power consumption is a crucial parameter to be taken into consideration. The power consumption that was measured for the SILS circuit is illustrated in Figure 6. The amount of power consumed depends on the intensity of the input signal. In addition, the input side inverter which is supplied via VDDH takes up the majority of the power. VDDL is connected only directly to an input converter when the input is at VDDH. The maximum power consumption variation is observed when the VIN is in the range of 0.175 V to 0.2 V. The smallest power utilization variation happens when the circuit transforms the input signal from VDDH to VDDL. The SILS power consumption is almost uniform for all VDDLs from 0.2 V to 0.375 V, and between 0.175 V and 0.2 V, there is a significant reduction in power due to the super threshold region of the MN2 operation. Due to the self-biasing of MP2-MN2, as VDDL increases, the SILS power is stable due to the feedback-driven MN4-MP4 arrangement, resulting in the significant difference in impedances among MP2-MN2. Taken as a whole, the results in terms of power and energy of each transition of the SILS show that it is suitable for all nanoscale applications aimed at moderate to high energy savings.

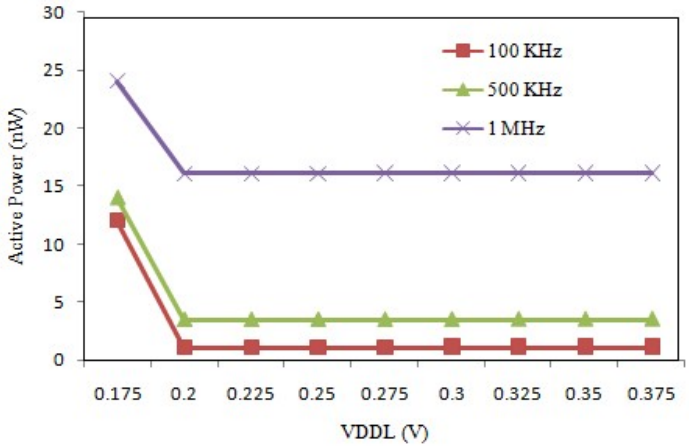


**Figure 6.** Average power of SILS @ VDDL at VDDH = 1.2 V.

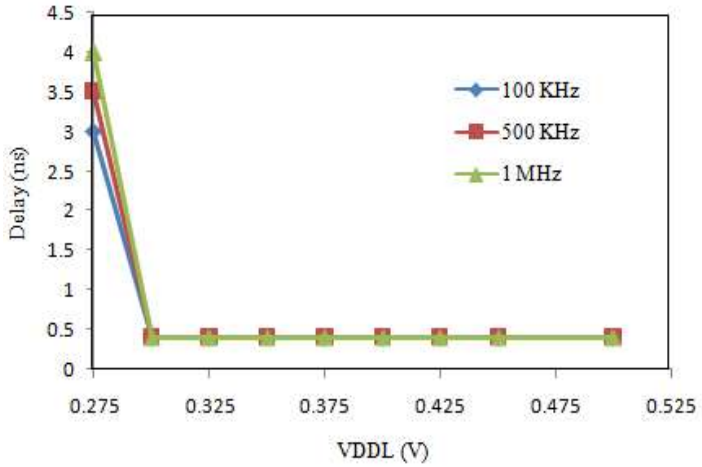


**Figure 7.** Delay of SILS @ VDDL at VDDH = 1.2 V.

The delay of SILS in relation to VDDL with a fixed VDDH of 1.2 V, as well as when using fem to farad capacitive load, is displayed in Figure 7. A delay when VDDL to VDDH transition, while VDDL < 0.3 V, is more because of the larger shifting gain of SILS when it is converting to 1.2 V. The delay variant curve, especially the rising delay, is approximately flat for VDDL > 0.3 V. The variations that have been measured for the rising delay at VDDH are fixed at 1.2 V, whereas an IC in the circuit is used to load the split-input inverter circuit. In this diagram, it is shown that the delay is measured as the SILS converts a pulse-shaped signal that has a 0.2 V and 1.2 V amplitude. In Figure 7, it is evident that the delay of the circuit is nearly flat from 0.3 V onwards. The SILS delay is uniform for all VDDLs from 0.3 V to 0.5 V, influenced by the self-biasing of MP2-MN2. As VDDL rises from 0.275 V to 0.3 V, the SILS delay decreases due to overcoming the super threshold region of the operation. Overall results in terms of delay show that the proposed SILS is suitable for all nanoscale applications.

### *3.2. Power and Delay as Functions of VDDH*

Figures 8 and 9 show the relationship between the measured average power and delay for different VDDHs while down shifting, as it shifts from 1.2 V to 0.2 V @ 1 MHz and the SILS temperature is at 27 °C. The SILS power consumption is almost uniform for all VDDHs from 0.9 V to 1.1 V, influenced by the (2) and self-biasing of MP2-MN2. As VDDH increases, the SILS power is stable due to the feedback-driven MN4-MP4 arrangement, resulting in the significant difference in impedances among MP2-MN2. The results of power and energy for each transition of the SILS show that it is suitable for all nanoscale

applications aimed at moderate to high energy savings. The amount of power consumed depends on the intensity of the input signal. For the level-up shift, the input inverter is supplied via VDDH, which takes up the majority of the power.

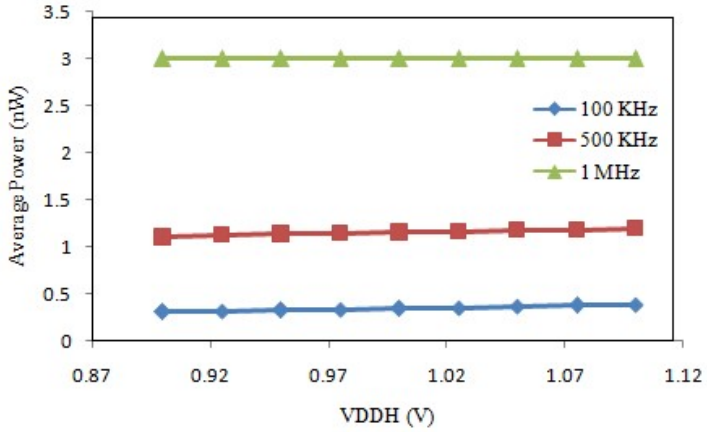


**Figure 8.** Power of SILS @ VDDH at VDDL = 0.2 V.

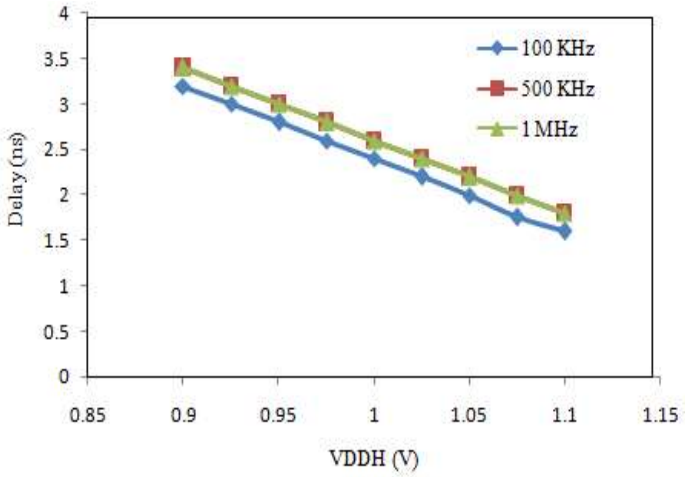


**Figure 9.** Delay of SILS @ VDDH at VDDL = 0.2 V.

The SILS delay decreases uniformly for all VDDHs from 0.9 V to 1.1 V, influenced by the (3) and self-biasing of MP2-MN2. As VDDH increases, the SILS delay decreases due to the feedback-driven MN4-MP4 arrangement, resulting in the significant difference in impedances among MP2-MN2. Overall results in terms of delay of SILS show that it is suitable for all nanoscale applications. The propagation delay for VDDH < 0.9 V is more because of the wider shifting gain of SILS when it is converting VDDH to VDDL of 0.2 V. From the delay variation curve, there is a flat delay for VDDL > 0.3 V. The variations that have been measured for the falling delay at VDDL are fixed at 0.2 V, whereas a split inverter integrated into the circuit is used to load the split-input inverter circuit.

### *3.3. Impact of Load on SILS Performance*

The measured power for a typical sample was recorded for the experiment that was conducted at different load capacitances from 10 fF to 90 fF, and it is illustrated in Figure 10 at VDDL = 0.2 V and VDDH = 1.2 V @ 1 MHz. The maximum power penalty variation of the SILS over the range is just 1.75 times the power at 10 fF while levelling up, and there is no considerable power penalty variation while levelling down, and the power variations of the other LSs are between 30 and 90 times [20–22]. The proposed SILS shows negligible power variations.

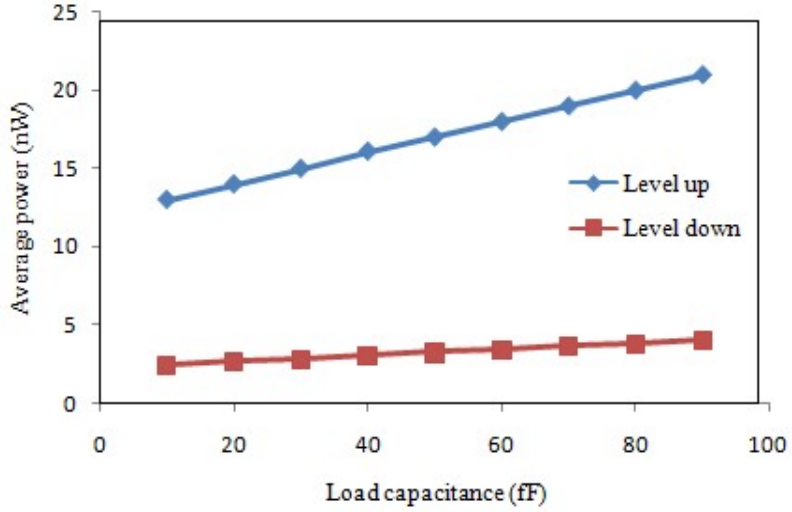


**Figure 10.** Power of SILS @ Load capacitance VDDH = 1.2 V, VDDL = 0.2 V and 1 MHz.

The measured delay for a typical sample was recorded for the experiment that was conducted at different load capacitances from 10 fF to 90 fF, and it is illustrated in Figure 11 at VDDL = 0.2 V and VDDH = 1.2 V @ 1 MHz. The maximum delay penalty variation of the SILS over the range is just 1.8 times the delay at 10 fF while levelling up, and 1.9 times the delay penalty variation while levelling down, and the delay discrepancies of the other LSs are around 25 to 100 times. The proposed SILS shows negligible power variations, which means the robustness of the SILS against load variations is strong.

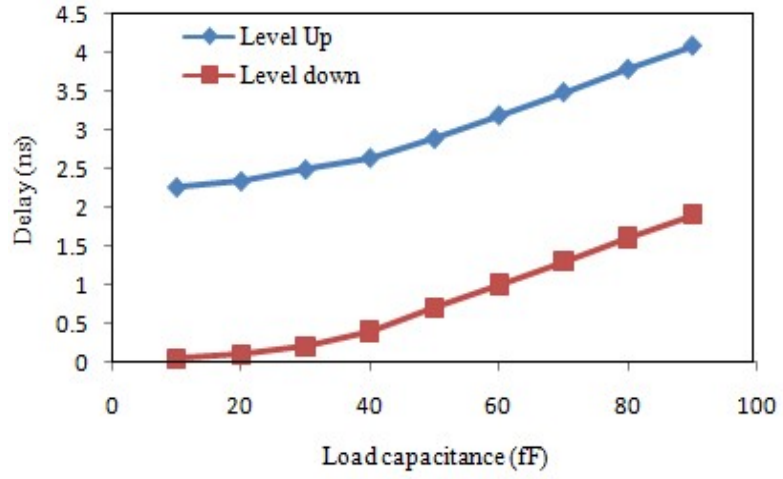


**Figure 11.** Delay of SILS @ Load capacitance VDDH = 1.2, VDDL = 0.2 V and 1 MHz.

The measured minimum VDDL required is 0.19 V for up-conversion to 1.2 V. Among the ten simulation results, the worst-case scenario resulted in a voltage input of 0.19 V at 27 °C. On the other hand, the most efficient sample was able to up-convert a VIN pulse as low as 0.2 V, as illustrated in Figure 5. The performance of the SILS-based structure was found to be very negligibly influenced by the temperature. At lower temperatures, the leakage current flow was reduced, leading to an improvement in the VDDL min value, while at higher temperatures, the VDDL min value deteriorated due to increased leakage current flow. The stable power consumption was determined by considering a VDDL value of 0.2 V and a VDDH value of 1.2 V, while levelling up the static power utilization remained constant at around 1.3 nW, which is 28% of the power for VDDH in the range of 4.65 W.

Two cascaded inverters were employed to buffer the proposed SILS for driving the output at a capacitive load of 50 fF and the test tools, which allowed us to measure the power and delay. Additionally, the output buffering was kept constant in an alternative

"test" path of the circuit to determine each element's separate contribution to the total power and delay. In the scenario where the input pulse voltage equals 0.2 V, the mean delay is practically 0.4 ns, whereas at a VDDH of 1.2 V, it rises to about 1.75 ns when VDDL is at 0.2 V, which is roughly 77% higher. The power drops when VDDL increases, primarily as a result of the short-circuit-aware inverter. The mean energy usage for VDDL = 0.2 V and VDDH = 1.2 V is just 16 fJ. Another major point to assert is how successfully the suggested LS adjusts the performance of the device improving with increasing operating frequency. It can be observed that the outcome was obtained from the layout in the presence of a load capacitance of 50 fF.

### *3.4. Comparison Results and Discussion*

Table 1 shows a comparison of various LS designs based on their performance. The CC-based LS circuit in [3,4] achieves low standby power, which is limited by a trade-off between their pull-up and pull-down, which affects their speed and energy consumption during switching, but consumes a significant amount of energy per transition at 30.7 fJ [3], which is approximately twice that of the proposed SILS. According to [11], the LS approach for the 55 nm CMOS node achieves the lowest energy/transition of 27 fJ and a marginal VDDL of 0.3 V. However, it also has the highest delay of 82 ns. Current-mirror-based architectures perform better when a wide range of up-conversion is required, as they face less contention between pull-up and pull-down, resulting in increased speed and reduced energy consumption. However, they tend to consume more static power [20,21], and the CM-based solution suffers from poor switching performance and a limited shifting range. Compared to other LS designs in 65 nm CMOS, the CM-based LS in [21] is competitive, with a switching delay of 7.5 ns. In comparison to [23], the proposed LS SILS demonstrates in this paper that it offers considerable decrements in power by approximately 25% higher power at the cost of lower VDDL at 0.2 V. This statement implies that in order to achieve a higher level of robustness against process corners, the proposed circuit has a trade-off between power and delay. The comparison in Table 1 shows that the suggested circuit has the minimum up-convertible VDDL and is the most robust among the compared circuits, with a variability of around 10%. It should be noted that the simulation results were taken at different process corners, which may be representative of all possible process variations, but the fact that the suggested circuit outperformed the other circuits despite the inverter type circuit limitation makes the result even more significant. The proposed SILS is robust not only in terms of a wide conversion range, power, and delay, but also in that it has the capability to perform up shift or down shift, unlike other LSs capable of performing only up shift.

**Table 1.** Comparison of LSs.

| Ref./ Proposed | Technology (nm) | Type of Technique | VDDL (V) | VDDH (V) | Power (nW) | Delay (ns) | PDP (fJ) |
|---|---|---|---|---|---|---|---|
| [3] | 65 | CC | 0.3 | 1.2 | 30.7 | 25 | 0.768 |
| [4] | 55 | CC | 0.3 | 1.2 | 23 | 53 | 1.219 |
| [20] | 65 | CM | 0.3 | 1.2 | 552 | 17.5 | 9.660 |
| [11] | 55 | CM | 0.3 | 1.2 | 27 | 82 | 2.214 |
| [21] | 65 | CM | 0.3 | 1.2 | 124 | 7.5 | 0.930 |
| [22] | 55 | CM | 0.45 | 1.2 | 180 | 57 | 10.26 |
| [23] | 65 | DLS | 0.3 | 1.2 | 12 | 186 | 2.230 |
| SILS (Up/Down) | 65 | Inverter | 0.2 | 1.2 | 16 | 0.4 | 0.006 |
| | | | | | 03 | 1.75 | 0.005 |

Where, CC—cross-coupled; CM—current mirror; DLS—dynamic leakage suppression.

The SILS has the least number of MOS devices (see Figure 12). The number of MOS devices needed for the proposed LS is only 08, which is the lowest among all LSs, mainly owing to both level up- or level down-conversion, and which is approximately 25% lower than the transistor used in [20].

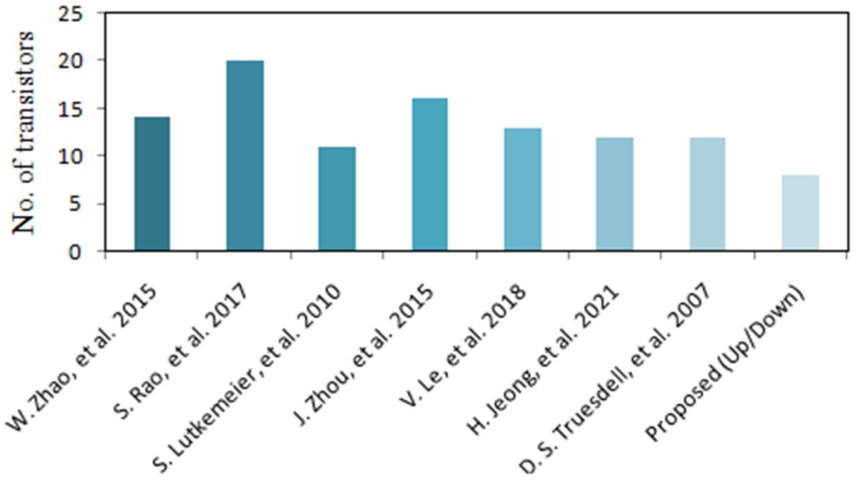


**Figure 12.** No. of transistors in LS [3,4,11,20–23].

Figure 5 illustrates the least possible VDDL of SILS for varying frequencies with a distinctive corner including MOS transistors, 27 °C and VDDH = 1.2 V. It can be seen that by decreasing the frequency of the circuit, the power consumption is decreased, which suggests that either decreases in frequency or decreasing the VDDL to lower than 0.2 V are possible. The minimum value of VDDL can be 0.15 V when the SILS operates at 100 kHz. The delay and power consumption at lower frequency has shown that the minimum possible VDDL can be achieved to meet the needs of IoT and biomedical, wireless sensor network applications. Apparently, the proposed SILS has the lowest PDP and area for up or down voltage-level conversions.

## 4. Conclusions

This study proposes a split-input inverter level shifter that effectively converts sub-threshold voltages to nominal supply voltages. The proposed structure consists of a short-circuit-aware inverter that can create common unconnected PMOS and NMOS transistors and an output inverter that can accelerate the inverter's power delivery to improve switching and energy efficiency. The split-input inverter level shifter was implemented using 65 nm CMOS technology, and we tested the performance for different factors such as voltages, temperatures, and process corners. From the results obtained, it is concluded that the design can convert very low-voltage inputs with an average of 0.2 V under optimistic conditions at 27 °C, and the SILS can produce up to 1.2 V. The proposed circuit demonstrates efficient dynamic power consumption and low latency. It has a remarkable delay of 1.3 ns, coupled with excellent energy efficiency. The energy consumption is also impressive, with an average power of 9.5 nW.

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