electronics

MDPI

Article

Design and Implementation of Single-Phase Grid-Connected Low-Voltage Battery Inverter for Residential Applications

Akekachai Pannawan [1], Tanakorn Kaewchum [1], Chayakarn Saeseiw [2], Piyadanai Pachanapan [2], Marko Hinkkanen [3] and Sakda Somkun [1,*]

[1] School of Renewable Energy and Smart Grid Technology (SGtech), Naresuan University, Phitsanulok 65000, Thailand; akekachaip61@nu.ac.th (A.P.); tanakornka65@nu.ac.th (T.K.)
[2] Department of Electrical and Computer Engineering, Naresuan University, Phitsanulok 65000, Thailand; chayakarns66@nu.ac.th (C.S.); piyadanip@nu.ac.th (P.P.)
[3] School of Electrical Engineering, Aalto University, 02150 Espoo, Finland; marko.hinkkanen@aalto.fi
* Correspondence: sakdaso@nu.ac.th

Abstract: Integrating residential energy storage and solar photovoltaic power generation into low-voltage distribution networks is a pathway to energy self-sufficiency. This paper elaborates on designing and implementing a 3 kW single-phase grid-connected battery inverter to integrate a 51.2-V lithium iron phosphate battery pack with a 220 V 50 Hz grid. The prototyped inverter consists of an *LCL*-filtered voltage source converter (VSC) and a dual active bridge (DAB) DC-DC converter, both operated at a switching frequency of 20 kHz. The VSC adopted a fast DC bus voltage control strategy with a unified current harmonic mitigation. Meanwhile, the DAB DC-DC converter employed a proportional-integral regulator to control the average battery current with a dynamic DC offset mitigation of the medium-frequency transformer's currents embedded in the single-phase shift modulation scheme. The control schemes of the two converters were implemented on a 32-bit TMS320F280049C microcontroller in the same interrupt service routine. This work presents a synchronization technique between the switching signal generation of the two converters and the sampling of analog signals for the control system. The prototyped inverter had an efficiency better than 90% and a total harmonic distortion in the grid current smaller than 1.5% at the battery power of ±1.5 kW.

Keywords: battery storage; DC-DC converter; grid-connected inverter; solar photovoltaic

Citation: Pannawan, A.; Kaewchum, T.; Saeseiw, C.; Pachanapan, P.; Hinkkanen, M.; Somkun, S. Design and Implementation of Single-Phase Grid-Connected Low-Voltage Battery Inverter for Residential Applications. *Electronics* **2024**, *13*, 1014. https://doi.org/10.3390/electronics13061014

Academic Editors: Amedeo Andreotti and Bianca Caiazzo

Received: 8 February 2024
Revised: 1 March 2024
Accepted: 5 March 2024
Published: 7 March 2024

1. Introduction

Reduction of CO_2 emissions has been driving shares of renewable energy in electricity generation systems. Solar photovoltaic (PV) technology has been the fastest-growing renewable energy technology since it can be adopted in small-scale to large-scale power generation systems [1]. Grid-connected PV rooftop systems are commonly installed in the residential sector. However, the excess power from the residential PV rooftop systems poses power quality problems for low-voltage (LV) distribution networks. Voltage violation due to the outfeed of PV power is the most common issue for the LV grid [2]. Extensive upgrades of LV distribution networks for supporting solar PV rooftop systems require a large amount of capital investment. Battery storage is an enabling technology for further deployment of variable renewable energy (VRE) technology. Moreover, integrating battery storage with LV grids reduces transmission congestion, improves power quality, and delays investment in upgrading existing networks [3,4].

Solar PV and battery storage integration into LV distribution networks can be implemented in various topologies. Battery storage can be connected to solar PVs on the DC side of the grid inverter, as depicted in Figure 1. These topologies are so-called DC coupling solar PV-battery hybrid inverters. The DC bus voltage is usually greater than the PV voltage, so non-isolated boost DC-DC converters interface the PV strings with the

DC bus voltage. Maximum power point tracking (MPPT) is embedded with the control system of the boost DC-DC converter [5,6]. A high voltage (HV) battery pack can be directly connected to the DC bus of the grid inverter, as shown in Figure 1a [7]. The battery voltage must be greater than the minimum requirement of the grid inverter, i.e., the peak value of the grid voltage for a single-phase system, and the peak value of the line-line voltage of a three-phase system. An HV battery pack can be connected to the DC bus via a non-isolated DC-DC converter, as shown in Figure 1b. Typically, a bidirectional buck-boost DC-DC converter allows a wide battery voltage range (200–500 V). Meanwhile, the DC bus voltage is regulated above the minimum requirement of the grid-interfaced inverter. A battery back requires an electronic battery management system (BMS) for voltage balancing, management, and protection of the galvanic cells [8]. Thus, HV battery storage with complex BMS may only be viable for some residential systems. Low-voltage battery storage (less than 100 V) with a less complicated and cheaper BMS can be a suitable option for a small household (less than 5 kW), as illustrated in Figure 1c [7]. The LV battery pack is interfaced with the DC bus through a bidirectional isolated DC-DC converter, which employs a medium frequency (MF) (20–150 kHz) transformer for voltage matching the LV battery pack with the DC bus [9,10]. Battery storage can be integrated with the LV network by the AC coupling topologies shown in Figure 2. A grid-interfaced inverter is dedicated to the battery systems of the DC coupling topologies in Figure 1. PV power P_{PV}, battery power P_{Batt}, load power P_L, and grid power P_g are exchanged at the AC point of common coupling (PCC). The AC coupling topologies have a lower efficiency than the DC coupling systems due to an increased conversion stage [11]. However, the AC coupling systems can be employed with existing grid-connected PV inverters or without any PV inverter for energy arbitrage or peak load shaving [7]. AC-coupled two-stage LV battery inverters depicted in Figure 2c are common for small residential applications with a power lower than 5 kW. The power conversion stages can be integrated with the battery pack into a single package [12,13].

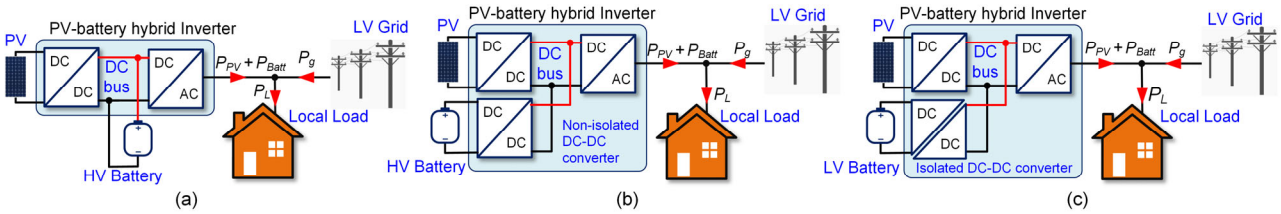

Figure 1. DC coupling grid-connected PV-battery hybrid inverters: (**a**) direct connection of the HV battery to the DC bus; (**b**) HV battery connected to the DC bus via a non-isolated DC-DC converter; (**c**) LV battery connected to the DC bus via an isolated DC-DC converter.

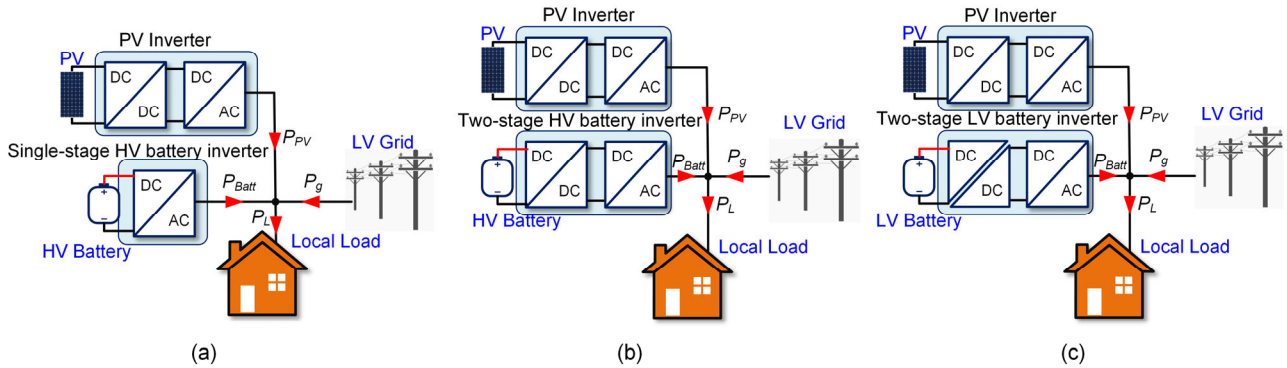

Figure 2. AC coupling grid-connected PV-battery hybrid inverters: (**a**) single-stage HV battery inverter; (**b**) two-stage HV battery inverter; (**c**) two-stage LV battery inverter.

This study focuses on a two-stage single-phase grid-connected LV battery inverter for small residential applications. A dual-active bridge DC-DC converter with phase-shift

modulation strategies is generally employed as the bidirectional isolated DC-DC converter for the LV battery pack. Meanwhile, *LCL*-filtered grid-connected voltage source converters (VSCs) are commonly adopted as the grid-interfaced inverter. However, a limited zero-voltage switching (ZVS) range of the DAB DC-DC converter causes a low efficiency if the voltage ratio between the sides deviates from the nominal value [14]. The efficiency of the DAB DC-DC converter can be enhanced by adding resonant networks to the MF transformer to increase the ZVS range [15,16]. However, power transfer of the resonant DAB DC-DC converter can be controlled by variation of the switching frequency, which is more complicated compared to the fixed frequency operation of the conventional DAB DC-DC converter. The DAB DC-DC converter is sensitive to an imbalance in the voltage-second applied to the MF transformer, which causes a DC offset in the transformer current [17]. The primary and secondary currents of the transformer were sampled 10 times over a switching period to determine the DC offset component, from which the DC offset was compensated through the duty ratios applied to the two active bridges. This method can attenuate the dynamic and static DC offset components [18]. For simplicity, the dynamic DC offset compensation can be embedded into the modulation scheme, where the phase angle of each leg of the DAB DC-DC converter is independently controlled [19,20]. These dynamic DC offset compensation methods require only delay elements.

The bus voltage is controlled through the VSC. The intrinsic double-frequency ripple component in the bus voltage can distort the grid current waveform [21]. A notch filter is usually employed to block the double-frequency ripple component to enter the bus voltage control loop so that the loop bandwidth can be increased with reduced bus capacitance and a near sinusoidal grid current waveform [22,23]. However, low-frequency harmonic components in the grid voltage and VSC terminal caused by the dead time effect can still distort the grid current waveform [24]. Recently, a unified current harmonic mitigation was adopted in a grid-connected VSC [24], which maintained the grid current near sinusoidal with a fast bus voltage control and rejection of voltage harmonic components in the grid and non-ideal switching of the VSC [24].

As mentioned above, the control techniques of the DAB DC-DC converter and grid-connected VSC have been widely presented. However, microcontroller-based implementation techniques of the two converters, with the generation of switching signals and interrupt request and analog signal sampling, have yet to be reported. Thus, this study covers the design and implementation of a single-phase grid-connected low-voltage battery inverter. The battery inverter consists of a DAB DC-DC converter and an *LCL*-filtered VSC thanks to their constant switching frequency application, which eases the implementation of the control system. The control systems of the two converters were implemented in the same microcontroller within the same interrupt service routine (ISR). Synchronous operations of the switching signal generation for the VSC and DAB DC-DC converter and sampling analog signals are highlighted. This work also presents a battery current control strategy with a dynamic DC offset mitigation of the MF transformer. Experimental validation of the proposed inverter is presented.

2. System Description

The main objective of this study is to design a 3 kW bidirectional inverter for interfacing a 16-cell lithium iron phosphate (LFP) battery pack with a single-phase 220 V 50 Hz grid for residential energy storage applications. Figure 3 shows the inverter topology in this study. The grid voltage $v_g(t)$ is converted to a 400 V DC voltage $v_D(t)$ through an *LCL*-filtered VSC. A DAB DC-DC converter well suits the second-stage battery converter as the voltage matching and galvanic isolation are achieved via the MF transformer. Moreover, if properly designed, the DAB DC-DC converter exhibits high efficiency thanks to the ZVS operation [14]. The VSC adopts the cascade control structure with the bus voltage control as the outer loop and the grid current control as the inner loop. The VSC can inject reactive power through the reference current $i_q^*(t)$ for grid support functionality. The inverse Park transformation phase-locked loop (PLL) [25] provides the estimated angle θ of

the grid voltage for synchronization with the grid. The battery current $i_B(t)$ is regulated by a proportional-integral (PI) controller with the reference phase difference δ^* between the primary and secondary voltages $v_p(t)$ and $v_s(t)$ of the transformer, which are generated by the LV and HV bridges with the single-phase shift (SPS) modulation. The DC offset mitigation technique for the transformer currents $i_p(t)$ and $i_s(t)$ is implemented with the SPS modulation. The series inductor L_a limits the maximum charge/discharge current [20]. The VSC and the DAB DC-DC converter's control systems and switching signal generation are implemented on a TMS320F280049C 32-bit microcontroller from Texas Instruments (Dallas, TX, USA) [26]. Table 1 summarizes the main specifications of the battery inverter. Note that the winding resistance symbols R_1, R_a, and R_g of the inductors L_1, L_a, and L_g are not illustrated in Figure 1 for simplicity. Table 2 lists the parameters of the battery inverter.

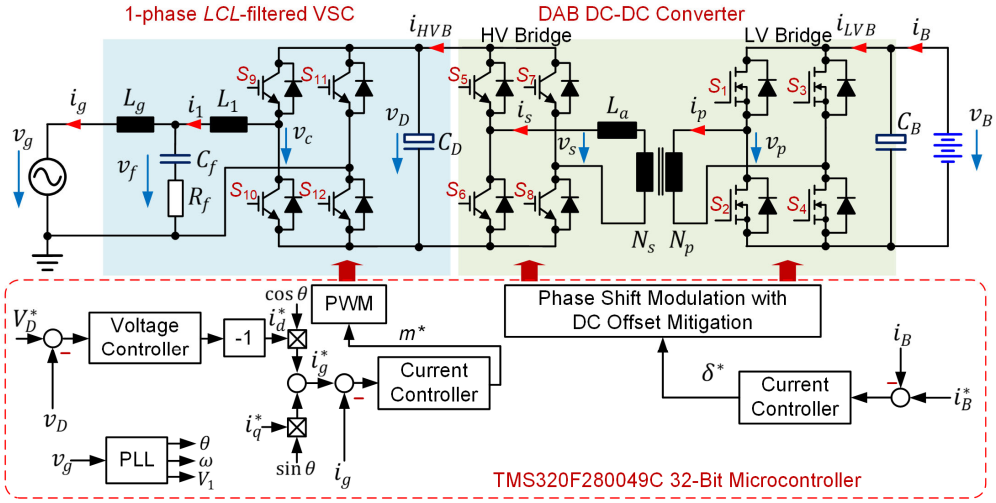

Figure 3. Circuit diagram and its simplified control system of the inverter in this study.

Table 1. Specification of the battery inverter.

Parameters	Value
Maximum grid power	3 kW
Nominal grid voltage	220 Vrms
DC bus voltage	400 V
Nominal grid frequency	50 Hz
Battery nominal voltage, V_{Bn}	51.2 V
Battery voltage range	40–60 V
Maximum battery current	60 A

Table 2. Parameters of the battery inverter.

Parameters	Value
Inductor L_1	0.8 mH
Winding resistance R_1 of L_1	0.07 Ω
Inductor L_2	0.4 mH
Winding resistance R_2 of L_2	0.06 Ω
Filter capacitor C_f	2 μF
Damping resistor R_f	1.1 Ω
DC bus capacitor C_D	800 μF
Series inductor L_a	230 μH
MF transformer's turn ratio N_s/N_p	7.81
Battery-side capacitor C_B	9.9 mF
Switching frequency f_{sw}	20 kHz
Control sampling frequency f_s	20 kHz

3. Implementation of the Grid-Connected VSC

3.1. VSC Modeling

The grid current $i_g(t)$ and bus voltage $v_D(t)$ of the VSC are the controlled variables. Averaging over a switching period T_{sw} yields the governing equations for $i_g(t)$ as follows:

$$L_2\frac{di_g(t)}{dt} + R_2 i_g(t) = v_f(t) - v_g(t)) \tag{1}$$

$$v_f(t) = v_{cf}(t) + R_f\big(i_1(t) - i_g(t)\big) \tag{2}$$

$$C_f\frac{dv_{cf}(t)}{dt} = i_1(t) - i_g(t) \tag{3}$$

$$L_1\frac{di_1(t)}{dt} + R_1 i_1(t) = v_c(t) - v_f(t) \tag{4}$$

$$v_c(t) = \underbrace{(d_1(t) - d_2(t))}_{m(t)} v_D(t) \tag{5}$$

where $v_c(t)$ is the VSC terminal voltage, $d_1(t)$ and $d_2(t)$ are the duty ratios of S_9 and S_{11} ranging from zero to unity, and $m(t)$ is the modulation signal. The grid current typically has a faster response than the bus voltage. Thus, the instantaneous bus voltage $v_D(t)$ in (5) can be approximated with its average value V_D. Equations (1)–(5) lead to the transfer function of the grid current given by

$$i_g(s) = \underbrace{\frac{sC_fR_f + 1}{C_fL_1L_2s^3 + C_f(L_1+L_2)R_fs^2 + C_f(L_1+L_2)s}}_{G_{LCL}(s)} v_c(s) - \underbrace{\left(\frac{L_1C_fs^2}{C_fR_fs+1} + 1\right)}_{G_{fw}(s)} v_g(s) \tag{6}$$

Neglecting power losses in the VSC and the DAB DC-DC converter, the bus voltage is governed by

$$v_D(t)\left(C_D\frac{dv_D(t)}{dt}\right) = p_B(t) - v_c(t)i_1(t) \tag{7}$$

where $p_B(t)$ is the battery power. The instantaneous power in the *LCL* filter is comparatively small, which yields

$$v_c(t)i_1(t) \approx \underbrace{v_g(t)i_g(t)}_{p_g(t)} \tag{8}$$

where $p_g(t)$ is the instantaneous grid power. Substitution of (8) into (7) and linearizing around the average bus voltage setpoint V_D^*, the bus voltage dynamic becomes

$$V_D^*C_D\frac{dv_D(t)}{dt} \approx p_B(t) - p_g(t) \tag{9}$$

The grid voltage is given by

$$v_g(t) = \hat{V}_1\cos\omega t \tag{10}$$

where $\hat{V}_1$ is the amplitude of the fundamental component, and $\omega_1 = 2\pi f_1$ is the fundamental frequency of the grid voltage. The grid current is usually controlled to be sinusoidal with an amplitude of $\hat{I}_1$ and a phase angle of ϕ_1, as given by

$$i_g(t) = \hat{I}_1\cos(\omega t + \phi_1) \tag{11}$$

The grid current in (11) can be decomposed to the $dq-$axes components $i_d(t)$ and $i_q(t)$ in the virtual synchronous reference frame as

$$i_g(t) = \underbrace{\hat{I}_1\cos\phi_1}_{i_d}\cos\omega t - \underbrace{\hat{I}_1\sin\phi_1}_{i_q}\sin\omega t \tag{12}$$

The grid current in (11) leads to the instantaneous grid power expressed by

$$p_g(t) = \underbrace{\frac{\hat{V}_1}{2} i_d}_{P_{g1}} + \underbrace{\underbrace{\frac{\hat{V}_1}{2} i_d}_{P_{g1}} \cos 2\omega t - \underbrace{\frac{\hat{V}_1}{2} i_q}_{Q_{g1}} \sin 2\omega t}_{\widetilde{p}_{g1}(t)} \tag{13}$$

where $P_{g1}(t)$ and $Q_{g1}(t)$ are the average active and reactive power components, and $\widetilde{p}_{g1}(t)$ is the oscillating power component at the frequency of 2ω. The oscillating power component $\widetilde{p}_{g1}(t)$ causes a 2ω ripple component $\widetilde{v}_D(t)$ in the bus voltage, while the average power component $P_{g1}(t)$ changes the average component $V_D(t)$ of the bus voltage. By substituting $P_{g1}(t)$ in (13) into (9), $V_D(t)$ can be approximated as

$$V_D^* C_D \frac{dV_D(t)}{dt} \approx P_B(t) - \underbrace{\frac{\hat{V}_1}{2} i_d(t)}_{P_g(t)} \tag{14}$$

where $P_B(t)$ is the average component of the battery power. Note that (14) is accurate for a frequency below 2ω.

3.2. VSC Control System Implementation

Figure 4 shows the VSC control system. A proportional-integral (PI) regulator is employed for the bus voltage control loop with a low-pass filter (LPF) for shaping the loop frequency response. Meanwhile, the grid current controller adopts the unbalanced synchronous reference frame control with PI regulators for the fundamental component. This control technique employs the grid current as the α-component and the orthogonal reference current $i_\beta^*(t)$ as the β-component for the axis transformation. In our previous work [24], the stationary reference frame equivalence $G_{ci1}(s)$ of the unbalanced synchronous reference frame control with the PI regulators was theoretically and experimentally proven to be identical to a proportional-resonant regulator, as given by

$$G_{ci1}(s) = K_{p1} + \frac{K_{i1} s}{s^2 + \omega^2} \tag{15}$$

where K_{p1} and K_{i1} are the proportional and integral gains of the PI controller. Three possible harmonic sources distort the grid current waveforms, which can be suppressed by multiple resonant (MR) controllers given by

$$G_{cih}(s) = \sum_{h=3}^{n} \frac{K_{ih} s}{s^2 + (h\omega)^2} \tag{16}$$

where h is the harmonic order number, and K_{ih} is the resonant gain at order h^{th}.

Figure 5 depicts the stationary reference frame's equivalent grid current control block diagram. The VSC is represented by

$$G_{PWM}(s) = V_D e^{-sT_d} \tag{17}$$

where T_d is the delay time caused by the sampling time of the control system and the transportation time of the pulse width modulation (PWM) process. Undesirable low-frequency harmonic components can be present in the grid voltage $v_g(t)$ and in the VSC terminal voltage $v_c(t)$ due to switching dead times. The 2ω ripple component in the bus voltage control loop with a bandwidth greater than 0.2ω also distorts the reference current

$i_g^*(t)$ [24]. With this current control structure, the transfer functions of the grid current to these three harmonic sources are written as follows [24].

$$G_{cl}(s) = \frac{i_g(s)}{i_g^*(s)} = \frac{G_{ci}(s)G_{PWM}(s)G_{LCL}(s)}{1 + \{G_{ci}(s) + G_{cih}(s)\}G_{PWM}(s)G_{LCL}(s)} \tag{18}$$

$$Y_{VSC}(s) = \frac{i_g(s)}{v_c(s)} = \frac{G_{LCL}(s)}{1 + \{G_{ci}(s) + G_{cih}(s)\}G_{PWM}(s)G_{LCL}(s)} \tag{19}$$

$$Y_g(s) = \frac{i_g(s)}{v_g(s)} = \frac{-G_{FW}(s)G_{LCL}(s)}{1 + \{G_{ci}(s) + G_{cih}(s)\}G_{PWM}(s)G_{LCL}(s)} \tag{20}$$

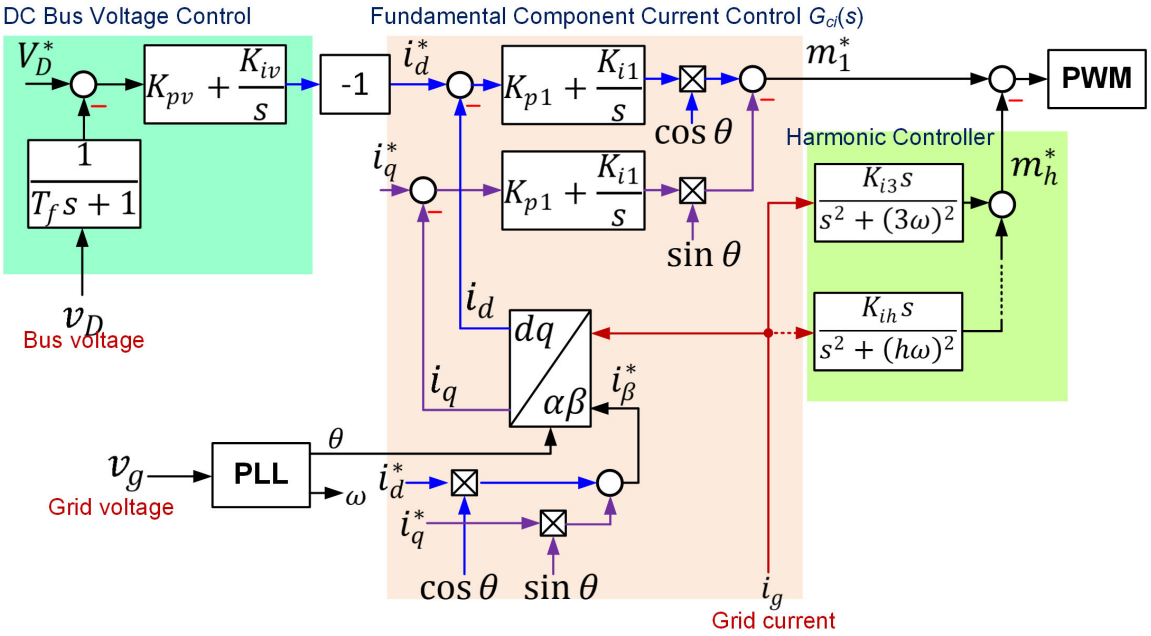

Figure 4. Bust voltage and grid current control block diagram of the VSC.

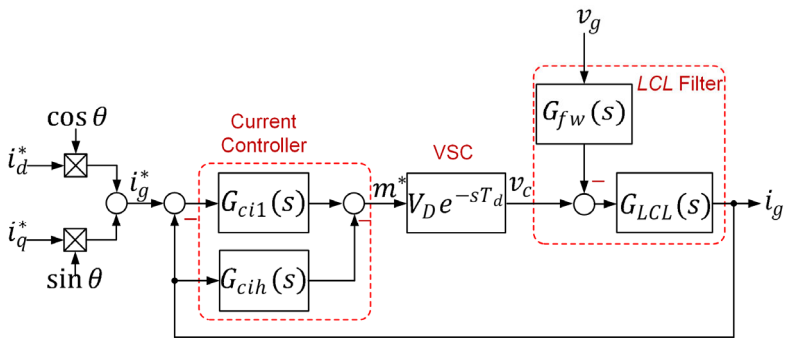

Figure 5. The stationary reference frame's equivalent control block diagram of the grid current in the stationary reference frame.

The MR regulator has infinite gains at selective frequencies, attenuating the harmonic components in $i_g^*(t)$, $v_g(t)$, and $v_c(t)$. Meanwhile, the fundamental component of $i_g^*(t)$ is regulated by the unbalanced synchronous reference frame controller with an infinite gain at ω_1. Figure 6 depicts the equivalent bus voltage control loop. The low-pass filter time constant T_f designed with the PI controller's constants K_{pv} and K_{iv} is used for loop shaping. The grid current control loop is approximated as a unity gain because its bandwidth is far higher than the bus voltage control loop. The rejection of the harmonic components in the

reference current allows the bandwidth of the bus voltage control loop to increase while maintaining the grid current near sinusoidal.

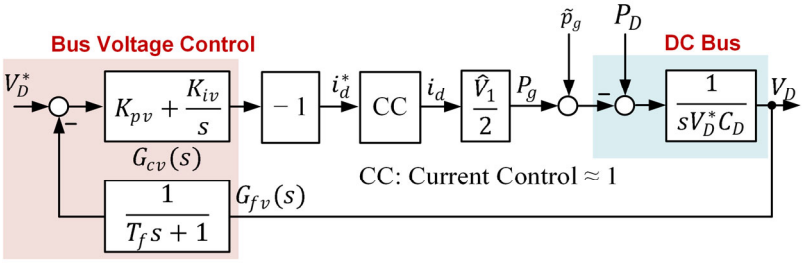

Figure 6. Equivalent control block diagram of the bus voltage.

This study employs the discontinuous PWM techniques shown in Figure 7. The positive half of $m(t)$ is used as the duty ratio reference for switches S_9 and S_{10}, and the positive half of $-m(t)$ for switches S_{11} and S_{12}. This PWM technique has a lower common-mode voltage and switching loss than the unipolar PWM [27]. Meanwhile, the VSC current $i_1(t)$ maintains a small ripple due to the three-level voltage output at the VSC terminal. Figure 8 illustrates the generation of the switching signals and interrupt setting. Time base counter 1 of the microcontroller [26] is set to operate in the up-down mode with the counter maximum value of PWMprd, which generates the interrupt signal when the counter value equals zero. The value of PWMprd is obtained from

$$\text{PWMprd} = \frac{1}{2} \times \frac{f_{clk}}{f_{sw}} \tag{21}$$

where $f_{clk} = 100$ MHz is the microcontroller's clock frequency [26]. Thus, PWMprd = 2500 for a switching frequency of 20 kHz. This interrupt signal simultaneously triggers the selected analog-to-digital converters (ADCs) for voltage and current signal sampling at the time instant k and the interrupt service routine (ISR) of the control algorithm for the VSC and DAB DC-DC converter. The resultant duty ratios are updated at the time instant $k+1$. Each counter consists of two compare registers (CMPAx and CMPBx), independently controlling two PWM outputs (PWMxA and PWMxB). For the VSC control, only CMPAx registers generate the PWMxA outputs, while the PWMxB outputs are opposite to the relevant PWMxA outputs with a switching dead time (active high complementary with a dead time) [26]. Thus, the PWM1A and PWM1B outputs of counter 1 control switches S_9 and S_{10}, and the PWM2A and PWM2B outputs of counter 2 for switches S_{11} and S_{12}. The synchronized operation between the ADC and PWM samples the average value of the grid current in each switching period both for the positive and negative regions of the modulation signal, as illustrated in Figure 8.

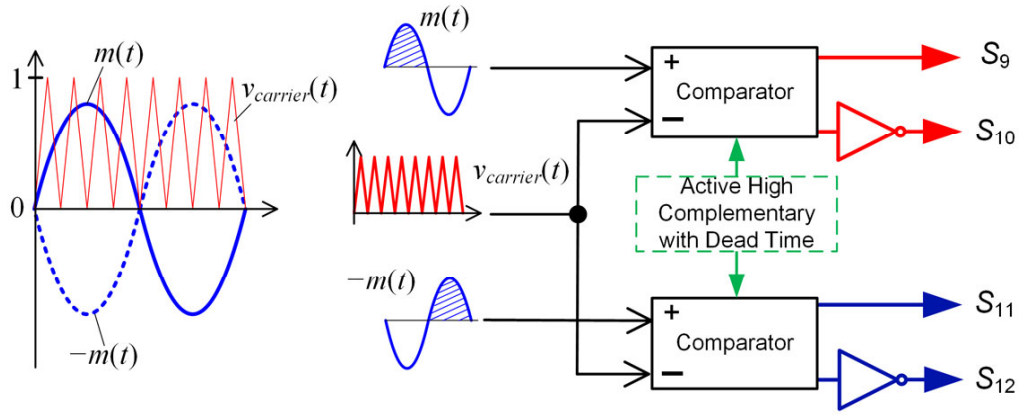

Figure 7. Discontinuous PWM block diagram for the VSC.

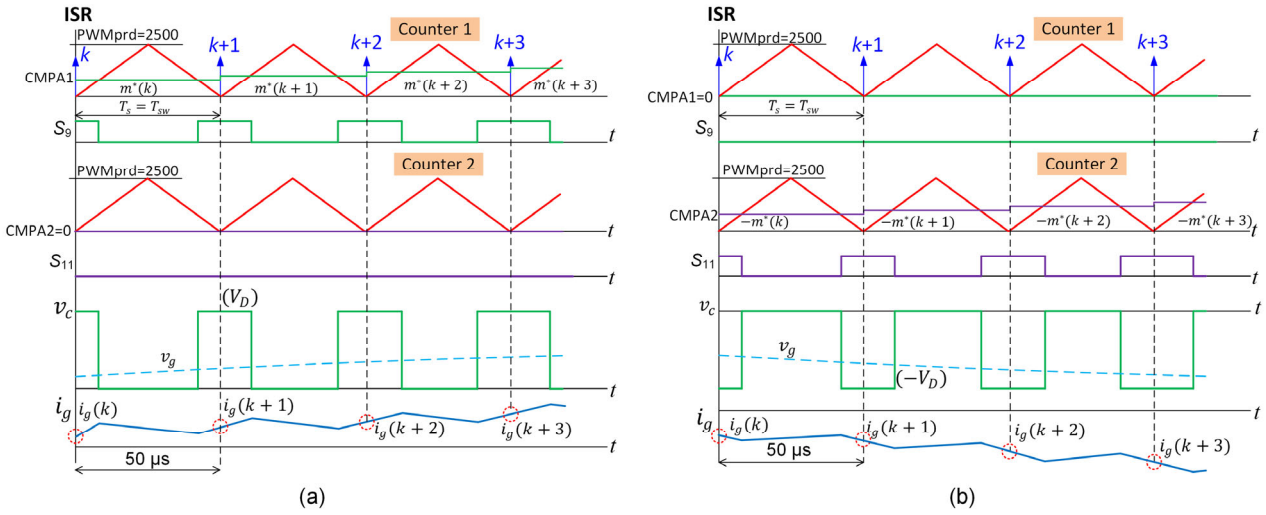

Figure 8. Timing diagram for interrupts, PWM generation, and analog signal samplings of the VSC: (**a**) for $m^*(t) \geq 0$; (**b**) for $m^*(t) < 0$.

4. Implementation of the Battery-Side DAB DC-DC Converter

4.1. Basic Operation of the DAB DC-DC Converter

Figure 9 illustrates the basic operation waveforms of the DAB DC-DC converter in the SPS modulation mode, where $\omega_{sw} = 2\pi f_{sw}$ and $\theta_{sw} = \omega_{sw} t$. The voltage $v_P(\theta_{sw})$ of the LV bridge leads the voltage $v_s(\theta_{sw})$ of the HV bridge by a phase angle of δ, which causes power to flow from the battery to the bus voltage. On the other hand, power transfers from the bus voltage to the battery with a phase angle of $-\delta$. Thus, the transferred power P_{DAB} of the DAB DC-DC converter is controlled by the angle δ by

$$P_{DAB} = \frac{V_D \left(\frac{N_s}{N_p}\right) V_B}{\omega_{sw} L_a} \delta \left(1 - \frac{|\delta|}{\pi}\right) \tag{22}$$

Neglecting losses in the DAB DC-DC converter, the average value I_{LVB} of the LV bridge input current i_{LVB} and the average battery current I_B are derived from P_{DAB} by

$$I_B = I_{LVB} = \frac{P_{DAB}}{V_B} = \left(\frac{N_s}{N_p}\right) \frac{V_D}{\omega_{sw} L_a} \delta \left(1 - \frac{|\delta|}{\pi}\right) \tag{23}$$

Hence, the phase angle δ is used as the controlled variable for the battery current control loop as shown in Figure 3. The theoretical range of the phase angle δ is $\pm\pi/2$. The DAB DC-DC converter exhibits the ZVS operation if the ratio between the voltages of the two DC sides is close to the transformer's turn ratio [28]. This ZVS range gets wider at a higher phase shift angle [14]. On the other hand, the root mean square (RMS) values of the MF transformer's currents increase with the phase shift angle [10].

Flux density $B(t)$ is an essential parameter for the design of the MF transformer and series inductor. According to the circuit topology in Figure 3, the transformer's primary winding is directly connected to the LV bridge. So, the peak flux density $\hat{B}_T$ of the transformer is proportional to the battery voltage, as given by

$$\hat{B}_T = \frac{1}{2N_p A_c} \int_0^{T_{sw}/2} v_p dt = \frac{V_B T_{sw}}{4N_p A_c} \tag{24}$$

where A_c is the cross-sectional area of the transformer core. Meanwhile, the peak flux density $\hat{B}_L$ of the series inductor is determined from the voltage across the inductor $v_{La}(\theta_{sw})$ in Figure 9, as given by

$$\hat{B}_L = \frac{1}{2N_L A_c}\int_0^{T_{sw}/2} v_{La}dt = \frac{T_{sw}}{4N_L A_c}\left\{\pi\frac{N_s}{N_p}V_B + (2\delta - \pi)V_D\right\} \quad (25)$$

where N_L is the winding turn number of the inductor. The peak flux densities $\hat{B}_T$ and $\hat{B}_L$ must be kept below the saturation flux density $\hat{B}_{sat}$ of the core material.

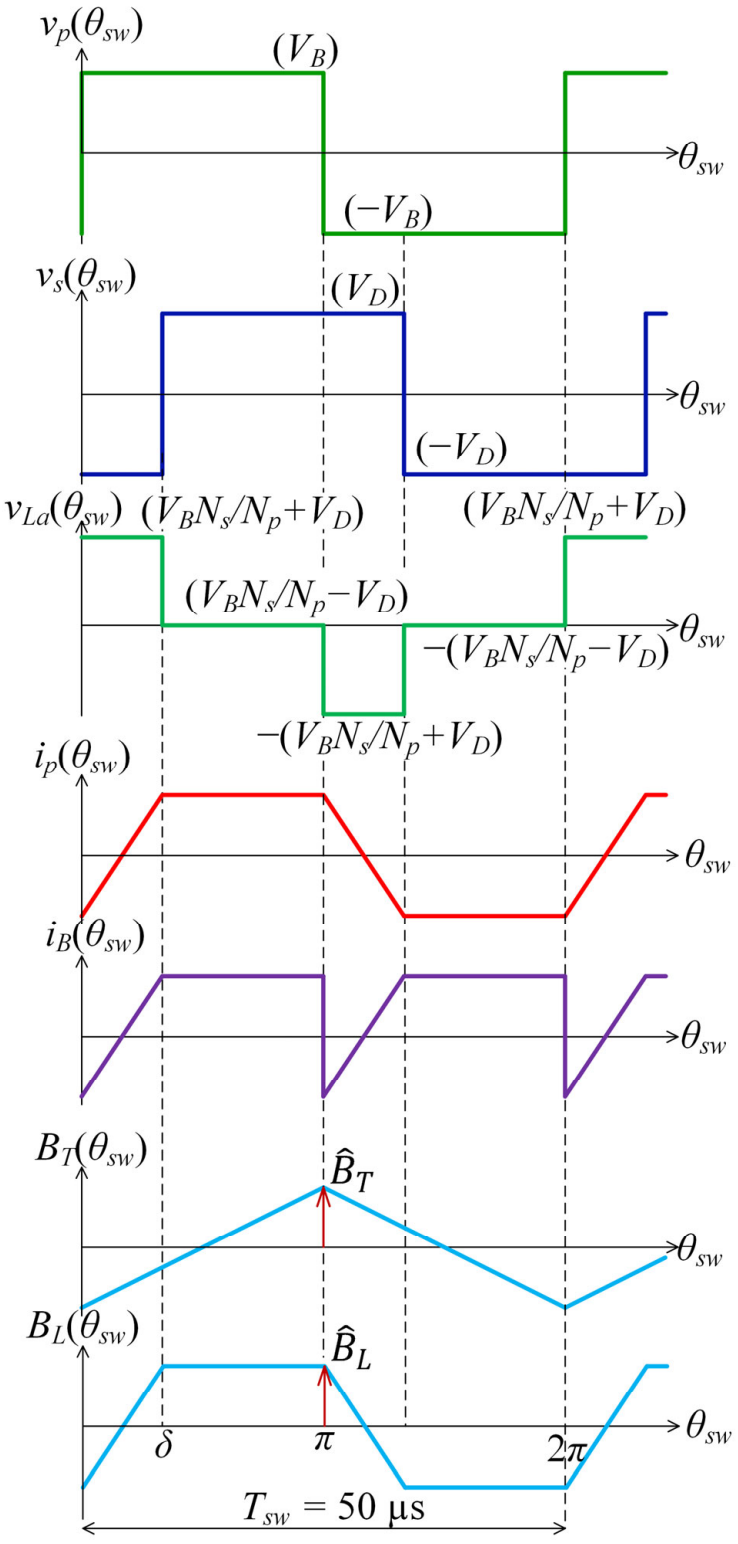

Figure 9. Voltage, current, and flux density waveforms of the DAB DC-DC converter with the SPS modulation strategy [28].

4.2. Design of the Transformer and Series Inductor

The MF transformer of the DAB DC-DC converter is a crucial element for transferring power and voltage conversion between the two DC sides. Meanwhile, the series inductor L_a limits the maximum power transfer. MnZn ferrite and nanocrystalline materials are suitable for the switching frequency of 20 kHz used in this study. For this application, the battery voltage varies with the state of charge and battery current, while the bus voltage is kept constant. Thus, the maximum allowable phase shift angle is $\pm\pi/3$ to exploit a large ZVS range at the rated power and achieve a fine battery current resolution, while the RMS values of the transformer currents are still acceptable. It was reported that nanocrystalline materials exhibited better power density and efficiency than MnZn ferrite material [10]. However, the cutting process of ribbon-wound nanocrystalline cores deteriorated their magnetic properties [10]. Hence, we selected N87 MnZn ferrite cores due to consistency in magnetic properties and market availability [29]. This core material has a saturation flux density of 0.39 T at 100 °C and is available in various core shapes.

An analytical transformer and inductor design method was chosen in this study [30]. The generalized Steinmetz equation expresses the core loss P_{fe} as a function of the core peak flux density $\hat{B}$. Meanwhile, the copper loss P_{cu} is derived from the RMS values of the transformer's currents and the winding resistance. Therefore, the winding resistance is derived from the core geometry, which is expressed as a function of the core peak flux density $\hat{B}$. Setting $P_{fe} = P_{cu}$ leads to the optimal peak flux density $\hat{B}_{opt}$, from which the minimum core size is obtained. An actual core size should be selected close to the optimal one.

The MF transformer and the inductor were designed at the nominal battery voltage V_{Bn} of 51.2 V using the peak flux densities given in (24) and (25). The transformer turn ratio is close to

$$\frac{N_s}{N_p} = \frac{V_D}{V_{Bn}} = \frac{400\ \text{V}}{51.2\ \text{V}} = 7.81 \tag{26}$$

The peak flux densities $\hat{B}_T$ and $\hat{B}_L$ calculated at the maximum battery voltage of 60 V were ensured to be below the core saturation value. The core loss coefficient was identified from the manufacturer's specification at the temperature of 100 °C. Enameled Litz wires were employed to minimize the skin and proximity effects from the switching frequency. The required value of L_a obtained from (23) is 297 µH. However, the inductance of 280 µH was used in the design to account for the leakage inductance of the MF transformer. Table 3 summarizes the key parameters of the MF transformer and series inductor. The actual core sizes are slightly larger than the required sizes. Thus, the peak flux densities $\hat{B}_T$ and $\hat{B}_L$ are smaller than their optimal values. This results in the estimated core losses being comparatively less than the copper losses. The predicted core loss using the generalized Steinmetz equation is based on the sinusoidal induction waveform. Moreover, the N87 ferrite material has a more significant core loss at low temperatures. In experiments, the core temperature was found to be lower than 60 °C, which agrees with our previous work with the same design methodology and core material [10]. Thus, the actual core losses are expected to exceed the predicted values.

Table 3. Parameters of the MF transformer and series inductor.

Parameters	Transformer	Inductor
Material	EPCOS N87 ferrite	EPCOS N87 ferrite
Core structure	2 sets of E65/32/27	1 set of ETD49 with 2 mm gap
Total core area, A_c	10.58 cm^2	2.11 cm^2
Magnetic length, l_m	14.7 cm	11.4 cm
Primary winding	4 turns 4 Litz wires (500 × WG40)	55 turns 2 Litz wires (128 × AWG40)
Secondary winding	31 turns 2 Litz wires (128 × AWG40)	-
$\hat{B}$ at 51.2 V/60 V	0.20 T/0.24 T	0.28 T/0.36 T

Table 3. *Cont.*

Parameters	Transformer	Inductor
Est. P_{cu} at 51.2 V V	9.1 W	4.0 W
Est. P_{fe} at 51.2 V V	8.7 W	2.2 W
Est. P_{tot} at 51.2 V V	17.8 W	6.2 W

4.3. Control System Implementation of the DAB DC-DC Converter

Figure 10 sketches the steady state timing diagram of the DAB DC-DC converter, implemented in the same ISR as the VSC control scheme in Figure 8. Counters 3–6 in the up-down mode generate the switching signals for the DAB DC-DC converter. The phase angles of counters 3–6 are synchronized with counter 1. Instead, the phase shift modulation is obtained by adjusting the CMPA3 to CMPA6 and the CMPB3 to CMPB6 registers of counters 3–6 [31]. During the rising period of counters 3–6, switches S_1, S_4, S_5, and S_8 are turned on when the values of the counters equal their CMPAs registers. For the falling period, switches S_1, S_4, S_5, and S_8 are turned off when the values of the counters equal their CMPBs registers. Thus, this modulation strategy accommodates the maximum phase shift angle of $\pm\pi/2$. Note that switches S_2, S_3, S_6, and S_7 complement switches S_1, S_4, S_5, and S_8 respectively.

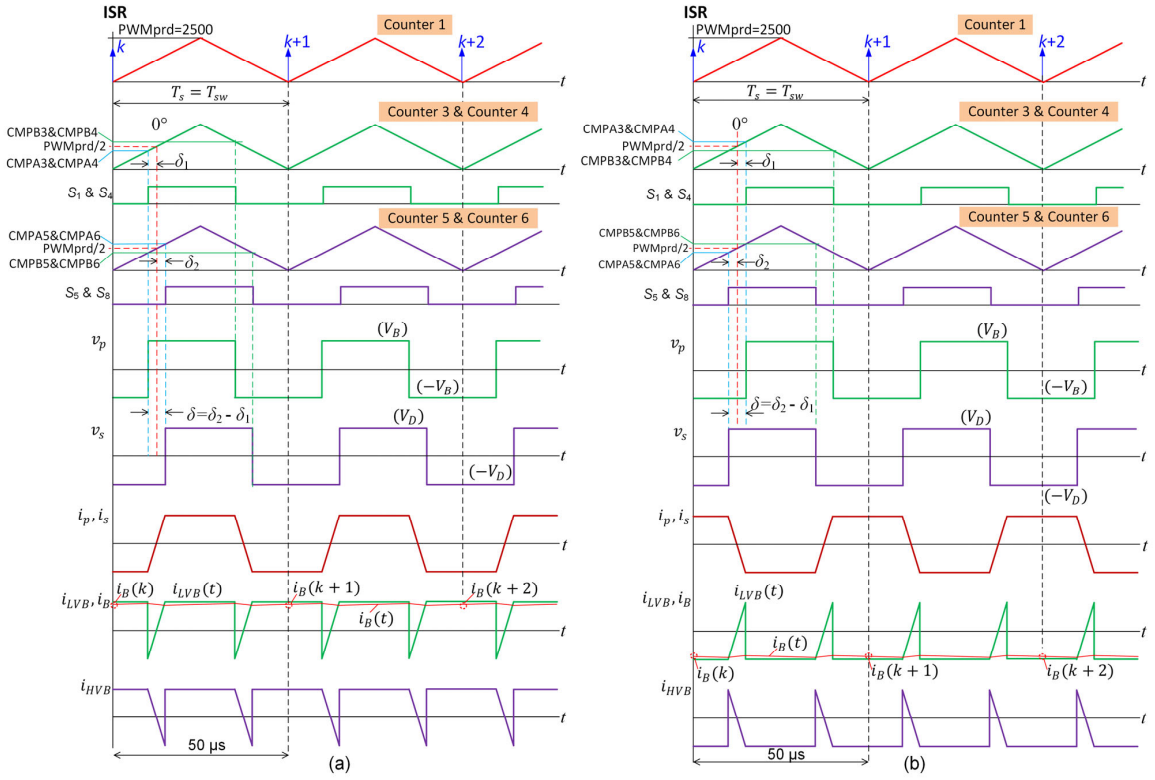

Figure 10. Steady-state timing diagram for the DAB DC-DC converter: (**a**) for $i_B(t) \geq 0$ (**b**) for $i_B(t) < 0$.

The phase shift angle $\delta = 0$ is set at $\pi/2$ of each ISR period to sample the average value of the battery current $i_B(t)$. The reference phase angles δ_1^* and δ_4^* for switches S_1 and S_4 of the LV bridge and δ_5^* and δ_8^* for switches S_5 and S_8 of the HV bridge are obtained from

$$\left.\begin{array}{l} \delta_1^* = \delta_4^* = -\frac{\delta^*}{2} \\ \delta_5^* = \delta_8^* = \frac{\delta^*}{2} \end{array}\right\} \quad (27)$$

where δ^* is the reference phase shift angle. Figure 9 shows the implementation diagram of the battery current control. The battery current is sampled every T_s. The discrete-time PI controller $G_{CB}(z)$ regulates the battery current $i_B(k)$ at instant k with the reference phase angle $\delta^*(k)$ as the output. The reference angles $\delta_1^*(k)$, $\delta_4(k)$, $\delta_5^*(k)$, and $\delta_8^*(k)$ are obtained from (27). The reference angles $\delta_1^*(k)$ and $\delta_8^*(k)$ are translated to the values of the CMPA3, CMPB3, CMPA6, and CMPB6 registers as depicted in Figure 11. Meanwhile, the reference angles $\delta_4(k)$ and $\delta_5^*(k)$ are delayed with a sampling period to prevent a large DC offset current in the transformer current $i_p(t)$ during the transient [20]. This method is to control the volt-second applied to the transformer to maintain a small DC offset. So, the values of CMPA4, CMPB4, CMPA5, and CMPB5 are accordingly determined from $\delta_4(k-1)$ and $\delta_5^*(k-1)$. The action qualifier submodule of each module defines the action of the PWMxA output when the CMPAx and CMPBx registers meet their conditions as indicated by "set" and "clear" in the brackets. Meanwhile, the PWMxB outputs are opposite to their PWMxA outputs, with a dead time of 1.25 µs similar to that of the VSC [26].

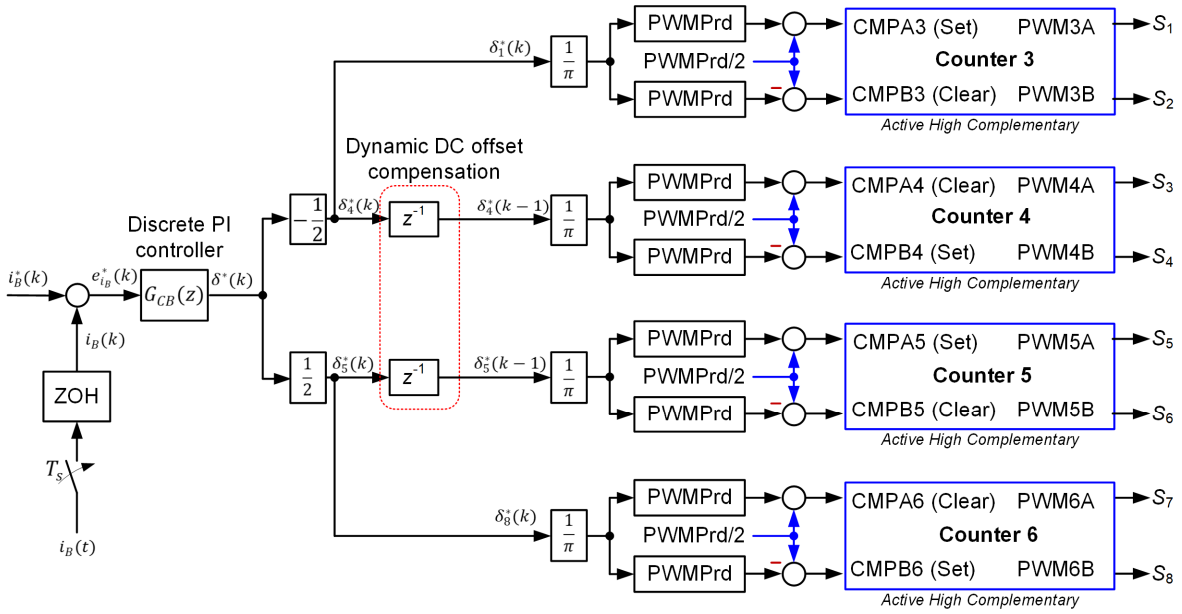

Figure 11. Implementation diagram of the battery current control loop of the DAB DC-DC converter.

4.4. Tuning of the Battery Current Control Loop

Figure 12 depicts the equivalent circuit on the battery side. The variables are averaged over a switching period of T_{sw}, denoted by the brackets $\langle\ \rangle$. Equation (23) yields the average current $\langle i_{LVB} \rangle$ of the DAB DC-DC converter, while the battery is simplified with an open-circuit voltage $\langle e_0 \rangle$ and an internal resistance R_i. The Thevenin-based equivalent circuit consisting of internal series resistance and capacitance paralleled with another resistance is more accurate than that in Figure 12 [32]. The Thevenin-based capacitance is much larger than the battery-side capacitance C_B [33]. From the control point of view, thus, the open-circuit voltage $\langle e_0 \rangle$ in Figure 12 including the voltage drops in the Thevenin-based capacitance is the disturbance of the battery current control loop. Figure 13 depicts the equivalent block diagram of the battery current in the continuous time domain, where a PI regulator with the constants K_{pb} and K_{ib} controls the battery current. A delay of $T_d = 2T_s$ represents the sampling and transport delays, as illustrated in Figure 10. The gain K_{DAB} is derived from the possible maximum value of (23), as given by

$$K_{DAB} = \frac{\langle i_{LVB} \rangle}{\delta} = \left(\frac{N_s}{N_p}\right) \frac{V_D}{\omega_{sw} L_a} \tag{28}$$

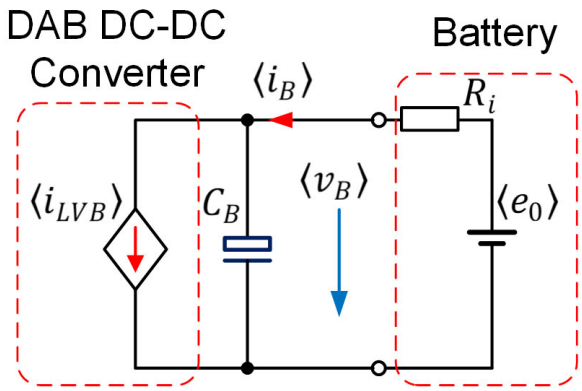

Figure 12. Equivalent circuit on the battery side.

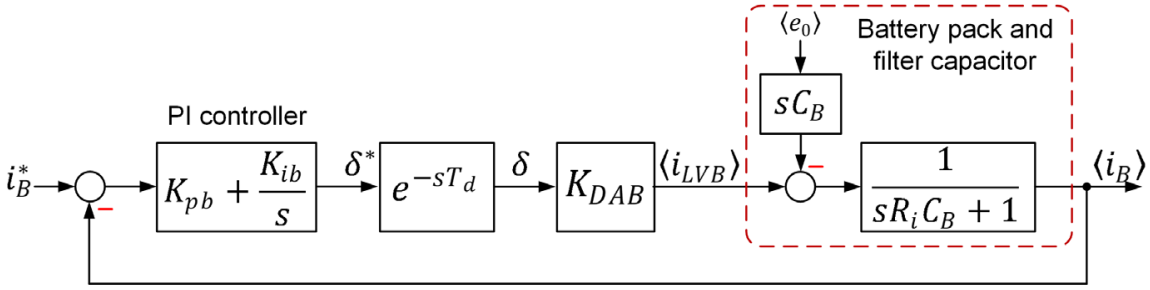

Figure 13. Equivalent control block diagram of the battery current.

According to (23), this gain K_{DAB} decreases with the angle δ for a higher battery current. However, the approximated gain K_{DAB} at its maximum value guarantees the maintenance of loop stability at a high current.

The open loop transfer function of the battery current control loop is written as

$$G_{bol}(s) = \left(K_{pb} + \frac{K_{ib}}{s}\right)\frac{K_{DAB}}{sR_iC_B + 1} \tag{29}$$

where the delay T_d is neglected as it usually is much smaller than the time constant R_iC_B. The closed-loop transfer function is given as

$$G_{bcl}(s) = \frac{\left(\frac{K_{DAB}}{R_iC_B}\right)s + \left(\frac{K_iK_{DAB}}{R_iC_B}\right)}{s^2 + \left(\frac{1+K_{pb}K_{DAB}}{R_iC_B}\right)s + \left(\frac{K_iK_{DAB}}{R_iC_B}\right)} \tag{30}$$

Compared to the standard second-order system [34], K_{pb} and K_{ib} can be written as

$$\left.\begin{aligned} K_{ib} &= \omega_0^2\frac{R_iC_B}{K_{DAB}} \\ K_{pb} &= \frac{2\xi\omega_0R_iC_B - 1}{K_{DAB}} \end{aligned}\right\} \tag{31}$$

where ω_0 is the natural frequency, and ξ is the damping factor of the closed-loop system. If R_i is unknown, a trial-and-error tuning method can be adopted by adjusting K_{ib} for ω_0^2 and K_{pb} for ξ.

5. Experimental Validation

5.1. Experimental Setup

Figure 14 depicts the experimental setup. A TMS320F280049C microcontroller controlled the VSC and DAB DC-DC converter with the parameters listed in Table 2. A switching dead time of 1.25 µs was applied to each leg of the VSC and DAB DC-DC con-

verter. A 16-cell 100 Ah LFP battery pack supplied the DAB DC-DC converter, while the VSC was connected to a Chroma 61860 grid simulator. We adopted the tuning procedure of the VSC presented in our previous work [24] with a bus voltage bandwidth of 30π rad/s and the current harmonic controllers, orders 3rd, 5th, 7th, and 9th for mitigation of the grid current waveform. The bus voltage was regulated at 400 V. The response of the battery current was tuned by the trial-and-error method with the guidelines given in (31). The battery management system has a maximum current of 30 A, which, unfortunately, limits the maximum system power within ± 1.5 kW or 50% of the rated power.

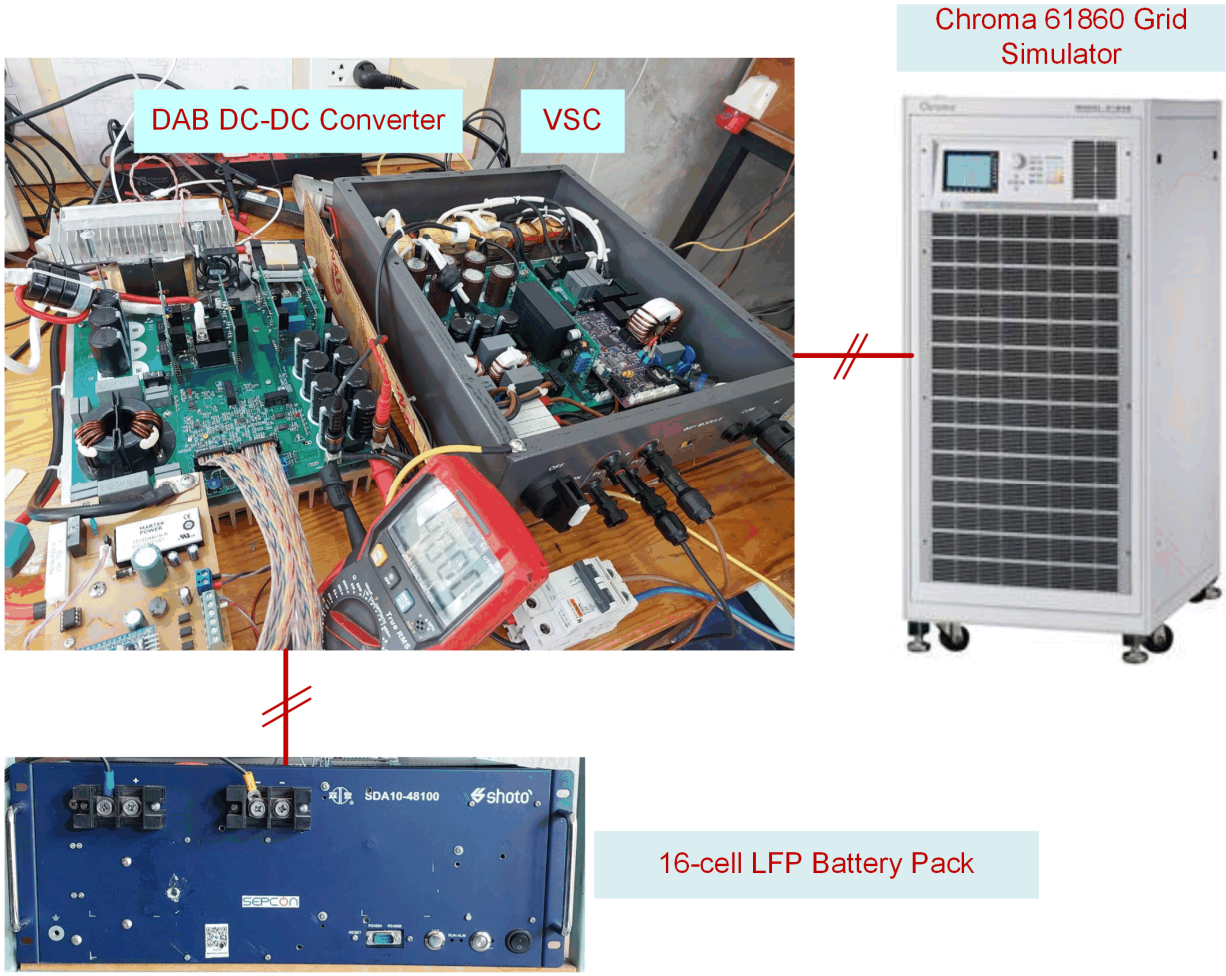

Figure 14. Experimental setup.

5.2. Experimental Results

5.2.1. Validation of the Dynamic DC Offset Compensation Scheme

The grid simulator supplied the VSC, and the bus voltage was regulated at 400 V. The DAB DC-DC converter operated with the reference phase angle δ^* in the open-loop control. Figure 15a depicts the transient response of the primary and secondary voltages $v_p(t)$ and $v_s(t)$, the transformer's primary current $i_p(t)$, and the inverted battery current $-i_B(t)$ under the step change of the reference angle δ^* changing from zero to $\pi/4$. In contrast, Figure 15b shows those waveforms for the reference angle δ^* changing from zero to $-\pi/4$. Without the dynamic DC offset compensation scheme shown in Figure 11, $i_p(t)$ exhibits a DC offset of approximately 30 A. This large current can cause saturation in the transformer core and may damage the switching devices. The DC offset compensation technique in Figure 11 is effective as the dynamic DC component of $i_p(t)$ is reduced significantly during the changes in the reference angle δ^*. Meanwhile, the DC offset compensation scheme does

not affect the steady waveform of $i_p(t)$. The first-order response of the battery current $i_B(t)$ agrees with the equivalent circuit in Figure 12.

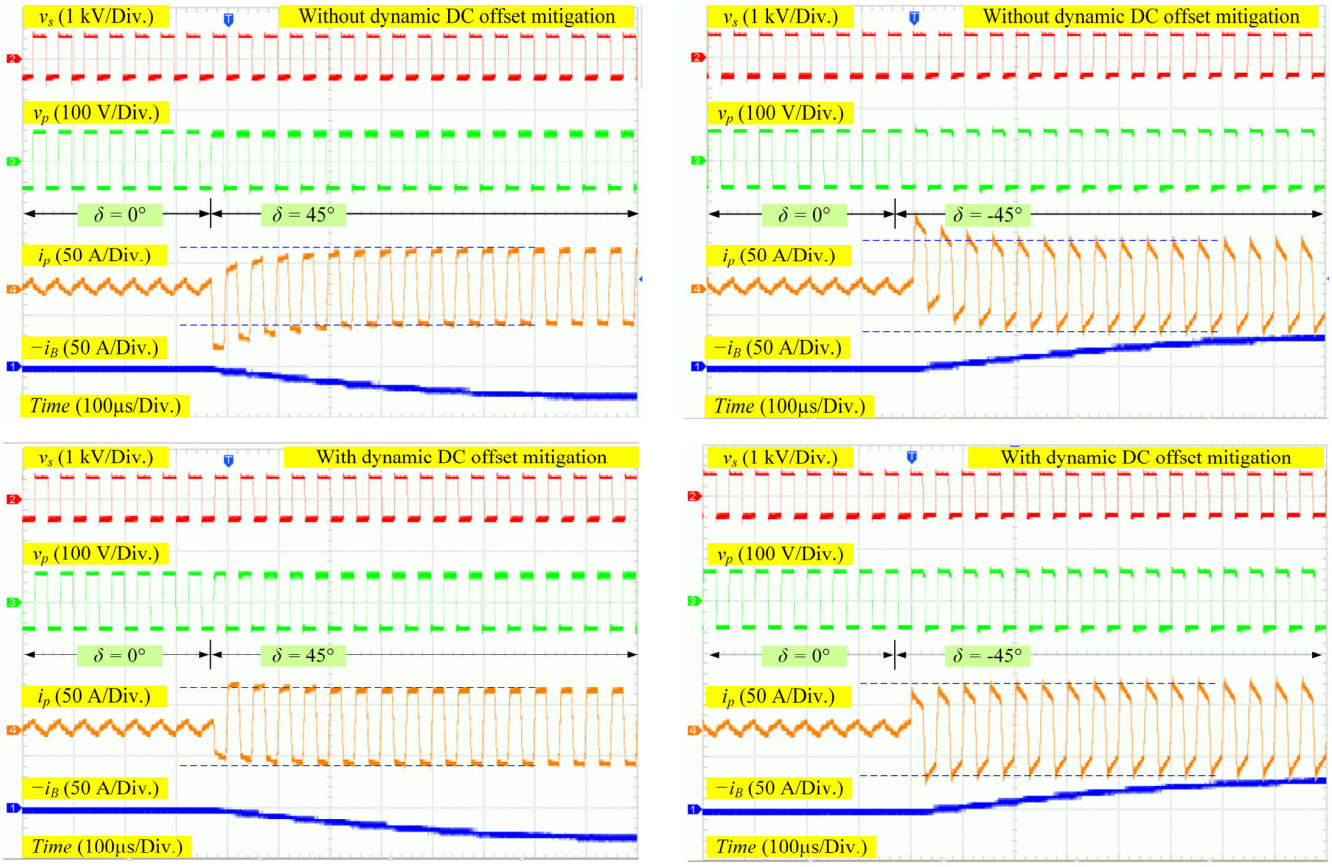

Figure 15. Open-loop transient response of the DAB DC-DC converter with and without the dynamic DC offset compensation scheme: (**a**) δ^* changing from 0 to $\pi/4$; (**b**) δ^* changing from 0 to $-\pi/4$.

5.2.2. Validation of the Closed-Loop Control of the Battery Current

The battery current control loop was tuned for a smooth response with a settling time of approximately 80 ms. The reference battery current i_B^* was set to create the battery power in the range of $\pm$1.5 kW. Figure 16 shows the experimental results in the discharging mode with a battery power of 1.5 kW. Although the discharged power from the battery causes the bus voltage to increase, the bus voltage controller forces the bus voltage to return to the reference of 400 V within four cycles, as shown in Figure 16a. Figure 16b depicts the steady-state waveforms of $v_D(t)$, $v_g(t)$, and $i_g(t)$. The grid current waveform is nearly sinusoidal thanks to the current harmonic current controller, which attenuates the harmonic components in the reference grid current and the VSC terminal voltage caused by the dead time. Figure 16c illustrates that a step change in the battery reference current i_B^* does not create a DC offset in the transformer's primary current $i_p(t)$, thanks to the DC offset compensation scheme implemented in the SPS modulation system in Figure 11. Meanwhile, the battery current $i_B(t)$ smoothly increases toward its reference. The steady-state waveforms of $v_p(t)$, $v_s(t)$, and $i_p(t)$ in Figure 16d agree with the sketched waveforms in Figure 10. At this operating point, the battery voltage was 51.5 V, close to the designed value of the MF transformer.

Figure 17 shows the experimental results in the charging mode with a battery power of $-$1.5 kW. The bus voltage $v_D(t)$, grid current $i_g(t)$, transformer's primary current $i_p(t)$, and battery current $i_B(t)$ respond to the battery reference current i_B^* in the same fashion as the discharging mode with the opposite direction. The steady-state grid current waveform

remains nearly sinusoidal. However, the steady-state waveform of $i_p(t)$ indicates that the DAB DC-DC converter operates in the boost mode, where $(N_s/N_p)V_B > V_D$ [19]. At this operating point, the battery voltage was 54.3 V, causing $(N_s/N_p)V_B = 424$ V.

Figure 18 shows the battery voltage, total efficiency of the VSC and DAB DC-DC converter, and total harmonic distribution (THD_i) of grid current with battery power. As expected, the battery voltage in the charging mode is greater than that in the discharging mode. The inverter's efficiency in the charging mode is lower than in the discharging mode. Partly, it is believed to be due to the mismatched voltage ratio of the MF transformer, which deviates the operating point out of the ZVS region o and increases RMS values in the transformer currents [28]. Thus, a variable DC voltage strategy with the battery voltage and a duty ratio adjustment of the transformer would improve the inverter's efficiency. The THDi values at 50% of the rated power are less than 1.5%, which are expected to be lower at the rated power of 3 kW.

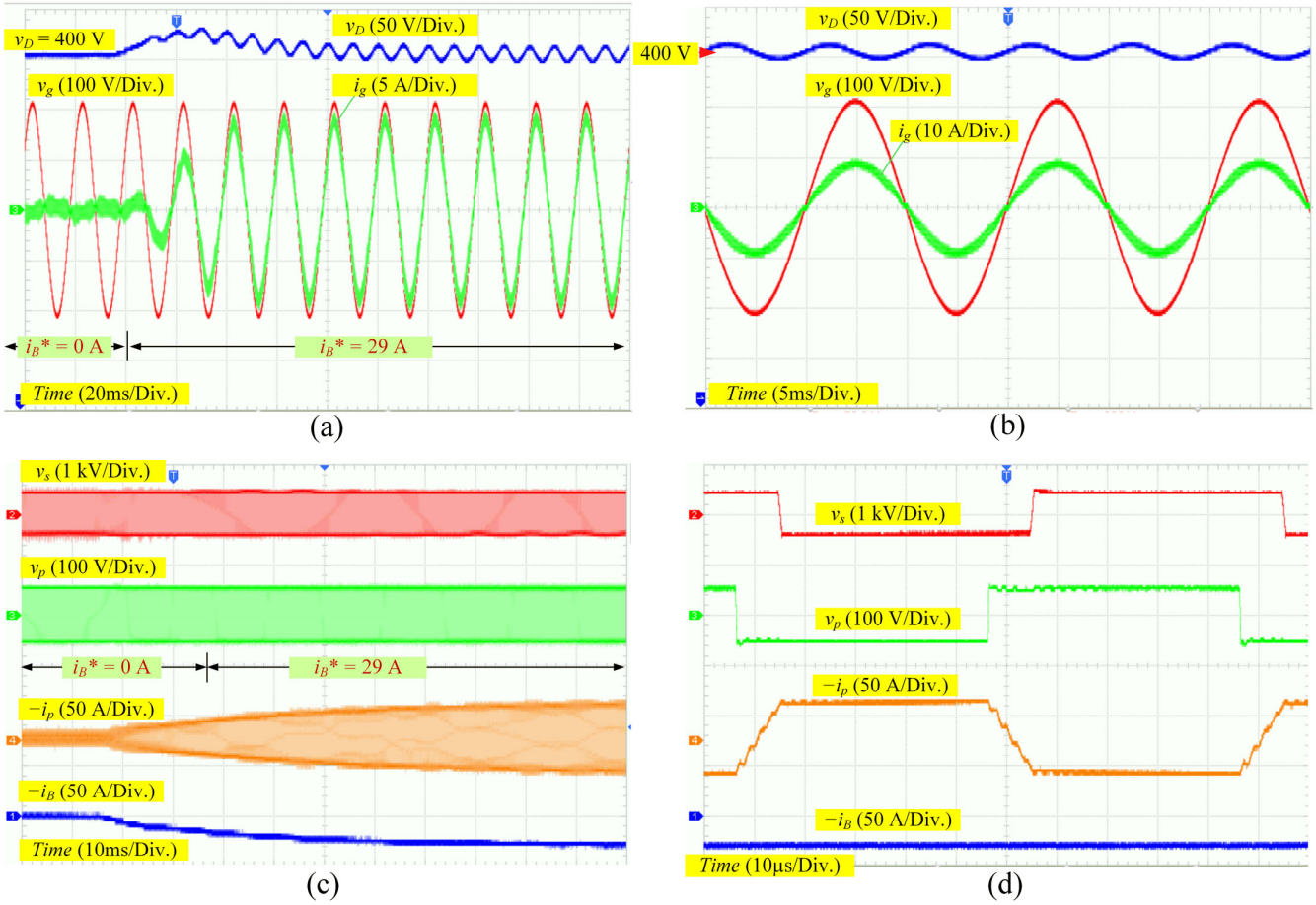

Figure 16. Experimental results of the closed-loop control of the battery current in the discharging mode with the battery power of 1.5 kW: (**a**) transient response of the bus voltage $v_D(t)$, grid voltage $v_g(t)$, and grid current $i_g(t)$; (**b**) steady-state waveforms of the bus voltage $v_D(t)$, grid voltage $v_g(t)$, and grid current $i_g(t)$; (**c**) transient response of the primary and secondary voltages $v_p(t)$ and $v_s(t)$, the transformer's inverted primary current $-i_p(t)$, and the inverted battery current $-i_B(t)$; (**d**) steady-state waveforms of the primary and secondary voltages $v_p(t)$ and $v_s(t)$, the transformer's inverted primary current $-i_p(t)$, and the inverted battery current $-i_B(t)$.

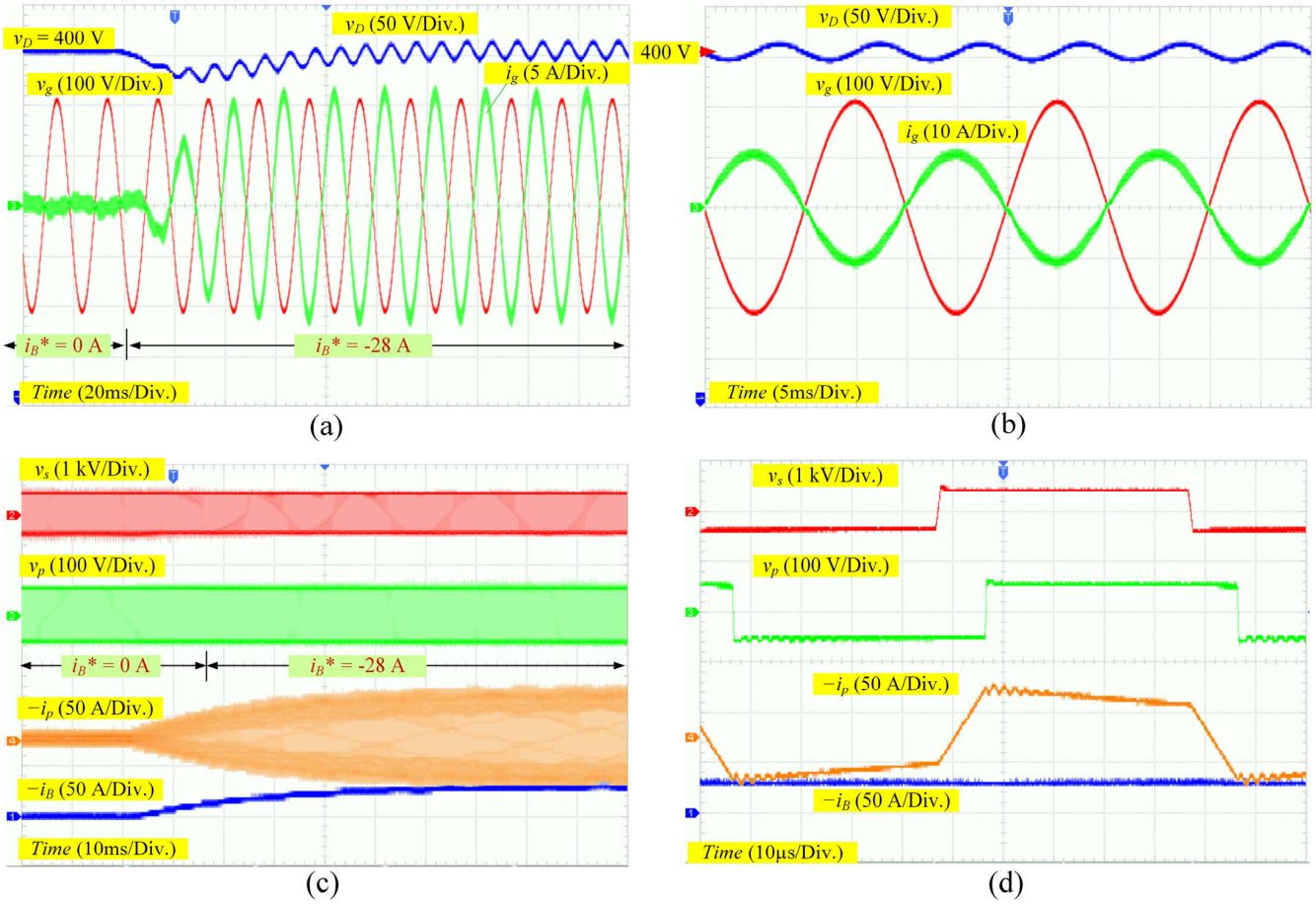

Figure 17. Experimental results of the closed-loop control of the battery current in the charging mode with the battery power of −1.5 kW: (**a**) transient response of the bus voltage $v_D(t)$, grid voltage $v_g(t)$, and grid current $i_g(t)$; (**b**) steady-state waveforms of the bus voltage $v_D(t)$, grid voltage $v_g(t)$, and grid current $i_g(t)$; (**c**) transient response of the primary and secondary voltages $v_p(t)$ and $v_s(t)$, the transformer's inverted primary current $-i_p(t)$, and the inverted battery current $-i_B(t)$; (**d**) steady state waveforms of the primary and secondary voltages $v_p(t)$ and $v_s(t)$, the transformer's inverted primary current $-i_p(t)$, and the inverted battery current $-i_B(t)$.

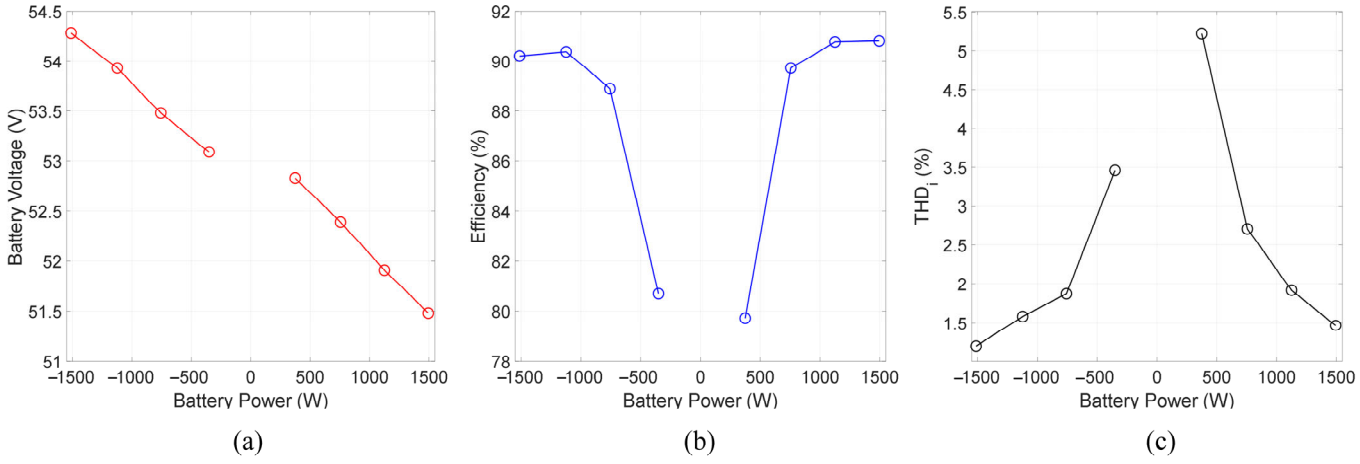

Figure 18. (**a**) Battery voltage V_B with battery power; (**b**) inverter's efficiency with battery power; (**c**) total harmonic distortion of grid current with battery power.

6. Conclusions and Future Outlook

A single-phase grid-connected 51.2-V battery inverter consisting of an *LCL*-filtered voltage source converter (VSC) and a dual active bridge (DAB) DC-DC converter was constructed. The control systems of the two converters were implemented in the same interrupt service routine on a TMS320F280049C microprocessor with a sampling and switching frequency of 20 kHz—the time base counters for switching generation of the DAB DC-DC converter synchronized with those of the VSC. The single-phase shift modulation strategy of the DAB DC-DC converter was adjusted through two separate compare registers with the time base counters during the count-up and count-down periods. This phase shift modulation was easy to implement on a standard microcontroller for power converter control. A DC offset compensation integrated with the battery current control loop allowed a smooth change in the battery and medium-frequency transformer's currents in response to a reference current step. The VSC adopted a bus voltage control with a unified harmonic mitigation strategy. Experimental validations in the charge and discharge operations exhibited a total system efficiency better than 90% and total harmonic distortion in the grid current lower than 1.5%.

However, certain aspects must be studied further to improve the proposed residential battery inverter as follows:

(1) Adoption of advanced battery current control schemes regardless of the battery's internal impedance parameters.
(2) Increasing the switching frequency and improving the modulation strategies of the DAB DC-DC converter to enhance efficiency and power density.
(3) Optimizing the design of the ripple filter on the battery side.

Author Contributions: Conceptualization, A.P. and S.S.; methodology, A.P. and S.S.; software, A.P. and T.K.; validation, A.P., T.K. and C.S.; formal analysis, A.P., S.S., P.P. and M.H.; investigation, A.P. and S.S.; resources, S.S.; data curation, A.P.; writing—original draft preparation, A.P. and S.S.; writing—review and editing, S.S., P.P. and M.H.; visualization, A.P. and T.K.; supervision, S.S.; project administration, S.S.; funding acquisition, S.S. All authors have read and agreed to the published version of the manuscript.

Funding: This research was partially supported by the Royal Golden Jubilee Ph.D. Program, grant number PHD02282560, and the Global and Frontier Research University Fund, Naresuan University, grant number R2567C002.

Data Availability Statement: The data presented in this study is available in the article.

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Renewables 2023-Analysis and Forecast to 2028. Available online: https://iea.blob.core.windows.net/assets/96d66a8b-d502-476b-ba94-54ffda84cf72/Renewables_2023.pdf (accessed on 4 February 2024).
2. Hu, J.; Li, Z.; Zhu, J.; Guerrero, J.M. Voltage Stabilization: A Critical Step Toward High Photovoltaic Penetration. *IEEE Ind. Electron. Mag.* **2019**, *13*, 17–30. [CrossRef]
3. IRENA. Innovation Landscape Brief: Utility-Scale Batteries. Available online: https://www.irena.org/-/media/Files/IRENA/Agency/Publication/2019/Sep/IRENA_Utility-scale-batteries_2019.pdf (accessed on 4 February 2024).
4. Riyaz, A.; Sadhu, P.K.; Iqbal, A.; Alamri, B. Comprehensive Survey of Various Energy Storage Technology Used in Hybrid Energy. *Electronics* **2021**, *10*, 2037. [CrossRef]
5. Ko, J.-S.; Huh, J.-H.; Kim, J.-C. Overview of Maximum Power Point Tracking Methods for PV System in Micro Grid. *Electronics* **2020**, *9*, 816. [CrossRef]
6. Ahmed, M.; Harbi, I.; Kennel, R.; Heldwein, M.L.; Rodríguez, J.; Abdelrahem, M. Performance Evaluation of PV Model-Based Maximum Power Point Tracking Techniques. *Electronics* **2022**, *11*, 2563. [CrossRef]
7. Galkin, I.A.; Blinov, A.; Vorobyov, M.; Bubovich, A.; Saltanovs, R.; Peftitsis, D. Interface Converters for Residential Battery Energy Storage Systems: Practices, Difficulties and Prospects. *Energies* **2021**, *14*, 3365. [CrossRef]
8. Cao, J.; Emadi, A. Batteries Need Electronics. *IEEE Ind. Electron. Mag.* **2011**, *5*, 27–35. [CrossRef]
9. Biao, Z.; Qiang, S.; Wenhua, L.; Yandong, S. Overview of Dual-Active-Bridge Isolated Bidirectional DC-DC Converter for High-Frequency-Link Power-Conversion System. *IEEE Trans. Power Electron.* **2014**, *29*, 4091–4106. [CrossRef]

10. Somkun, S.; Sato, T.; Chunkag, V.; Pannawan, A.; Nunocha, P.; Suriwong, T. Performance Comparison of Ferrite and Nanocrystalline Cores for Medium-Frequency Transformer of Dual Active Bridge DC-DC Converter. *Energies* **2021**, *14*, 2407. [CrossRef]
11. Lo Franco, F.; Morandi, A.; Raboni, P.; Grandi, G. Efficiency Comparison of DC and AC Coupling Solutions for Large-Scale PV+BESS Power Plants. *Energies* **2021**, *14*, 4823. [CrossRef]
12. Duracell Energy Bank. Available online: https://www.duracellenergybank.com/ (accessed on 4 February 2024).
13. What to Expect for Powerwall 3. Available online: https://www.tesla.com/support/energy/powerwall/learn/what-expect-powerwall-3 (accessed on 4 February 2024).
14. Kheraluwala, M.N.; Gascoigne, R.W.; Divan, D.M.; Baumann, E.D. Performance characterization of a high-power dual active bridge DC-to-DC converter. *IEEE Trans. Ind. Appl.* **1992**, *28*, 1294–1301. [CrossRef]
15. Jin, N.-Z.; Feng, Y.; Chen, Z.-Y.; Wu, X.-G. Bidirectional CLLLC Resonant Converter Based on Frequency-Conversion and Phase-Shift Hybrid Control. *Electronics* **2023**, *12*, 1605. [CrossRef]
16. Zhou, K.; Sun, Y. Research on Bidirectional Isolated Charging System Based on Resonant Converter. *Electronics* **2022**, *11*, 3625. [CrossRef]
17. Shu, L.; Chen, W.; Song, Z. Prediction method of DC bias in DC-DC dual-active-bridge converter. *CPSS Trans. Power Electron. Appl.* **2019**, *4*, 152–162. [CrossRef]
18. Wang, Z.; Chai, J.; Sun, X. Method to control flux balancing of high-frequency transformers in dual active bridge dc–dc converters. *J. Eng.* **2018**, *2018*, 1835–1843. [CrossRef]
19. Guzmán, P.; Vázquez, N.; Liserre, M.; Orosco, R.; Pinto Castillo, S.E.; Hernández, C. Two-Stage Modulation Study for DAB Converter. *Electronics* **2021**, *10*, 2561. [CrossRef]
20. Takagi, K.; Fujita, H. Dynamic Control and Performance of a Dual-Active-Bridge DC–DC Converter. *IEEE Trans. Power Electron.* **2018**, *33*, 7858–7866. [CrossRef]
21. Karimi-Ghartemani, M.; Khajehoddin, S.A.; Jain, P.; Bakhshai, A. A systematic approach to DC-bus control design in single-phase grid-connected renewable converters. *IEEE Trans. Power Electron.* **2013**, *28*, 3158–3166. [CrossRef]
22. Somkun, S.; Srita, S.; Kaewchum, T.; Pannawan, A.; Saeseiw, C.; Pachanapan, P. Adaptive Notch Filters for Bus Voltage Control and Capacitance Degradation Prognostic of Single-Phase Grid-Connected Inverter. *IEEE Trans. Ind. Electron.* **2023**, *70*, 12190–12200. [CrossRef]
23. Taghizadeh, S.; Karimi-Ghartemani, M.; Hossain, M.J.; Lu, J. A Fast and Robust DC-Bus Voltage Control Method for Single-Phase Voltage-Source DC/AC Converters. *IEEE Trans. Power Electron.* **2019**, *34*, 9202–9212. [CrossRef]
24. Pannawan, A.; Kaewchum, T.; Somkun, S.; Hinkkanen, M. Fast Bus Voltage Control of Single-Phase Grid-Connected Converter with Unified Harmonic Mitigation. *IEEE Access* **2023**, *11*, 6452–6466. [CrossRef]
25. Golestan, S.; Monfared, M.; Freijedo, F.D.; Guerrero, J.M. Dynamics assessment of advanced single-phase PLL structures. *IEEE Trans. Ind. Electron.* **2013**, *60*, 2167–2177. [CrossRef]
26. *TMS320F28004x Real-Time Microcontrollers-Technical Reference Manual*; Texas Instruments Incorporated: Dallas, TX, USA, 2022.
27. Kot, R.; Stynski, S.; Stepien, K.; Zaleski, J.; Malinowski, M. Simple technique reducing leakage current for H-bridge converter in transformerless photovoltaic generation. *J. Power Electron.* **2016**, *16*, 153–162. [CrossRef]
28. De Doncker, R.W.A.A.; Divan, D.M.; Kheraluwala, M.H. A three-phase soft-switched high-power-density DC/DC converter for high-power applications. *IEEE Trans. Ind. Appl.* **1991**, *27*, 63–73. [CrossRef]
29. *Ferrites and Accessories SIFERRIT Material N87*; EPCOS AG: Heidenheim, Germany, 2006.
30. Erickson, R.W.; Maksimovic, D. *Fundamentals of Power Electronics*, 2nd ed.; Kluwer Academic: New York, NY, USA, 2001.
31. Gierczynski, M.; Grzesiak, L.M.; Kaszewski, A. A Dual Rising Edge Shift Algorithm for Eliminating the Transient DC-Bias Current in Transformer for a Dual Active Bridge Converter. *Energies* **2021**, *14*, 4264. [CrossRef]
32. Tomasov, M.; Kajanova, M.; Bracinik, P.; Motyka, D. Overview of Battery Models for Sustainable Power and Transport Applications. *Transp. Res. Procedia* **2019**, *40*, 548–555. [CrossRef]
33. Sadhukhan, C.; Mitra, S.K.; Bhattacharyya, S.; Almatrafi, E.; Saleh, B.; Naskar, M.K. Modeling and simulation of high energy density lithium-ion battery for multiple fault detection. *Sci. Rep.* **2022**, *12*, 9800. [CrossRef] [PubMed]
34. Åström, K.J.; Hägglund, T. *PID Controllers: Theory, Design, and Tuning*, 2nd ed.; ISA: Durham, NC, USA, 1995.