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Asymmetric GaN High Electron Mobility Transistors Design with InAlN Barrier at Source Side and AlGaN Barrier at Drain Side

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Abstract: The InAlN/GaN HEMT has been identified as a promising alternative to conventional AlGaN/GaN HEMT due to its enhanced polarization effect contributing to higher 2DEG in the GaN channel. However, the InAlN barrier usually suffers from high leakage and therefore low breakdown voltage. In this paper, we propose an asymmetrical GaN HEMT structure which is composed of an InAlN barrier at the source side and an AlGaN barrier at the drain side. This novel device combines the advantages of high 2DEG density at the source side and low electrical-field crowding at the drain side. According to the TCAD simulation, the proposed asymmetric device exhibits better drain current and transconductance compared to AlGaN/GaN HEMT, and enhanced breakdown voltage compared to InAlN/GaN HEMT. The current collapse effects have also been evaluated from the process-related point of view. Possible higher interface traps related to the two-step epitaxial growth for the asymmetric structure fabrication will not exacerbate the current collapse and reliability.

Keywords: AlGaN/GaN HEMTs; InAlN/GaN HEMTs; asymmetric structure; TACD simulation; GaN HEMTs

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1. Introduction

Over the years, GaN high electron mobility transistors (HEMTs) have been widely used in high-frequency and high-power applications due to the fascinating physical properties of GaN, such as a wide bandgap, high critical electric field, high electron mobility and high saturation velocity [1–3]. These properties make GaN HEMTs ideal for use in power electronics applications in which a high voltage and current are required. For conventional materials, the free charges come from the impurity ionization. In GaN HEMTs, the polarization effects give rise to a high density of electron gas even without intentional doping [4]. The reported power density of GaN HEMTs is already impressive, reaching as high as 51 W/mm [5–8]. However, power density scaling with drain voltage alone becomes limiting, which negatively impacts the frequency application of these devices, since it is dominated by the saturation current [9]. To overcome this limitation and increase power densities at millimeter-wave frequencies, increasing the transistor current density and operating voltage is required. The challenge is to engineer a device that simultaneously supports both a high channel charge density and a high breakdown voltage. Engineers must work to improve GaN HEMTs to meet the needs of high-frequency and high-power applications. By increasing both the current density and the operating voltage, they can continue to push the limits of these devices and unlock even more potential for their use in the future.

The spontaneous polarization of GaN and AlGaN and the piezoelectric polarization induced by the strain of the lattice mismatch between AlGaN and GaN can induce two-dimensional electron gas (2DEG) at a volume as high as 1×10^{13} cm^{-2} with careful Al composition and thickness engineering. The lattice mismatch refers to the difference in the

spacing between atoms in the crystal lattices of two materials. When the lattice constants of two materials are significantly different, the atoms in one material cannot perfectly align with the atoms in the other material, causing strain in the crystal structure. As Al alloy fraction increases, so does the lattice mismatch with GaN, resulting in limitations on barrier thickness to avoid strain-relaxation-related cracking and reliability problems [10,11]. To avoid such cracking and ensure reliability, there are limits on the thickness of the barrier layer in GaN-based devices. The barrier layer is designed to separate different layers within the transistor structure and provide efficient electron confinement. However, due to the lattice mismatch, there is a maximum thickness beyond which the strain becomes too significant, increasing the likelihood of cracking.

InAlN, as another barrier material, can be lattice-matched to GaN and therefore avoids critical thickness issues. This allows the 2DEG channel density to be mainly induced by spontaneous polarization [12,13]. This polarization effect enhances the device's performance in terms of drain current and transconductance. Figure 1 illustrates the variation of the 2DEG concentration in AlGaN/GaN and InAlN/GaN HEMTs as a function of barrier thicknesses [14,15] at different alloy fractions (X). Despite the absence of piezo polarization, the 2DEG-channel sheet charge density in InAlN/GaN HEMTs is three times that of AlGaN/GaN HEMTs, which potentially leads to a higher output current and power density.

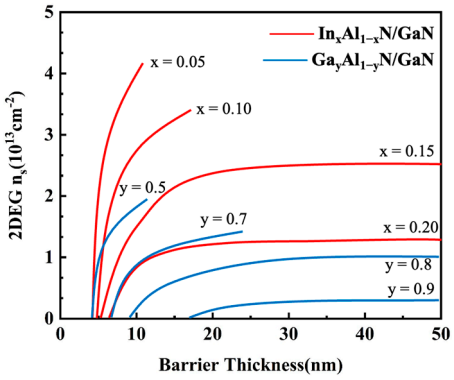


Figure 1. Two-dimensional electron gas (2DEG) density (ns) versus barrier thickness at different alloy compositions for InAlN/GaN HEMTs and GaAlN/GaN HEMTs.

However, one significant drawback of InAlN/GaN HEMTs is their susceptibility to large leakage currents, which is primarily caused by the high electric field near the gate edge towards the drain side. This high electric field intensity at the gate edge leads to a crowding phenomenon, which can result in premature breakdown and compromise the device's reliability. Compared to AlGaN/GaN HEMTs, InAlN/GaN HEMTs typically exhibit lower breakdown voltages. This limitation poses a challenge for their application in ultra-high power scenarios in which both a high drain current and high breakdown voltage are crucial requirements [16].

In order to make up for the shortcomings of low breakdown voltage while using InAlN's polarization advantage, this paper proposes an asymmetric GaN HEMT structure. That is, an $In_{0.17}Al_{0.83}N$/GaN structure is used in the source-to-gate side while an $Al_{0.25}Ga_{0.75}N$/GaN structure is used in the gate-to-drain side. This represents the first time such a configuration has been proposed, and the aim is to engineer a device that simultaneously supports both a high current density and a high operating voltage (or breakdown voltage) for ultra-high-power applications. The influences of the new structure on the performances of the HEMTs are compared theoretically. The results indicate that this novel device combines the advantages of AlGaN/GaN HEMTs and InAlN/GaN HEMTs. According to the TCAD simulation, the proposed asymmetric device exhibits a better drain current, transconductance and enhanced breakdown voltage compared to the conventional HEMTs.

2. Device Description and Physical Models

Two-dimensional physics-based simulation is used to simulate the electrical performances of the proposed device, which is compared with the standard symmetric devices. Figure 2a,b illustrate the schematics of the standard symmetric devices which are composed of the same GaN buffer and 20 nm $Al_{0.25}Ga_{0.75}N$ barrier and 10 nm $In_{0.17}Al_{0.83}N$ barrier on top of the GaN layer, respectively. Compared with the conventional structures, the schematic of the proposed asymmetric GaN device is illustrated in Figure 2c. It is composed of the GaN buffer on top of the SiC substrate, and a 10 nm thick $In_{0.17}Al_{0.83}N$ barrier layer at the source–gate side and a 20 nm thick $Al_{0.25}Ga_{0.75}N$ barrier layer at the gate–drain side. The gate electrode is situated on top of the $In_{0.17}Al_{0.83}N$ barrier. Ohmic contacts are formed in the source and drain terminals among the above three structures. The distances of gate–source, gate–drain, and length of the gate are 1 µm, 3.55 µm and 0.45 µm, respectively. The specific schematic diagram is shown in Figure 2c. The device's surface is passivated by using Si_3N_4 thin film to reduce the current collapse effect in the HEMTs [17].

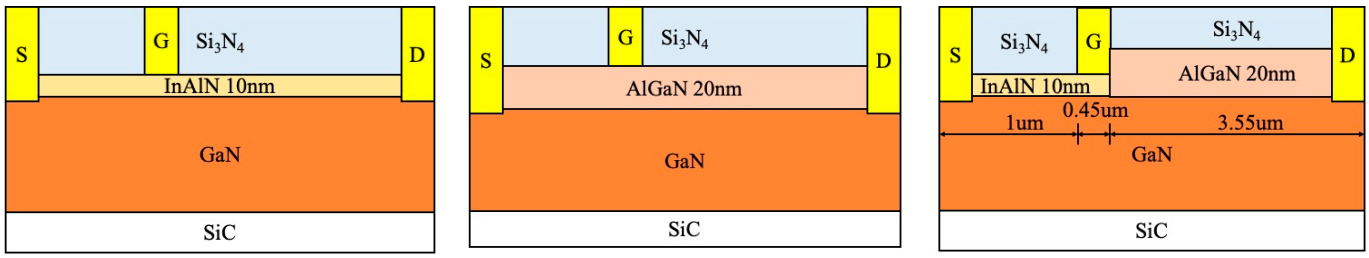


Figure 2. Cross-sectional views of three different structures: (**a**) The $In_{0.17}Al_{0.83}N$/GaN HEMTs with 10 nm InAlN barrier; (**b**) the $Al_{0.25}Ga_{0.75}N$/GaN HEMTs with 20 nm AlGaN barrier; (**c**) asymmetric GaN HEMTs with 10 nm InAlN barrier at the source–gate side and 20 nm AlGaN barrier at the gate–drain side.

The TCAD simulation take consideration of a comprehensive set of physical models, including Shockley–Read–Hall (SRH), Fermi–Dirac, Polarization (spontaneous polarization and piezoelectric polarization) as well as ionization for device simulation [18]. The physical parameters of GaN, AlN and InN during the simulation are shown in Table 1 [19]. To assess the impact of current collapse and distinguish the effect of source and drain on device reliability, trap and inttrap models are employed to simulate the consequences of buffer layer and interface defects on device performance, respectively. Traps and interface traps are also employed to simulate the consequences of buffer layer and interface defects on device performance, respectively. The parameters of traps and interface traps are shown in Table 2 [20,21].

Table 1. Parameters of GaN, AlN, InN in the simulation.

Parameters	GaN	AlN	InN
Bandgap, E_g (eV)	3.4	6.2	0.7
Dielectric constant, ε	9.0	8.5	15.3
Electron mobility (cm^2/Vs)	1250	500	3280
Saturation velocity (10^7 cm/s)	2.50	0.02	4.30
Electron affinity (eV)	1.84	1.45	4.70
Effective electron mass (m_0)	0.20	0.48	0.06
Thermal conductivity	1.3	2.0	0.8

Table 2. Parameters of buffer and interface traps in the simulation.

Parameters	Value
Buffer traps density (cm^{-3})	5×10^{18}
Buffer trap type, energy (eV)	Acceptor at 0.5 eV
Interface trap density (cm^{-2})	2×10^{12}
Interface type, energy (eV)	Acceptor at 0.8 eV

The bandgap of ternary compound depends on composition fraction x, which is usually approximated by [22,23]:

$$E_g(x) = xE_g(AlN) + (1-x)E_g(GaN) - bx(1-x) \quad (1)$$

$$E_g(x) = xE_g(AlN) + (1-x)E_g(InN) - bx(1-x) \quad (2)$$

where the deviation from a linear behavior is considered through the bowing parameter b.

The electron concentration is given by [24]:

$$\mathrm{n}(x,y) = 2\frac{k_B T}{\pi h^2}\sum_v \sqrt{m_x^v(x,y)m_z^v(x,y)}\sum_{i=0}^{\infty}|\psi_{iv}(x,y)|^2 \ln\left[1+\exp(-\frac{E_{iv}-E_F}{k_B T})\right] \quad (3)$$

where E_{iv} (x) is the eigen state energy at each electron valley v, φ_{iv} $(x,)$ is the wave function and $m_x^v(x,y)$ is the effective mass subject to spatial variation.

Considering the effect of material component and temperature, the general expression for the low field mobility that is typically used in drift-diffusion simulations is given as [24,25]:

$$\mu_0(T,N) = \mu_{min}(\frac{T}{300})^{\beta_1} + \frac{(\mu_{max}-\mu_{min})(\frac{T}{300})^{\beta_2}}{1+\left[\frac{N}{N_{ref}(\frac{T}{300}^{\beta_3})}\right]^{\alpha(T/300)^{\beta_4}}} \quad (4)$$

where T is the lattice temperature and N is the doping concentration.

The GANSAT model is adopted considering the unique polarization characteristics of the GaN device. This model enables the polarization effect; stress caused by lattice mismatch; carrier recombination; mobility effected by lattice temperature and doping concentration; and polarization.

The two mobility models have been used to consider various types of scattering mechanisms. The high field mobility model can be specified as shown below [19,26]:

$$\mu_n = \frac{\mu_{n0}(T,N) + v^{sat}\left(\frac{E^{n1-1}}{E_c^{n1}}\right)}{1 + a\left(\frac{E}{E_c}\right)^{n_2} + \left(\frac{E}{E_c}\right)^{n_1}} \quad (5)$$

where $\mu_{n0}(T,N)$ is the low field mobility, v^{sat} represents the saturation velocities and E is the electric field. The values of E_c, a_n, n_1 and n_2 can refer to [19].

The low field mobility model can be given by [24]:

$$\frac{1}{\mu} = a\left(\frac{N_I}{10^{17}\mathrm{cm}^{-3}}\right)\ln\left(1+\beta_{cw}^2\right)\left(\frac{T}{300\mathrm{K}}\right)^{-1.5} + b\left(\frac{T}{300\mathrm{K}}\right)^{-1.5} + \frac{c}{\exp\left(\frac{\Theta}{T}\right)-1} \quad (6)$$

where $\Theta = \frac{\hbar\omega_{LO}}{k_B} = 1065\mathrm{K}$, $\beta_{cw}^2 = 3\left(\frac{T}{300\mathrm{K}}\right)^2\left(\frac{N_\mathrm{I}}{10^{17}\mathrm{cm}^{-3}}\right)^{-1.5}$, $N_\mathrm{I} = (1+k_c)N_D$, $a = 2.61 \times 10^{-4}$ Vscm^{-2}, $b = 2.90 \times 10^{-4}$ Vscm^{-2} and $c = 1.70 \times 10^{-2}$ Vscm^{-2}. Here, N_D is the ionized donor concentration in cm^{-3}, T is the ambient temperature in Kelvin, and $k_c = N_A/N_D$ is the compensation ratio.

SRH recombination, also known as Shockley–Read–Hall recombination, is a process in which electrons and holes recombine through energy states associated with defects in the semiconductor material. This type of recombination can have a significant impact on the performance of electronic and optoelectronic devices. To explore the precise physical mechanism of electron trapping, it is necessary to calculate the electron trapping process associated with each trap level within the SRH recombination model. The SRH recombination rate is modeled using the standard expression [27,28]:

$$R_{SRH} = \frac{pn - n_i^2}{\tau_p\left(n + n_i \exp\left(\frac{E_{trap}}{kT}\right)\right) + \tau_n\left(p + n_i \exp\left(-\frac{E_{trap}}{kT}\right)\right)} \tag{7}$$

where τ_n and τ_p are the carrier lifetimes governed in turn by traps and the doping concentration, E_{trap} is the difference between the trap energy level and intrinsic Fermi level, n_i is the intrinsic carrier concentration and T is the lattice temperature.

In GaN-based devices, polarization plays a significant role due to the unique properties of this material. GaN exhibits spontaneous and piezoelectric polarizations, which can impact the performance of electronic devices. The total polarization-induced polarization charge density is given by [29]:

$$P_{total} = [P_{PE}(\text{bottom}) + P_{SP}(\text{bottom})] - [P_{PE}(top) + P_{SP}(\text{top})] \tag{8}$$

where P_{PE} and P_{SP} represent the piezoelectric polarization and spontaneous polarization, respectively.

Spontaneous polarizations of AlGaN/GaN HEMTs are linearly interpolated with Al content as follows [30]:

$$P_{SP}(x) = xP_{SP}(AlN) + (1 - x)P_{SP}(GaN) \tag{9}$$

Piezoelectric polarization in the c-axis direction can be determined by:

$$P_{PE}(x) = 2\frac{a - a_0(x)}{a_0(x)}\left[e_{31}(x) - e_{33}(x)\frac{C_{13}(x)}{C_{33}(x)}\right] \tag{10}$$

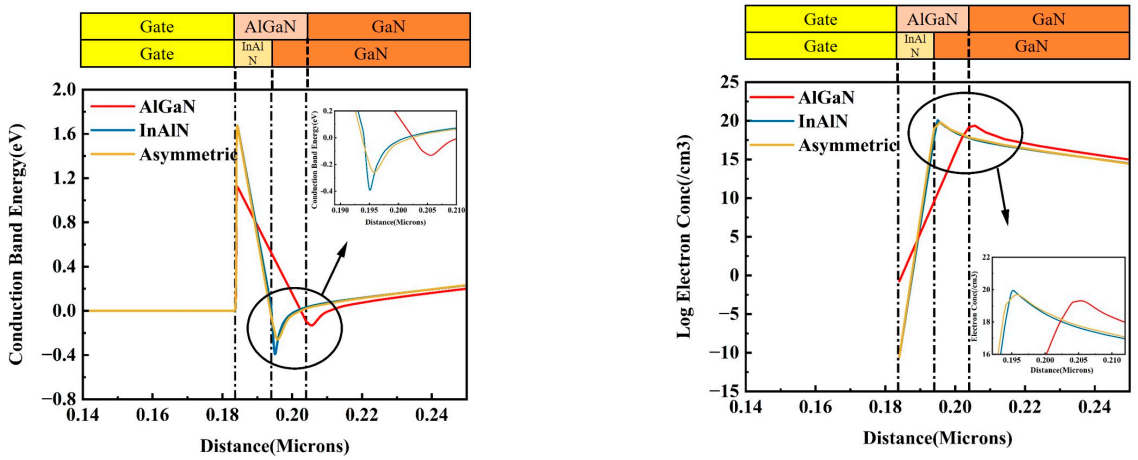
where a is the length of the hexagonal edge of a strained $Al_xGa_{1-x}N$ and $a_0(x)$ is the is the equilibrium length of the hexagonal edge of a nonstrained $Al_xGa_{1-x}N$, whose length is linearly interpolated with Al content x together with piezoelectric coefficients e_{ij} and elastic constants C_{ij} in the same way as estimated in (9).

To simply the simulation, diffusivity on the boundary between InAlN and AlGaN is not taken into account. Combining these models, we simulated the current transport characteristics and performed correlation analysis between the electron transport performance and device structures.

3. Results and Discussion

3.1. DC Characteristics

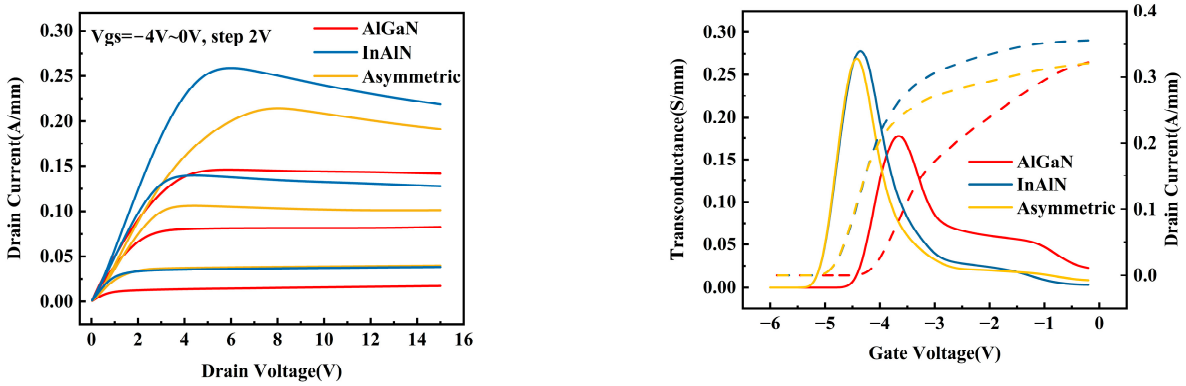
The asymmetric and symmetric devices are simulated using the same models and under the same conditions. The conduction band energy and electron concentration distribution diagrams for three different structures are presented in Figure 3a,b, extracted vertically from the gate electrode to GaN buffer cross-section, as shown in the upper part of the figure. It can be observed that asymmetric and InAlN/GaN HEMTs structures have a larger conduction band offset and therefore can polarize more carriers in the GaN channel, as shown in Figure 3b. The log electron concentration of the asymmetric device is similar to that of InAlN/GaN HEMTs and higher than that of AlGaN/GaN HEMTs (19.8 cm^{-3} vs. 19.4 cm^{-3}), as shown in the inserted figure in Figure 3a.



(**a**) (**b**)

Figure 3. (**a**) Conduction band energy distribution and (**b**) electron concentration distribution for AlGaN/GaN HEMTs, InAlN/GaN HEMTs and asymmetric GaN HEMTs.

The drain current versus drain voltage (IDVD) output characteristics and transfer characteristics (Gm) are highly related to the electron concentration, as illustrated in Figure 4a,b. In the IDVD output characteristics, gate voltage is scanned from −4 V to 0 V with a step of 2 V. The threshold voltages for the conventional AlGaN/GaN HEMTs, InAlN/GaN HEMTs, and asymmetric structures were −5 V, −5.2 V, and −5.2 V, respectively. There is a left shift of the Vth in InAlN and asymmetric barrier devices, which could be due to the thinner barrier thickness under the gate electrode and the higher 2DEG density. It is clear from the simulation results that the highest saturation current and transconductance were obtained for the InAlN barrier. In comparison, the AlGaN barrier exhibited a peak Gm value of about 35% lower than that of the InAlN barrier (177 mS/mm vs. 273 mS/mm) due to larger gate-to-channel distance, and an IDVD output current of about 44% lower than that of the InAlN devices (1460 mA/mm vs. 2600 mA/mm), which is related to the lower 2DEG in the GaN channel (19.4 cm^{-3} vs. 20.1 cm^{-3}) as depicted in Figure 3b. The transconductance of the asymmetric barrier is close to that of the InAlN barrier due to the same gate-to-channel distance, while the saturation current is slightly lower than in InAlN/GaN HEMTs but much higher than in AlGaN/GaN HEMTs due to its 2DEG density, which is in between that of the AlGaN and InAlN barriers.



(**a**) (**b**)

Figure 4. (**a**) IDVD (drain current versus drain voltage) output characteristics and (**b**) Transfer characteristics and IDVG (drain current versus gate voltage) for AlGaN/GaN HEMTs, InAlN/GaN HEMTs and asymmetric GaN HEMTs.

Although the InAlN HEMT structure offers significant benefits in terms of output drain current and transconductance, it is found through breakdown voltage simulation that it is most likely to break down (50.2 V vs. 580.5 V). Figure 5 shows the breakdown voltage (BV) characteristics of GaN HEMTs with different structures. During the simulation, the gate is biased at the off-state, and the drain voltages gradually increase until they reach drain current compliance of 1 mA/mm. It can be seen that the breakdown voltages of AlGaN barrier devices and asymmetric structures are much higher than those of InAlN barrier devices. The drain current starts to increase straight forward at VD about 50 V for the InAlN device, while the current starts to increase steeply at about 580 V and 575 V for the AlGaN and asymmetric devices separately. To investigate the breakdown phenomenon, electric fields are extracted along the source–drain cutline both in the barrier and in the channel for three devices to study their impact on the breakdown voltage.

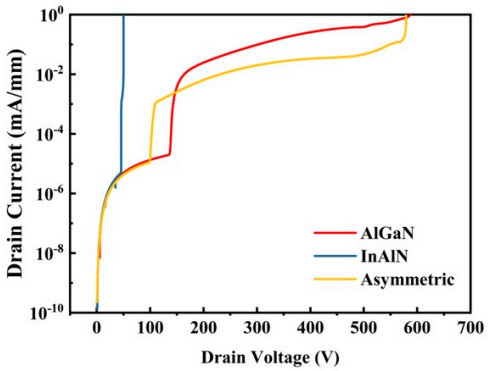


Figure 5. The reverse breakdown voltage for AlGaN/GaN HEMTs, InAlN/GaN HEMTs and asymmetric GaN HEMTs.

Figure 6 demonstrates the electrical field distribution at the breakdown point for each structure (once the devices have reached the compliance current 1 mA/mm). As can be seen, all the devices have a peak electric field at the gate edge towards the drain side both in the barrier and in the channel. This observation suggests that there is an electric field crowding phenomenon at the gate edge, which can have significant implications for device reliability and breakdown behaviour. And the peak electric field is the highest for InAlN/GaN HEMTs, which can explain the early breakdown of the device. The magnified section is shown in Figure 6. The electric field crowding with an electric field peak always happens at the gate edge closest to the drain, and the breakdown voltage can be improved if the crowding phenomenon can be mitigated.

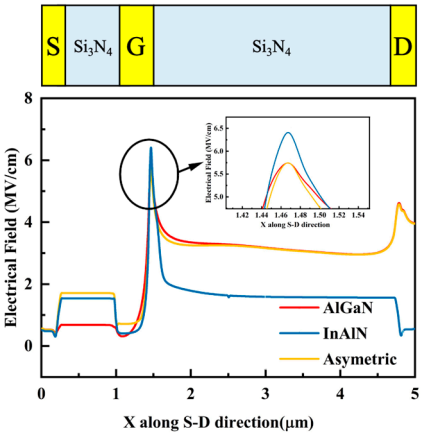
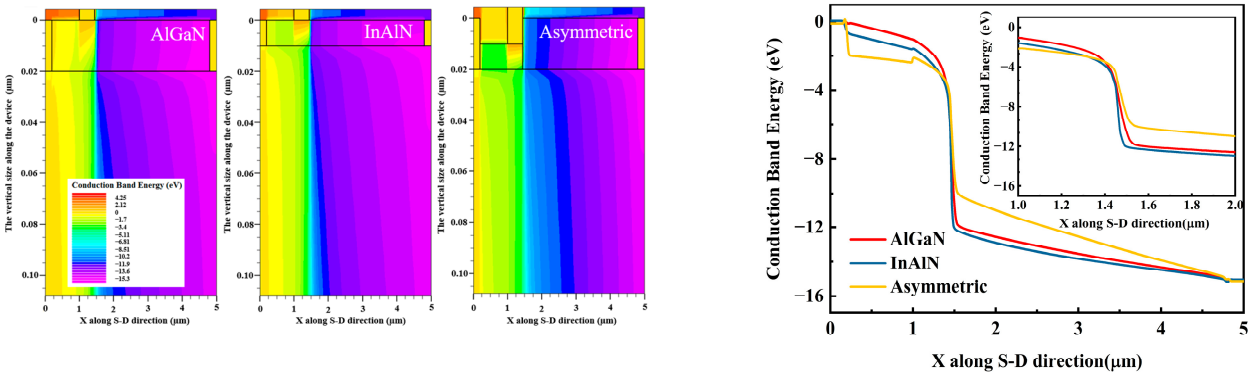


Figure 6. Electrical field distribution diagrams for AlGaN/GaN HEMTs, InAlN/GaN HEMTs and asymmetric GaN HEMTs.

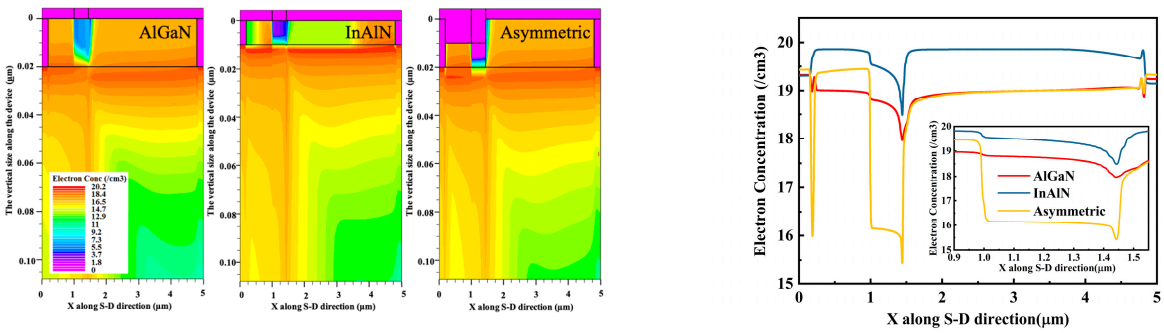
Figure 7a,b illustrate the conduction band energy of three different structures, including the conventional $Al_{0.25}Ga_{0.75}N$/HEMTs, $In_{0.17}Al_{0.83}N$/GaN HEMTs and the asymmetric HEMTs. It can be observed that when using the asymmetric HEMTs, the depletion region is enlarged both in the barrier and in the channel at the gate edge towards the drain side. This enlarged depletion region has the potential to mitigate the electric field crowding effect near the gate edge, which is a significant concern. This enlarged depletion region might be related to the different electron affinity between the $In_{0.17}Al_{0.83}N$ barrier layer and the $Al_{0.25}Ga_{0.75}N$ barrier layer. The enlarged depletion region in the asymmetric device also impacts the electron concentration in the channel. Understanding the relationship between the enlarged depletion region, electron affinity, and channel electron concentration is essential for optimizing the design and functionality of such devices.



(**a**) (**b**)

Figure 7. (**a**) Conduction band energy distribution and (**b**) its cutline plane distribution of AlGaN/GaN HEMTs, InAlN/GaN HEMTs and asymmetric GaN HEMTs at the on state.

In Figure 8a,b, the logarithm of the electron concentration in the channel is depicted, revealing a significant reduction in the electron concentration at the gate edge for the asymmetric device. This observed decrease in electron concentration is advantageous as it contributes to the relief of electrical field crowding at the gate edge. By mitigating electrical field crowding, this effect can help improve the overall performance and reliability of the device by minimizing the undesirable effects associated with high electrical field strengths. Furthermore, understanding and controlling the distribution of electron concentration in the channel is crucial for optimizing the behavior and characteristics of the device in practical applications.



(**a**) (**b**)

Figure 8. (**a**) Log electron concentration and (**b**) its cutline plane distribution of AlGaN/GaN HEMTs, InAlN/GaN HEMTs and asymmetric GaN HEMTs at the on state.

The reduced breakdown voltage of the InAlN/GaN HEMTs can also be attributed to gate leakage. Therefore, investigations of gate leakage have been carried out for three different structures. As depicted in Figure 9, gate leakage current is extracted at reverse gate bias from 0 V to −20 V. The results show that the InAlN/GaN HEMTs have significantly higher gate leakage compared to the AlGaN/GaN HEMTs (more than one order of magnitude difference), which on the one hand is due to their thin barrier thickness, and on the other hand is due to the tunneling probability of InAlN material being significantly higher than that of AlGaN material. This will cause the gate leakage current to increase and the device breakdown voltage to decrease. Interestingly, the overall gate leakage of the asymmetric structure is slightly lower even with the same thin InAlN barrier under the gate. We speculate that this could be due to mirror force mitigation, which is highly related to the electron concentration. As discussed in the previous part, the electron concentration has been highly reduced at the gate edge using asymmetric barrier; therefore the mirror force is reduced. Hence, the tunneling probability is also reduced.

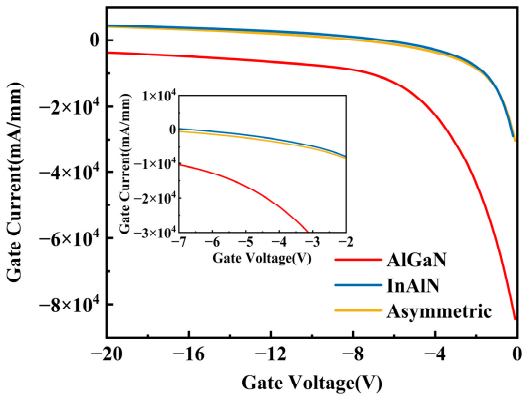
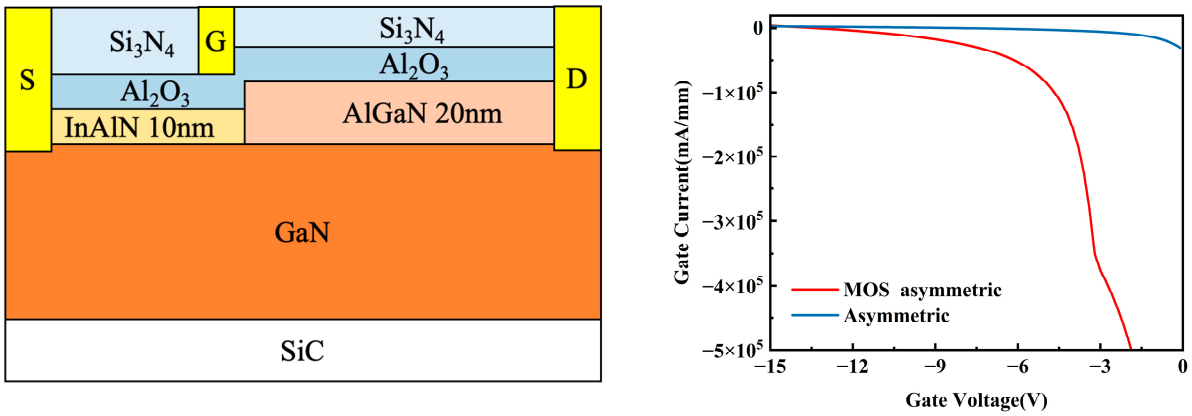


Figure 9. The gate leakage under gate voltage for AlGaN/GaN HEMTs, InAlN/GaN HEMTs and asymmetric GaN HEMTs.

Aluminum oxide (Al_2O_3) is a type of dielectric material that can be utilized as a gate dielectric layer in MOS (metal-oxide semiconductor) structures to further reduce the gate leakage current. MOS structures are widely used in integrated circuits and other electronic devices due to their ability to provide a high degree of control over the flow of current through the device. When Al_2O_3 is added as the gate dielectric layer in an MOS structure, it provides a higher level of insulation than SiO_2, thereby minimizing current leakage. This is because Al_2O_3 has a higher dielectric constant than SiO_2, which means that it can store more electric charge per unit area.

The cross-sectional diagram of an MOS structure in Figure 10a shows the different layers that make up the device, including the gate electrode, the Al_2O_3 dielectric layer, and the channel region. The simulation results in Figure 10b demonstrate that the gate leakage of MOS asymmetric structures with Al_2O_3 decreased significantly compared to structures without it. Specifically, the insertion of Al_2O_3 reduced gate leakage by five orders of magnitude, which is a significant improvement.

Overall, the use of Al_2O_3 as a gate dielectric layer in MOS structures is an important development in the field of electronics. It has the potential to enhance the performance of integrated circuits and other electronic devices by reducing gate leakage and improving device reliability.



(**a**) (**b**)

Figure 10. (**a**) A cross-sectional view of MOS asymmetric structure and (**b**) the gate leakage under gate voltage for MOS asymmetric structure.

3.2. Reliability

The novel asymmetric structure has been shown to have a good balance between high drain current and breakdown voltage from TCAD simulation. To fabricate this structure, a two-step epitaxial growth process is employed. The first step involves the growth of an AlGaN barrier layer along with the whole structure. In the second step, InAlN is grown after the AlGaN layer is selectively etched at the source side. This etching process introduces the potential for inconsistent source and drain interface defects. Therefore, it is necessary to evaluate the impact of defect density on the source side and drain side separately.

As shown in Figure 11, three AlGaN/GaN HEMTs are defined with different interface trap setups, which all have the same concentration of 2×10^{12} cm^{-2}. Structure A has only source interface traps, which are acceptor-like traps at 0.8 eV. Structure B has only drain interface traps of the same type. Structure C has interface traps both at the source and drain. By separately investigating the position where the interface traps have the most impact, potential current collapse due to second epitaxial growth can be estimated. The quiescent bias is at VGQ = 0 V and VDQ = 5 V, and the devices are stressed at VG = −8 V and VD = 25 V for 1 ms, and then return to the quiescent state, as shown in Figure 12a. According to the simulation results as shown in Figure 12b, after only 1 ms of bias stress, the drain current is significantly reduced, demonstrating the current collapse phenomenon. By comparing three different structures, drain interface defects play a dominant role in current collapse effects. Considering only drain interface defects, the current collapse is 23.1%. Considering only source interface defects, the current collapse is 10.8%. Considering both source and drain interface defects at the same time, the current collapse is 30.8%. The current collapse is calculated by the equation below:

$$Current\ Collapse(\%) = \frac{I_{Pre-Stress} - I_{Post-Stress}}{I_{Pre-Stress}} \times 100\% \quad (11)$$

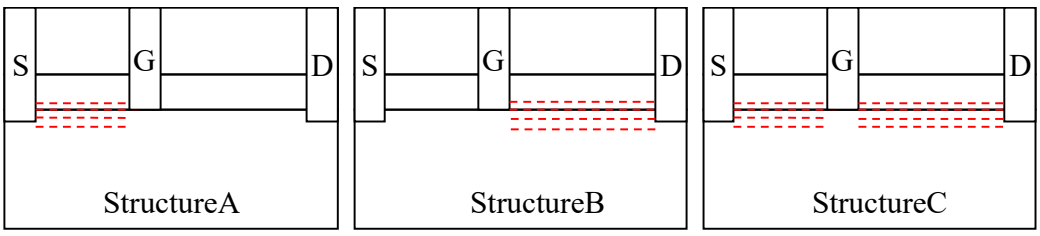
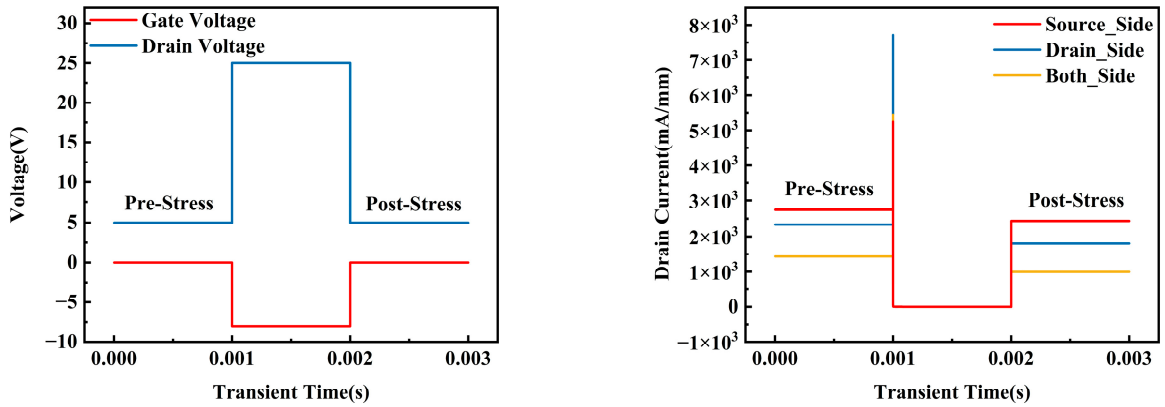


Figure 11. Schematic diagram of traps in different locations.



(**a**) (**b**)

Figure 12. (**a**) Voltage setup and (**b**) current collapse for AlGaN/GaN HEMTs, InAlN/GaN HEMTs and asymmetric GaN HEMTs.

Therefore, drain interface quality has a more significant impact on current collapse effects. For the realization of the asymmetric structure, the drain heterojunction structure AlGaN/GaN is standardly formed by the first epitaxial growth. The interface defect can be most effectively improved by in situ SiN passivation or LPCVD SiN passivation. The source heterojunction structure InAlN/GaN can be formed by etching and epitaxial regrowth. This additional etching and regrowth process may bring potential extra interface defects to the source side. However, according to simulations, defect density at the source-side does not affect current collapse as significantly as defects at the drain side. Through careful surface treatment before regrowth and the growth condition engineering, it is expected that we will reduce interface defects at the source side. Besides, further research is still needed to investigate the reliability and defects of the devices under various bias stress and temperature conditions [31,32].

4. Conclusions

AlGaN/GaN and InAlN/GaN HEMTs are widely developed for high-frequency and high-power applications. Device electrical performances can be tuned through barrier layer engineering techniques such as alloy fraction composition and thickness. InAlN/GaN HEMTs are expected to exhibit higher drain current and transconductance than AlGaN/GaN HEMTs due to higher 2DEG induced by InAlN's effective polarization. However, high leakage current and low breakdown voltages have limited their application in ultra-high-power applications.

To solve the contradictory problem between high drain current and high breakdown voltage, novel asymmetric structures with an InAlN source barrier and an AlGaN drain barrier have been proposed, which can combine the advantages of traditional InAlN/GaN HEMTs and AlGaN/GaN HEMTs. This innovative structure offers superior performance relative to its traditional counterparts, demonstrating not only high-output drain current and transconductance but also excellent breakdown voltage, which can be potentially applied to ultra-high-power applications.

On the other hand, we simulate the impact of defect density on the source side and drain side separately. The simulations indicate that the defect density on the source side does not have as significant an impact on current collapse as defects on the drain side. Moreover, by implementing surface treatment before regrowth, it is anticipated that interface defects on the source side can be reduced. As a result, the asymmetric device can be realized without compromising the device's reliability.

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References

1. Asif Khan, M.; Chen, Q.; Shur, M.S.; Dermott, B.T.; Higgins, J.A.; Burm, J.; Schaff, W.J.; Eastman, L.F. CW Operation of Short-Channel GaN/AlGaN Doped Channel Heterostructure Field Effect Transistors at 10 GHz and 15 GHz. *IEEE Electron Device Lett.* **1996**, *17*, 584–585. [CrossRef]
2. Mishra, U.K.; Shen, L.; Kazior, T.E.; Wu, Y.-F. GaN-Based RF Power Devices and Amplifiers. *Proc. IEEE* **2008**, *96*, 287–305. [CrossRef]
3. Mishra, U.K.; Parikh, P.; Wu, Y.-F. AlGaN/GaN HEMTs-an Overview of Device Operation and Applications. *Proc. IEEE* **2002**, *90*, 1022–1031. [CrossRef]
4. Zeng, F.; An, J.X.; Zhou, G.; Li, W.; Wang, H.; Duan, T.; Jiang, L.; Yu, H. A Comprehensive Review of Recent Progress on GaN High Electron Mobility Transistors: Devices, Fabrication and Reliability. *Electronics* **2018**, *7*, 377. [CrossRef]
5. Leoni, R.; Kolias, N.; Jablonski, P.; Altunkilic, F.; Johnson, E.; Bourcy, W. Raytheon High Power Density GaN Technology. In Proceedings of the 2017 IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS), Miami, FL, USA, 22–25 October 2017; pp. 1–4.
6. Wu, Y.-F.; Moore, M.; Saxler, A.; Wisleder, T.; Parikh, P. 40-W/Mm Double Field-Plated GaN HEMTs. In Proceedings of the 2006 64th Device Research Conference, State College, PA, USA, 26–28 June 2006; pp. 151–152.
7. Wu, Y.-F.; Saxler, A.; Moore, M.; Smith, R.P.; Sheppard, S.; Chavarkar, P.M.; Wisleder, T.; Mishra, U.K.; Parikh, P. 30-W/Mm GaN HEMTs by Field Plate Optimization. *IEEE Electron Device Lett.* **2004**, *25*, 117–119. [CrossRef]
8. Ohki, T.; Yamada, A.; Minoura, Y.; Makiyama, K.; Kotani, J.; Ozaki, S.; Sato, M.; Okamoto, N.; Joshin, K.; Nakamura, N. An Over 20-W/Mm S-Band InAlGaN/GaN HEMT With SiC/Diamond-Bonded Heat Spreader. *IEEE Electron Device Lett.* **2019**, *40*, 287–290. [CrossRef]
9. Karmalkar, S.; Mishra, U.K. Very High Voltage AlGaN/GaN High Electron Mobility Transistors Using a Field Plate Deposited on a Stepped Insulator. *Solid-State Electron.* **2001**, *45*, 1645–1652. [CrossRef]
10. Feng, Y.; Saravade, V.; Chung, T.-F.; Dong, Y.; Zhou, H.; Kucukgok, B.; Ferguson, I.T.; Lu, N. Strain-Stress Study of AlxGa1−xN/AlN Heterostructures on c-Plane Sapphire and Related Optical Properties. *Sci. Rep.* **2019**, *9*, 10172. [CrossRef]
11. Arulkumaran, S.; Egawa, T.; Ishikawa, H.; Jimbo, T. Characterization of Different-Al-Content AlxGa1−xN/GaN Heterostructures and High-Electron-Mobility Transistors on Sapphire. *J. Vac. Sci. Technol. B Microelectron. Nanometer Struct. Process. Meas. Phenom.* **2003**, *21*, 888–894. [CrossRef]
12. Kohn, E.; Medjdoub, F. InAlN—A New Barrier Material for GaN-Based HEMTs. In Proceedings of the 2007 International Workshop on Physics of Semiconductor Devices, Mumbai, India, 16–20 December 2007; pp. 311–316.
13. Gonschorek, M.; Carlin, J.-F.; Feltin, E.; Py, M.A.; Grandjean, N. High Electron Mobility Lattice-Matched AlInN/GaN Field-Effect Transistor Heterostructures. *Appl. Phys. Lett.* **2006**, *89*, 062106. [CrossRef]
14. Ambacher, O.; Christian, B.; Yassine, M.; Baeumler, M.; Leone, S.; Quay, R. Polarization Induced Interface and Electron Sheet Charges of Pseudomorphic ScAlN/GaN, GaAlN/GaN, InAlN/GaN, and InAlN/InN Heterostructures. *J. Appl. Phys.* **2021**, *129*, 204501. [CrossRef]
15. Kazior, T.E.; Chumbes, E.M.; Schultz, B.; Logan, J.; Meyer, D.J.; Hardy, M.T. High Power Density ScAlN-Based Heterostructure FETs for Mm-Wave Applications. In Proceedings of the 2019 IEEE MTT-S International Microwave Symposium (IMS), Boston, MA, USA, 2–7 June 2019; pp. 1136–1139.
16. Zhou, Y.; Zhu, J.; Mi, M.; Zhang, M.; Wang, P.; Han, Y.; Wu, S.; Liu, J.; Zhu, Q.; Chen, Y.; et al. Analysis of Low Voltage RF Power Capability on AlGaN/GaN and InAlN/GaN HEMTs for Terminal Applications. *IEEE J. Electron Devices Soc.* **2021**, *9*, 756–762. [CrossRef]
17. Prunty, T.R.; Smart, J.A.; Chumbes, E.N.; Ridley, B.K.; Eastman, L.F.; Shealy, J.R. Passivation of AlGaN/GaN Heterostructures with Silicon Nitride for Insulated Gate Transistors. In Proceedings of the 2000 IEEE/ Cornell Conference on High Performance Devices, Ithaca, NY, USA, 7–9 August 2000; pp. 208–214, Cat. No. 00CH37122.
18. Frayssinet, E.; Knap, W.; Lorenzini, P.; Grandjean, N.; Massies, J.; Skierbiszewski, C.; Suski, T.; Grzegory, I.; Porowski, S.; Simin, G.; et al. High Electron Mobility in AlGaN/GaN Heterostructures Grown on Bulk GaN Substrates. *Appl. Phys. Lett.* **2000**, *77*, 2551–2553. [CrossRef]
19. Gu, Y.; Chang, D.; Sun, H.; Zhao, J.; Yang, G.; Dai, Z.; Ding, Y. Theoretical Study of InAlN/GaN High Electron Mobility Transistor (HEMT) with a Polarization-Graded AlGaN Back-Barrier Layer. *Electronics* **2019**, *8*, 885. [CrossRef]

20. Marcon, D.; Viaene, J.; Favia, P.; Bender, H.; Kang, X.; Lenci, S.; Stoffels, S.; Decoutere, S. Reliability of AlGaN/GaN HEMTs: Permanent Leakage Current Increase and Output Current Drop. In Proceedings of the 20th IEEE International Symposium on the Physical and Failure Analysis of Integrated Circuits (IPFA), Suzhou, China, 15–19 July 2013; pp. 249–254.
21. Yi, B.; Xu, Y.; Cheng, J.; Huang, H.; Kong, M.; Yang, H. Investigation of a Novel Enhancement-Mode Al0.25Ga0.75N/AlN/Al X Ga(1-X)N/GaN MIS-HEMT for High Vth and Low R on,sp. *IEEE Trans. Electron Devices* **2023**, *70*, 3704–3710. [CrossRef]
22. Nunez-Gonzalez, R.; Reyes-Serrato, A.; Posada-Amarillas, A.; Galvan, D.H. First-Principles Calculation of the Band Gap of $Al_xGa_{1-x}N$ and $In_xGa_{1-x}N$. *Rev. Mex. Física* **2008**, *54*, 111–118.
23. Man Shrestha, N.; Li, Y.; Chang, E.Y. Simulation Study on Electrical Characteristic of AlGaN/GaN High Electron Mobility Transistors with AlN Spacer Layer. *Jpn. J. Appl. Phys.* **2014**, *53*, 04EF08. [CrossRef]
24. Ambacher, O.; Smart, J.; Shealy, J.R.; Weimann, N.G.; Chu, K.; Murphy, M.; Schaff, W.J.; Eastman, L.F.; Dimitrov, R.; Wittmer, L.; et al. Two-Dimensional Electron Gases Induced by Spontaneous and Piezoelectric Polarization Charges in N- and Ga-Face AlGaN/GaN Heterostructures. *J. Appl. Phys.* **1999**, *85*, 3222–3233. [CrossRef]
25. Neamen, D.A. *Semiconductor Physics and Devices: Basic Principles*, 4th ed.; McGraw-Hill: New York, NY, USA, 2012; ISBN 978-0-07-352958-5.
26. Farahmand, M.; Garetto, C.; Bellotti, E.; Brennan, K.F.; Goano, M.; Ghillino, E.; Ghione, G.; Albrecht, J.D.; Ruden, P.P. Monte Carlo Simulation of Electron Transport in the III-Nitride Wurtzite Phase Materials System: Binaries and Ternaries. *IEEE Trans. Electron Devices* **2001**, *48*, 535–542. [CrossRef]
27. Megherbi, M.L.; Pezzimenti, F.; Dehimi, L.; Saadoune, M.A.; Della Corte, F.G. Analysis of Trapping Effects on the Forward Current–Voltage Characteristics of Al-Implanted 4H-SiC p-i-n Diodes. *IEEE Trans. Electron Devices* **2018**, *65*, 3371–3378. [CrossRef]
28. Shockley, W.; Read, W.T. Statistics of the Recombinations of Holes and Electrons. *Phys. Rev.* **1952**, *87*, 835–842. [CrossRef]
29. Ambacher, O.; Majewski, J.; Miskys, C.; Link, A.; Hermann, M.; Eickhoff, M.; Stutzmann, M.; Bernardini, F.; Fiorentini, V.; Tilak, V.; et al. Pyroelectric Properties of Al(In)GaN/GaN Hetero- and Quantum Well Structures. *J. Phys. Condens. Matter* **2002**, *14*, 3399. [CrossRef]
30. Inoue, T.; Nakayama, T.; Ando, Y.; Kosaki, M.; Miwa, H.; Hirata, K.; Uemura, T.; Miyamoto, H. Polarization Engineering on Buffer Layer in GaN-Based Heterojunction FETs. *IEEE Trans. Electron Devices* **2008**, *55*, 483–488. [CrossRef]
31. Wang, P.F.; Li, X.; Zhang, E.X.; Jiang, R.; McCurdy, M.W.; Poling, B.S.; Heller, E.R.; Schrimpf, R.D.; Fleetwood, D.M. Worst-Case Bias for High Voltage, Elevated-Temperature Stress of AlGaN/GaN HEMTs. *IEEE Trans. Device Mater. Reliab.* **2020**, *20*, 420–428. [CrossRef]
32. Fleetwood, D.M.; Wang, P.F.; Zhang, E.X.; Schrimpf, R.D.; Pantelides, S.T. Defect Dehydrogenation in Si-MOS and Compound-Semiconductor-Based Devices. In Proceedings of the 2020 IEEE 15th International Conference on Solid-State & Integrated Circuit Technology (ICSICT), Kunming, China, 3–6 November 2020; pp. 1–4.