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# A Linear Multi-Band Voltage-Controlled Oscillator with Process Compensation for SerDes Applications

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**Abstract:** A new voltage-controlled oscillator (VCO) topology for serializer–deserializer (SerDes) applications is proposed in this paper. The topology is suitable for SATA, PCI Express, and USB 3 protocols. The VCO is based on two-ring oscillator cores and operates in several frequency bands, as required by the corresponding protocol specifications, with a constant VCO gain and improved linear control over the frequency tuning. Additionally, it is supported by an automatic digital compensation mechanism for process variations. The VCO has been designed to cover the several speeds of the SATA and PCI Express protocols, with optimized performance in all of them, including the current consumption, the phase noise, and the frequency tuning in each case. Designed in a CMOS 22 nm technology node with a 0.8 V supply voltage, it can achieve, at 3 GHz frequency, a phase noise better than −90 dBc/Hz at 1 MHz offset and an average power consumption equal to 3.84 mW. Extended digital control can set optimized configurations for phase noise, current consumption, and VCO gain vs. process variations. Extensive post-layout simulation results verify the superior performance.

**Keywords:** VCO; multi-band VCO; wide range VCO; PCIe; SATA; SerDes; frequency compensation; corner detection



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## 1. Introduction

Voltage-controlled oscillators (VCOs) are important circuits in wired and wireless communication systems, such as Bluetooth, Zigbee, WiFi, USB, SATA, PCI Express (PCIe), and others [1,2]. The continuous improvement of communication protocols sets demanding specifications in the design of VCO in terms of oscillation accuracy, power consumption, phase noise, and frequency tuning linearity. The layout area is also an important factor in lowering the total cost of the product. Therefore, ring VCOs are usually preferable compared to LC VCOs in terms of layout area utilization [3]. On the other hand, ring VCOs show worse phase noise than LC VCOs. Finally, the selection between the LC and the ring VCOs is a trade-off mostly between layout area, phase noise, and current consumption. According to these factors, the use of ring oscillators with improved phase noise is the preferred option to be included in communication systems. All types of VCOs must be able to operate in the frequency range defined by the specification, covering the process, voltage, and temperature (PVT) variations. In most cases, this is difficult to achieve with simple circuit configurations. While usually the voltage variations can be easily managed by supplying the oscillators with voltage regulators [4], the temperature and process variations require more complicated designs or additional control setups and calibrations [5,6]. Thus, regarding the temperature influence on the VCO operation, the performance of current steering oscillators could be compensated by using temperature-dependent current sources, e.g., proportional to absolute temperature (PTAT) or complementary to absolute temperature (CTAT), for temperature variation [6]. For process variation detection, more complicated methods must be employed, as the process corner is more difficult to detect automatically and, at the same time, produces a stronger influence on the oscillator performance. By detecting the

process corner, a compensation mechanism can be used to keep the oscillator performance within the specifications. As correct corner detection is not an easy task, such a mechanism is usually missing from most VCO designs, and only recently have some related attempts been proposed [7]. If the frequency range is not widely extended and, thus, there is no necessity for performance optimization at different frequencies, simple, low-cost designs can be used [8–10].

In some cases, a VCO is designed with specifications suitable for being employed in systems of different protocols if the different systems operate at similar data rates. For example, two such systems are SATA, PCIe, and USB. As depicted in Table 1, the SATA protocol specifies that the data rates are 6 Gb/s, 3 Gb/s, and 1.5 Gb/s for SATA 3.0, SATA 2.0, and SATA 1.0, respectively. Similarly, the PCIe protocol specifies that the data rates are 5 Gb/s and 2.5 Gb/s for PCIe 2.0 and PCIe 1.1, respectively. The USB 3.0 and 3.1 Gen 1 are also compatible with the PCIe 2.0, which operates at 5 Gb/s. In that case, a VCO covering the several protocols for these speeds can be designed to reduce the development cost of the final products. A method to change the frequency band of a ring oscillator is by enabling different numbers of delay elements, depending on the specific frequency band [11,12], but this design may not be optimized for every band. Another method is by using a high VCO gain, which, however, may develop high sensitivity to process and voltage variations and worsen the phase noise [11,13]. In [14], the supply voltage has been used to select frequency bands, but this is not optimized for each one of them.

**Table 1.** The data rates of some serial bus protocols.

| SATA | | PCIe | | USB | |
|---|---|---|---|---|---|
| **Version** | **Data Rate (Gb/s)** | **Version** | **Data Rate (Gb/s)** | **Version** | **Data Rate (Gb/s)** |
| 1.0 | 1.5 | - | - | - | - |
| 2.0 | 3 | 1.1 | 2.5 | - | - |
| 3.0 | 6 | 2.0 | 5 | 3.0<br>3.1 Gen 1 | 5 |

In this paper, a novel, wide-range ring VCO for SATA, PCIe, and USB protocols is proposed, with improved frequency tuning linearity and constant VCO gain Kvco over the total control voltage *Vctrl* range. The VCO operates at least from 0.75 GHz to 3 GHz, covering the frequency range required by the SATA, PCIe, and USB protocols. For optimized phase noise and current consumption in the overall frequency range, there are two main bands: the high frequency (HF) band and the low frequency (LF) band, generated by two corresponding ring VCOs. The HF band covers the clock frequencies of the corresponding versions at 2.5 GHz for USB and PCIe and 3 GHz for SATA. The LF band covers the clock frequencies of the corresponding versions at 1.25 GHz for PCIe and 0.75 GHz to 1.5 GHz for SATA, respectively. Furthermore, a new compensation mechanism is employed in this VCO topology for process variations through automatic process detection. The process detection mechanism proposed in this paper controls a resistor bank in the delay elements of the VCO to keep the oscillation frequency and the phase noise within the required range. The phase noise can also be improved in terms of the cost of current consumption without affecting other operation parameters.

In what follows, the proposed delay element and the compensation are presented in detail in Section 2, and the simulation results are presented in Section 3. The conclusions are provided in Section 4.

## 2. The Proposed VCO Topology

The proposed novel VCO is designed for SATA and PCIe systems and covers two main bands: the first in the high frequency (HF) range from 2.5 GHz (USB 3.0 and 3.1 Gen 1 and PCIe 2.0) to 3 GHz (SATA 3.0), and the second in the low frequency (LF) range from 0.75 GHz (SATA 1.0) to 1.25 GHz (PCIe 1.1) and 1.5 GHz (SATA 2.0), as shown in Table 2.

**Table 2.** The VCO operating frequencies.

| VCO \ Protocol | SATA | | PCIe | | USB | |
|---|---|---|---|---|---|---|
| | Version | Frequency (GHz) | Version | Frequency (GHz) | Version | Frequency (GHz) |
| LF | 1.0<br>2.0 | 0.75<br>1.5 | -<br>1.1 | -<br>1.25 | -<br>- | -<br>- |
| HF | 3.0 | 3 | 2.0 | 2.5 | 3.0<br>3.1 Gen 1 | 2.5 |

To achieve the best performance in both bands, two dedicated ring VCOs of the same architecture have been employed, and each one operates in a separate band. The cost paid for the two dedicated rings is the larger layout area, which is nevertheless shared by all other parts of the phase-locked loop (PLL), and they are too small compared with the overall layout of the rest of the PLL. The two VCOs have similar topologies, but each one is optimized for the best current consumption in each band. The outputs of the VCOs are driven through buffers to a multiplexer, as depicted in Figure 1. Each separate VCO topology is based on a similar four-stage ring topology, shown in Figure 2. This configuration offers a four-phase differential output with accurate phase differences.

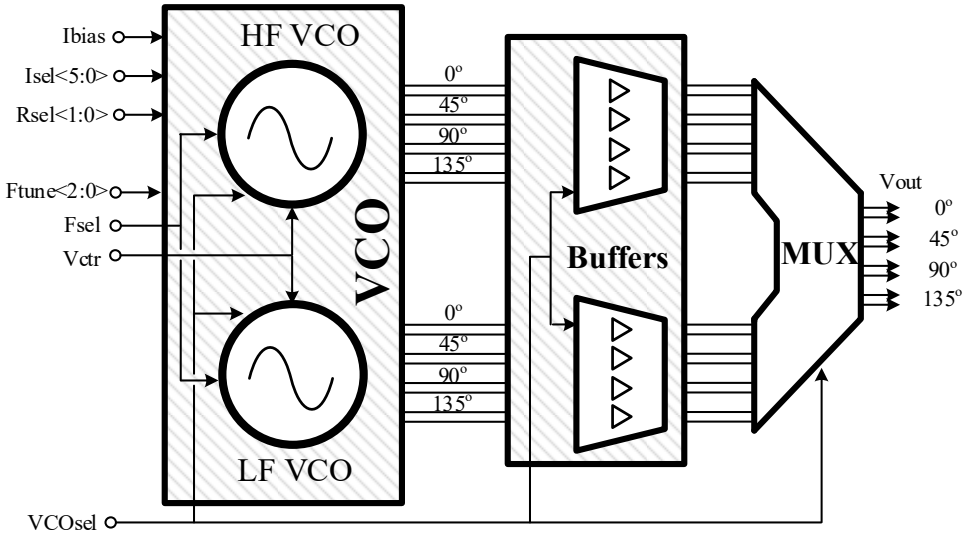



**Figure 1.** The two-band VCO topology.

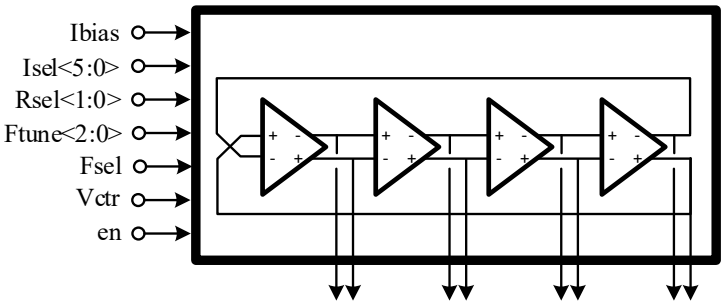



**Figure 2.** The four-stage ring VCO topology.

According to phase-locked loop (PLL) system noise analysis, including the noise contribution of all the sub-blocks in the loop, the target phase noise of the oscillator should be better than −90 dBc/Hz at 1 MHz offset in the higher operating frequency in order to meet the random jitter performance specified by the protocols. Also, the desired power consumption of the VCO has been extracted from the total PLL power consumption budget,

and for the HF bands, it should be less than 6 mW, while for the LF bands, it should be less than 4 mW.

### *2.1. The Delay Element*

The topology of the delay element for both VCOs, the HF-VCO and the LF-VCO, is shown in Figure 3. It is based on an NMOS differential pair with a combined load consisting of the passive resistors R1, R2, the PMOS transistor Mptune, and a pair of positive feedback cross-connected transistors Mp1. A key point in this design is that the transistor Mptune is actively involved in the frequency tuning together with the varactors, which finally improves the frequency linear control, and the Kvco is constant over the voltage range of *Vctrl*. The cross-connected PMOS transistors Mp1, through their positive feedback, ensure that the oscillation will start and remain under several tough bias conditions. When the additional resistors R2 are enabled or disabled by the transistor Mpsel, the oscillation frequency becomes 3 GHz (SATA 3.0) or 2.5 GHz (PCIe 2.0 and USB), respectively, in the case of the HF-VCO. In a corresponding way, for the LF-VCO frequency with the R2 enabled, the oscillation frequency is 1.5 GHz (SATA 2.0) and 1.25 GHz (PCIe 1.1); otherwise, it is 0.75 GHz (SATA 1.0). The aspect ratio of the transistors, along with the values of the resistors in the delay cell, are summarized in Table 3.

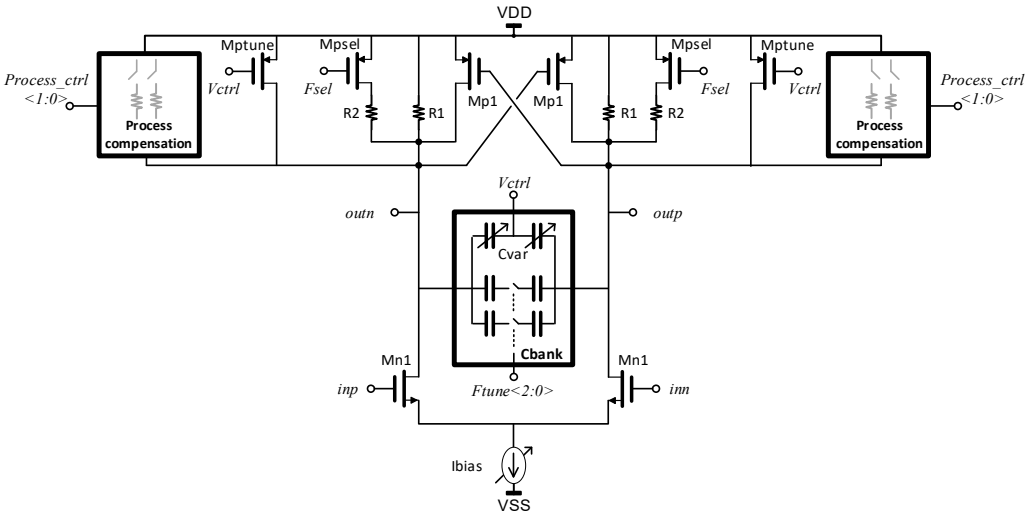



**Figure 3.** The delay element.

**Table 3.** Transistor aspect ratios and resistor values of the elements in Figure 3.

| Element | Aspect Ratio/Resistor Value |
|---|---|
| Mn1 | 2 μm/100 nm |
| Mp1 | 2 μm/60 nm |
| Mptune | 300 nm/130 nm |
| Mpsel | 24 μm/30 nm |
| R1 | 410 Ω |
| R2 | 3 kΩ |

The frequency of the VCO is tuned by the control voltage *Vctrl*, which biases the capacitor Cvar and the PMOS transistors Mptune. The proposed combined engagement of the varactors and the transistors, at the same time, significantly improves the tuning linearity compared with the control by the varactors alone. A capacitor bank, as shown in Figure 4, is used to select the frequency range. It consists of the two varactors that make the continuous tuning range connected in parallel with blocks of other capacitor arrays (4 fF, 8 fF, 16 fF) that are partially enabled by the control signal *Ftune*<2:0>. Additionally, a programmable current is employed to control the current, which biases the delay elements, as depicted in Figure 5. The bias current can be selected among six values by enabling the

corresponding resistors R5 to R0 through the control signals *Isel*<5:0>, respectively. The aspect ratio of the transistors, as well as the resistor values, are included in Table 4. The minimum current is enabled by *Isel<0>* and the corresponding resistor R0. The rest of the current control is performed by enabling the resistors R1 to R5 through the transistors M1 to M5, respectively, following a thermocode logic. The minimum and maximum values of each delay element are between 1 mA and 2 mA.

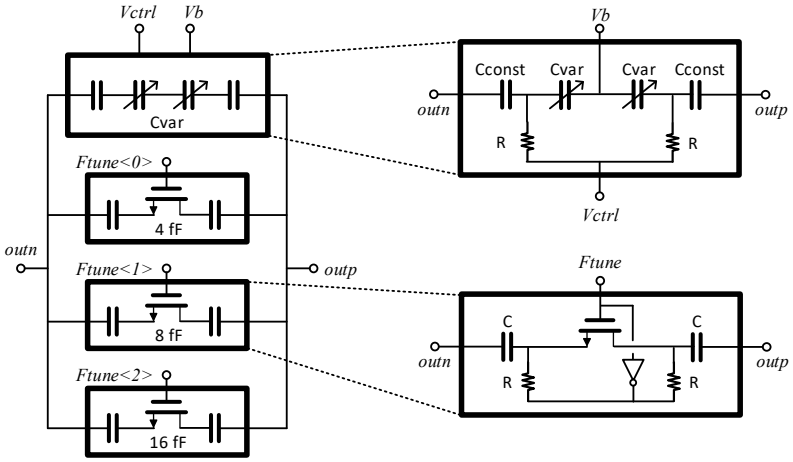



**Figure 4.** The capacitor bank.

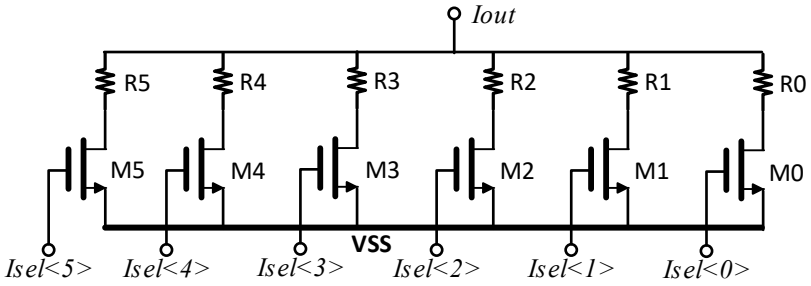



**Figure 5.** The programmable bias.

**Table 4.** Transistor aspect ratios and resistor values of the elements in Figure 5.

| Element | Aspect Ratio/Resistor Value |
|---|---|
| M<5:0> | 10 µm/50 nm |
| R0 | 285 Ω |
| R1 | 975 Ω |
| R2 | 850 Ω |
| R3 | 590 Ω |
| R4 | 415 Ω |
| R5 | 275 Ω |

### *2.2. The Linearity Improvement Technique*

Frequency tuning linearity is one of the most critical performance factors of a VCO and one of the most important parameters in the design of phase-locked loops (PLLs) [1]. Most of the ring-oscillator-based VCOs suffer from poor frequency tuning linearity, which results in a quite significant variation in the $K_{VCO}$ in the *Vctrl* range that the PLL must be able to support. The *Vctrl* range of a PLL is mainly determined by the voltage headroom of the charge pump (CP), which is the preceding stage of the VCO. Since the $K_{VCO}$ directly affects the dynamics of the PLL, a large variation may create serious issues, such as loop instability and degraded phase noise performance. Thus, $K_{VCO}$ should be constant over the entire *Vctrl* range with a $K_{VCO,max}/K_{VCO,min}$ ratio less than two [1,15].

The proposed technique in this paper significantly improves tuning linearity. The concept for the linearization is to produce a tuning function complementary to the initial tuning generated by the varactor, as illustrated in Figure 6. Therefore, the tuning in the proposed design is performed by biasing the varactors together with the transistors Mptune, as shown in Figure 3.

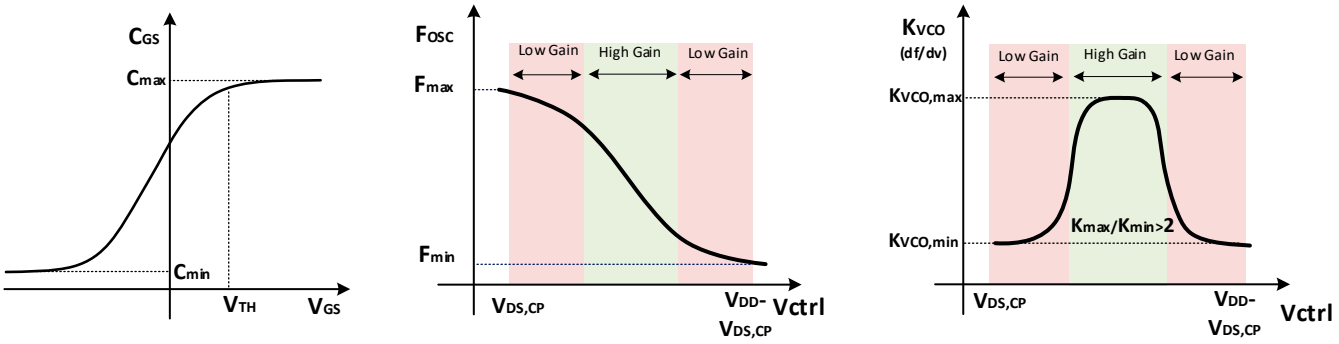



**Figure 6.** (**a**) Varactor capacitance dependence on $V_{GS}$; (**b**) frequency control vs. *Vctrl*; (**c**) Kvco vs. *Vctrl*.

A popular method of fine frequency tuning in CMOS VCOs is the usage of accumulation mode varactors. The varactors are able to offer variable capacitance, the value of which depends on their gate-source voltage, with a Cmax/Cmin ratio higher than 2 in most modern process nodes. Their main drawback is related to the fact that they approach their maximum and minimum values for $V_{GS}$ range less than 0.5 V, as shown in Figure 6a, which can be even lower than 0.5 V, resulting in non-linear frequency control and VCO gain (Kvco), as illustrated in Figure 6b and Figure 6c, respectively [16]. Kvco linearity is a quite critical performance factor for the PLL since it can affect the loop dynamics, leading to degraded loop stability or noise shaping. As a result, it is critical to ensure that the VCO gain is maintained quite constant, with a maximum over minimum ratio of less than 1.5 across all the *Vctrl* ranges that the PLL must support.

A widely used technique for VCO gain equalization is the utilization of a parallel combination of two or more varactor stages biased at different source-bulk voltage levels [16], as presented in Figure 7. In this case, the total capacitance is equal to the sum of the capacitance offered by each varactor stage, resulting in a fairly linear variable capacitance over the total required voltage range. However, this technique may lead to a large layout area with increased parasitics, which, especially in ring oscillator-based VCOs, can limit the maximum oscillation frequency or result in a power-hungry design.

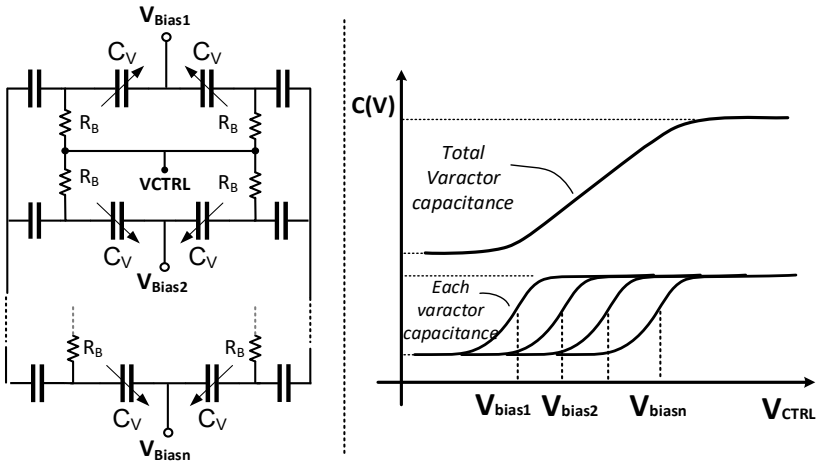



**Figure 7.** Parallel combination of multiple varactor stages biased at different source-bulk voltages.

Another well-known method of fine frequency tuning in ring oscillators is the use of variable resistors as the load for the delay cells [17]. The variable resistor is mainly implemented by MOS devices, the gate voltage of which is controlled by the PLL control voltage. It is well known that a MOS transistor operating in the triode region behaves as a linear variable resistor with a sufficiently high maximum-to-minimum ratio. Thus, it can offer a sufficient way of tuning the frequency of a ring oscillator. However, for control voltage levels at which the MOS device enters the saturation region, the slope of the V/I output characteristic of the device is drastically reduced, leading to decreased resistance variability and, therefore, reduced VCO gain. The voltage range for which the device remains in the triode region does not exceed some hundreds of mV, resulting again in a quite non-linear Kvco in the *Vctrl* range of interest, usually from $V_{DS,CP}$ to $V_{DD} - V_{DS,CP}$, where $V_{DS,CP}$ is the drain-source voltage of one MOSFET [1,2].

In the proposed design, in order to achieve linear Kvco across all the required *Vctrl* ranges while simultaneously preserving low layout area and parasitic elements, a combination of both of the aforementioned techniques is exploited. The parallel combination of a MOS variable resistor and an accumulation mode varactor biased at the proper source-bulk voltage, as illustrated in Figure 8, is able to sufficiently equalize the VCO gain in the total range of interest. More specifically, the main idea on which the proposed linearization technique is based is as follows:

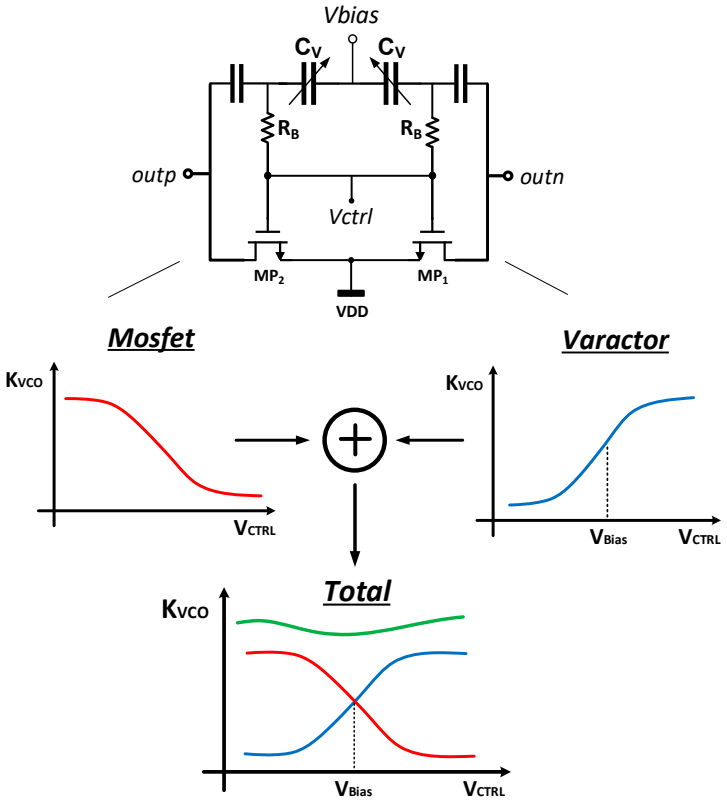



**Figure 8.** The linearization technique of Kvco (Mosfet contribution on $K_{VCO}$ with red line, Varactor contribution on $K_{VCO}$ with blue line, Combined contribution on $K_{VCO}$ with green line).

The MOSFET is able to offer adequate gain for *Vctrl* values for which it remains in the triode region and operates as a variable resistor, as explained before. When *Vctrl* becomes low, the MOSFET enters the saturation region, and its output resistance ($dV_{DS}/dI_{DS}$) becomes almost constant, resulting in reduced variability and, therefore, decreased VCO gain. However, the varactor is biased at a proper source–body voltage, offering increased gain in these *Vctrl* values, where the MOSFET is not able to maintain the gain constant at the desired level. As presented in Figure 8, after design optimization of both the MOSFET and the varactor dimensions, as well as the biasing voltage, the VCO gain is equalized across

the total *Vctrl* range. In this way, the Kvco is almost constant without the necessity of using multiple varactor stages, which may result in a power-hungry design and bulky layout.

### *2.3. The Process Detection and Compensation Topology*

As shown in Figure 9, the topology of the process detection and compensation topology consists of three blocks: the process-dependent circuit, the process-independent circuit, and the decision circuit.

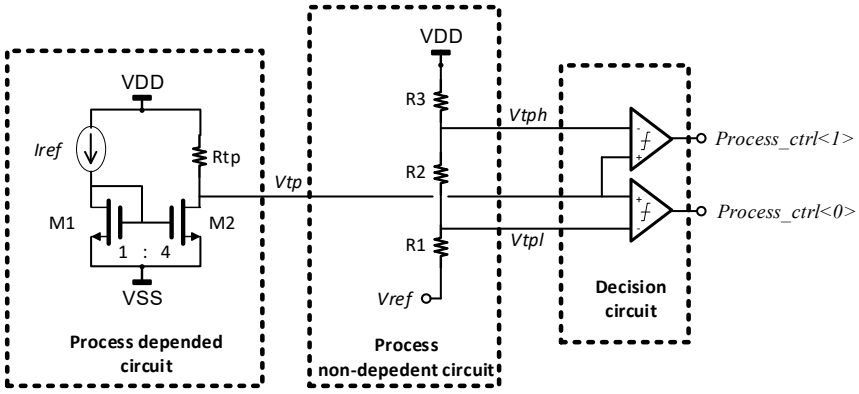



**Figure 9.** The process compensation method.

The process-dependent circuit is based on a current mirror with a load resistor producing the test voltage *Vtp*, which strongly depends on the process variations. A constant reference current *Iref* is driving the test poly-resistor Rtp through the NMOS current mirror. The topology intentionally includes the specific NMOS current mirror and poly-resistor in a similar way that the delay element includes the NMOS transistor Mn1, the poly-resistors R1, R2, and those employed in the process compensation block, shown in Figure 3. Thus, the process variation has a related impact on both process-dependent circuits and delay elements.

The process-independent circuit is a voltage divider producing two constant voltages, *Vtph* and *Vtpl*, where *Vtp* is greater than *Vtpl*. The voltages *Vref* and *VDD* are constant, as they are generated by a bandgap voltage reference circuit and a low dropout regulator, respectively. The resistors R1 to R3 are of the same type as each other, and, therefore, the process variation does not affect the output voltages *Vtph* and *Vtpl*.

The decision circuit consists of two comparators that compare the process-dependent voltage *Vtp* with the constant levels of *Vtph* and *Vtpl*. In the typical case, the value of *Vtp* is between the voltages *Vtph* and *Vtpl*, while in the fast–fast (ff) corner, *Vtp* is greater than both *Vtph* and *Vtpl*, and in the slow-slow (ss) corner, *Vtp* is lower than *Vtph* and *Vtpl*. The result of the comparison is the 2-bit digital word *Process_ctrl*<1:0> that enables or disables the corresponding compensating resistors in the delay element.

The circuit has been designed to keep the current consumption low. Thus, for VDD = 0.8 V and setting *Iref* equal to 1 μA, the aspect ratio of the transistor M1 is 1 μm/0.1 μm and of M2 is 4 μm/0.1 μm. The value of Rtp is 34.9 kΩ, R1 = 50.8 kΩ, R2 = 7.25 kΩ, and R3 = 29 kΩ.

## 3. Simulation Results

The VCO topology has been designed using CMOS 22 nm technology. The supply voltage (*VDD*) is 0.8 V. The design has been optimized, focusing on three targets: (a) high-tuning linearity in all sub-bands; (b) full coverage of the main frequency in all process corners; and (c) optimized phase noise in all corners and speeds with optimum current consumption.

The performance of the overall topology has been evaluated by post-layout simulation results obtained through Virtuoso Cadence Tools and Spectre simulator. Depending on the intended performance metric, a suitable analysis has been used, including the transient analysis, the periodic steady state (PSS), and the periodic noise (pnoise).

### *3.1. The Automatic Process Corner Detector*

The proposed method that compensates for the frequency drift due to process variations has been described in Section 2.3. Through the compensation, the VCO automatically switches to the suitable configuration in order for the oscillation frequency to retrieve the correct range. In this way, the VCO tuning range can be significantly reduced, and the overall performance is kept within the optimal state. In the process detection circuit, *Iref* is 1 μA and *Vref* is 0.4 V. For the typical case, *Vtp* is equal to 650 mV, while for the ss and ff corners, *Vtp* becomes equal to 610 mV and 685 mV, respectively. Therefore, the low and high-level voltage thresholds, *Vtpl* and *Vtph*, have been set equal to 633 mV and 667 mV, respectively. It must be noted that the voltage variation of *Vtp*, due to temperature variation from −40 °C to 125 °C, is less than ±1 mV in the typical case and less than ±5 mV in the worst corners, and consequently, it can be ignored. The results are depicted in Figure 10.

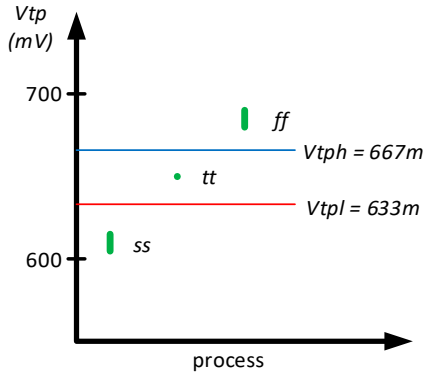



**Figure 10.** The test process voltage *Vtp* vs. the process corner over temperature −40 °C to 125 °C.

### *3.2. The Linearity Improvement*

Special care has been given in this design to keep the VCO gain Kvco almost constant over the control voltage *Vctrl*, resulting in improved tuning linearity, as already described in Section 2.2. The final result of the Kvco, together with the impact of each one of the varactors and the MOSFET, is shown in Figure 11. The final Kvco, depicted with the green line, becomes more stable, with significantly less variation across the full range of *Vctrl*.

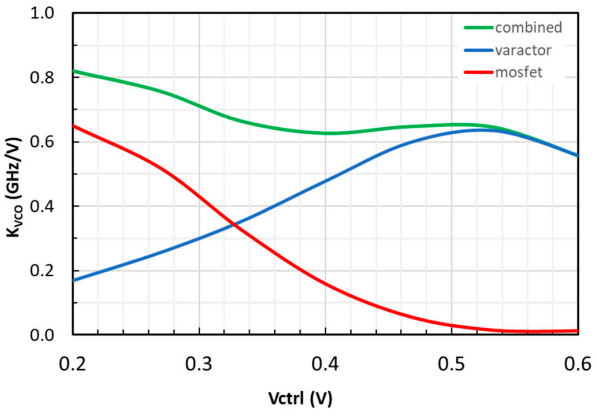



**Figure 11.** Kvco vs. *Vctrl* with and without the linearity improvement technique.

### *3.3. The High-Speed VCO*

The high-speed VCO is designed to cover the frequency range from 2.5 GHz to 3 GHz. The switch between the 2.5 GHz and 3 GHz oscillation frequencies is achieved by enabling the resistor R2, depicted in Figure 3. As already mentioned, simultaneous tuning by both a varactor and a MOSFET improves the tuning linearity. The frequency tuning over *Vctrl* in the typical process case is shown in Figure 12, with (solid line) and without (dashed line) the linearity improvement.

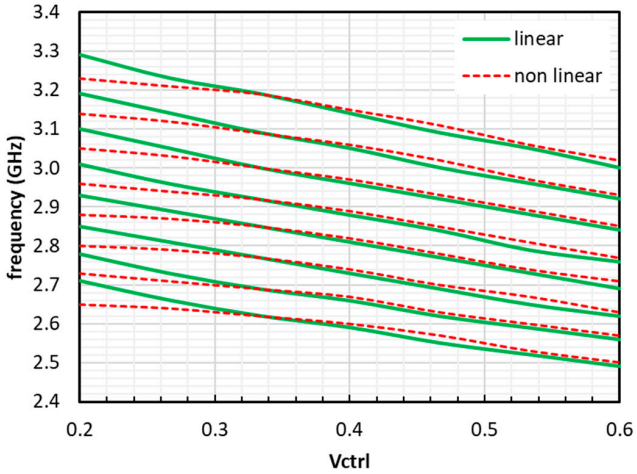
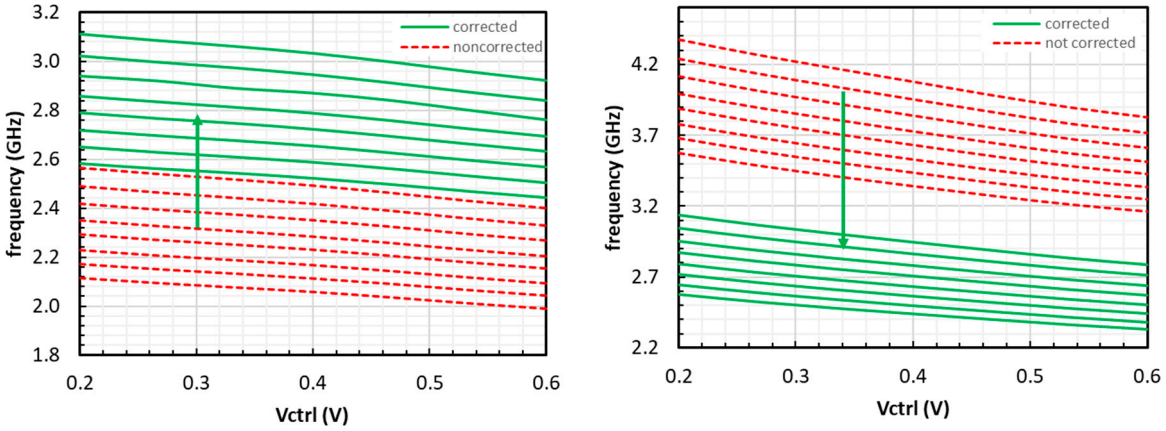



**Figure 12.** Frequency tuning with tuning linearity improvement (green line) and without tuning linearity improvement (red line).

VCOs are very susceptible in the process corner, and this is probably one of the major factors that affects mostly the oscillation frequency and, secondly, other parameters, like the power consumption and the phase noise. One of the most common methods to overcome this problem is by employing a capacitor array in the delay element. However, as the frequency drift due to the process variation is usually significantly large, the required compensation capacitors must also have a large value, occupying a considerably large area in the layout. The drawback is, then, that the overall layout of the delay elements and the VCO may become large, minimizing the ability for a compact and symmetrical layout and creating more parasitic elements. Furthermore, this method may not improve other important parameters, like phase noise.

On the other hand, the method proposed in this paper, by enabling only one resistor, saves layout area and reduces complexity. Applying this method to the proposed VCO and setting the operating frequency in the range of 3 GHz, the compensation over process can be shown in Figure 13a for the ss corner. The compensation for the ff corner can be shown in Figure 13b. In both cases, the frequency range recovers within the required values, while otherwise, the frequency range would be shifted completely out of the specifications. The total correction over the ss and the ff corners for a middle range *Vctrl* equal to 0.4 V is also depicted in Figure 14. It is clear that the tuning ranges of the corners are restored to regular values, allowing the VCO to operate within the specs designed for the typical case.




(**a**) (**b**)

**Figure 13.** Frequency tuning range with and without correction (**a**) ss corner and (**b**) ff corner.

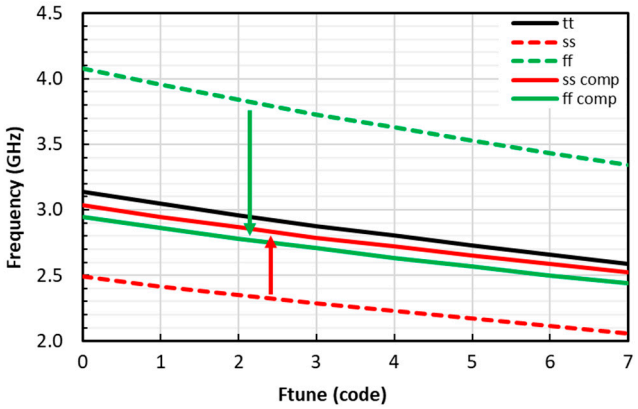



**Figure 14.** The frequency compensation over the corners in sub-bands for *Vctrl* = 0.4 V.

Important specifications for every VCO are the phase noise and the current consumption. Unfortunately, these two features are opposed to each other, meaning that good phase noise performance requires high current consumption. Therefore, as already mentioned, the bias current is programmable in order to maintain minimum consumption while achieving the required phase noise performance. The programmability helps to keep the performance at the required levels over the process variations and overcome other design failures. The phase noise at 3 GHz for power consumption from 3.84 mA to 6.88 mA, in typical process cases, is shown in Figure 15. The phase noise range is from −88.2 dBc/Hz to 96.1 dBc/Hz, respectively, at 1 MHz. A summary of the most significant parameters of the HF-VCO performance is shown in Table 5. There, it can be shown that the phase noise can be improved by increasing the power consumption, while the other parameters remain almost constant in all currents and all corners. The worst output duty cycle error is less than 2.5%, and the phase differences between the 90 deg outputs are negligible.

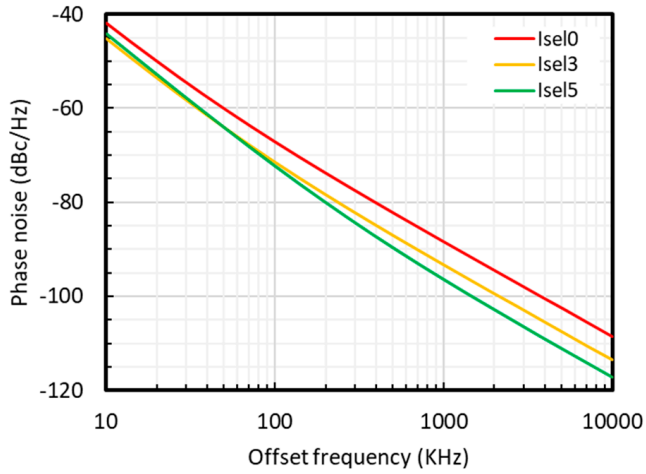



**Figure 15.** The phase noise at 3 GHz over the bias current (*Ftune*<2:0> = 4).

The performance results for the HF-VCO operating at 3 GHz in the SATA 3 mode are summarized in Table 5. For the sake of space in the paper, the results of only two of the six available bias currents are shown, specifically, the minimum *Isel0* and the maximum *Isel5*. The results show that the phase noise can be improved by setting a higher current bias, but all the other performance parameters are almost constant and invariant by the process corner. In particular, the phase error is less than 0.6 deg in all cases. Similar or even better results are taken from the HF-VCO at 2.5 GHz for the PCIe 2.0 mode, as summarized in Table 6.

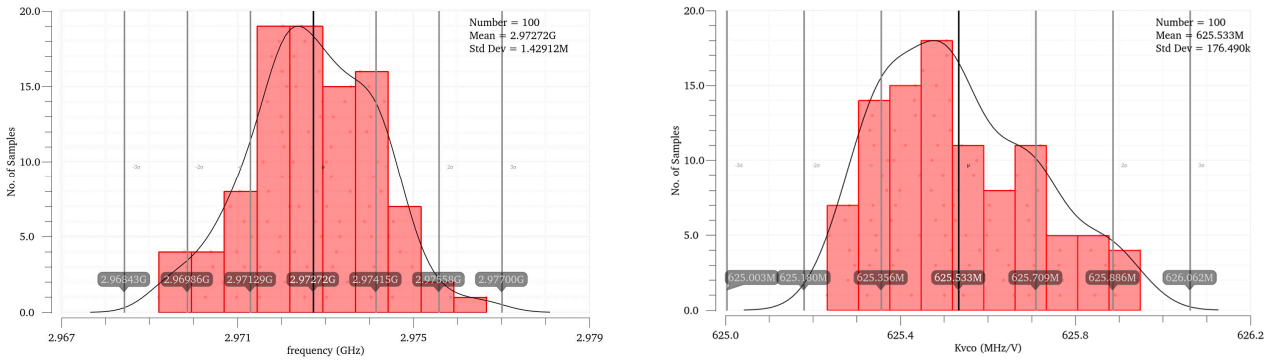
**Table 5.** HF-VCO performance at 3 GHz (SATA).

| Current Select | Performance Metric | tt Case | ss Case | ff Case |
|---|---|---|---|---|
| CURSEL0 | Frequency (GHz) | 3 | 3 | 3 |
| | Power consumption (mW) | 3.84 | 3.36 | 4.08 |
| | Phase noise @ 1 MHz (dBc/Hz) | −88.2 | −86.4 | −89.6 |
| | Duty cycle (%) | 49.7 | 52.2 | 49.4 |
| | Phase error for 90 deg (deg) | 0.02 | 0.2 | 0.03 |
| | Phase error for 180 deg (deg) | 0.05 | 0.4 | 0.01 |
| | Phase error for 270 deg (deg) | 0.04 | 0.6 | 0.01 |
| CURSEL5 | Frequency (GHz) | 3 | 3 | 3 |
| | Power consumption (mW) | 6.88 | 6.24 | 7.44 |
| | Phase noise @ 1 MHz (dBc/Hz) | −96.1 | −93.8 | −97.5 |
| | Duty cycle (%) | 49.1 | 49.8 | 47.7 |
| | Phase error for 90 deg (deg) | 0.02 | 0.07 | 0.01 |
| | Phase error for 180 deg (deg) | 0.05 | 0.2 | 0.02 |
| | Phase error for 270 deg (deg) | 0.1 | 0.2 | 0.01 |

**Table 6.** HF-VCO performance at 2.5 GHz (PCIe).

| Current Select | Performance Metric | tt Case | ss Case | ff Case |
|---|---|---|---|---|
| CURSEL0 | Frequency (GHz) | 2.5 | 2.5 | 2.5 |
| | Power consumption (mW) | 3.68 | 3.28 | 3.84 |
| | Phase noise @ 1 MHz (dBc/Hz) | −88.9 | −86 | −88.3 |
| | Duty cycle (%) | 50.5 | 51.8 | 49.9 |
| | Phase error for 90 deg (deg) | 0.1 | 0.2 | 0.02 |
| | Phase error for 180 deg (deg) | 0.2 | 0.4 | 0.04 |
| | Phase error for 270 deg (deg) | 0.04 | 0.5 | 0.01 |
| CURSEL5 | Frequency (GHz) | 2.5 | 2.5 | 2.5 |
| | Power consumption (mW) | 6.56 | 6.08 | 7.12 |
| | Phase noise @ 1 MHz (dBc/Hz) | −96.2 | −93.9 | −97.8 |
| | Duty cycle (%) | 49.3 | 50 | 48 |
| | Phase error for 90 deg (deg) | 0.01 | 0.01 | 0.01 |
| | Phase error for 180 deg (deg) | 0.04 | 0.03 | 0.02 |
| | Phase error for 270 deg (deg) | 0.02 | 0.01 | 0.01 |

Setting the tuning close to the frequency of 3 GHz, Monte Carlo simulations have been performed over local and process mismatches to verify that the frequency and $K_{VCO}$ are not affected by them. The results for 100 samples show for the frequency a mean value of 2.973 GHz with a standard deviation of 1.5 MHz and for $K_{VCO}$ a mean value of 625.533 MHz/V with a standard deviation of 176.5 kHz/V, respectively. The histograms of the Monte Carlo simulation results are depicted in Figure 16a,b.




(**a**) (**b**)

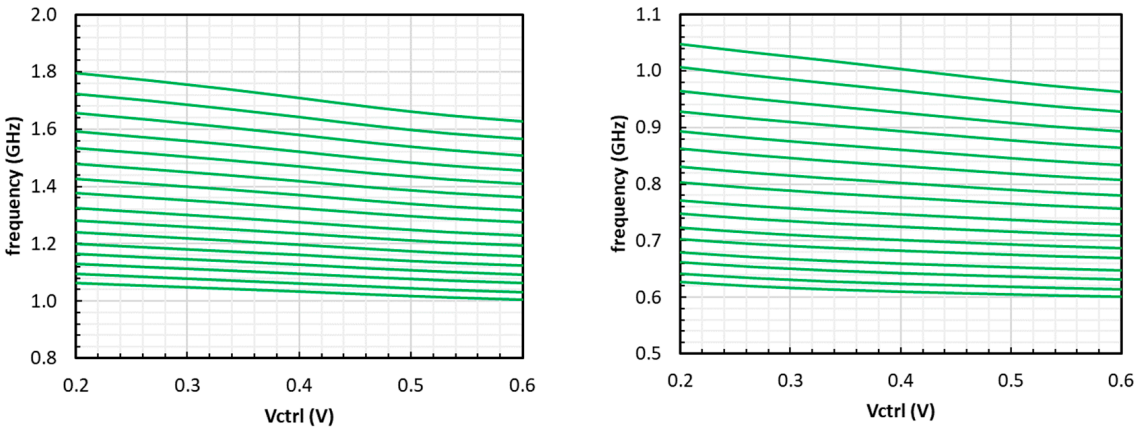
**Figure 16.** The histograms of Monte Carlo simulations at a 3 GHz oscillation frequency for (**a**) oscillation frequency and (**b**) $K_{VCO}$.

### *3.4. The Low-Speed VCO*

The LF-VCO, operating at frequencies less than 2 GHz, has been designed by following a similar design approximation to the HF-VCO. As already presented in Table 2, this VCO is optimized in terms of current consumption and phase noise for the frequencies required from the low-speed modes of the SATA (1.5–0.75 GHz) and PCIe (1.25 GHz), respectively.

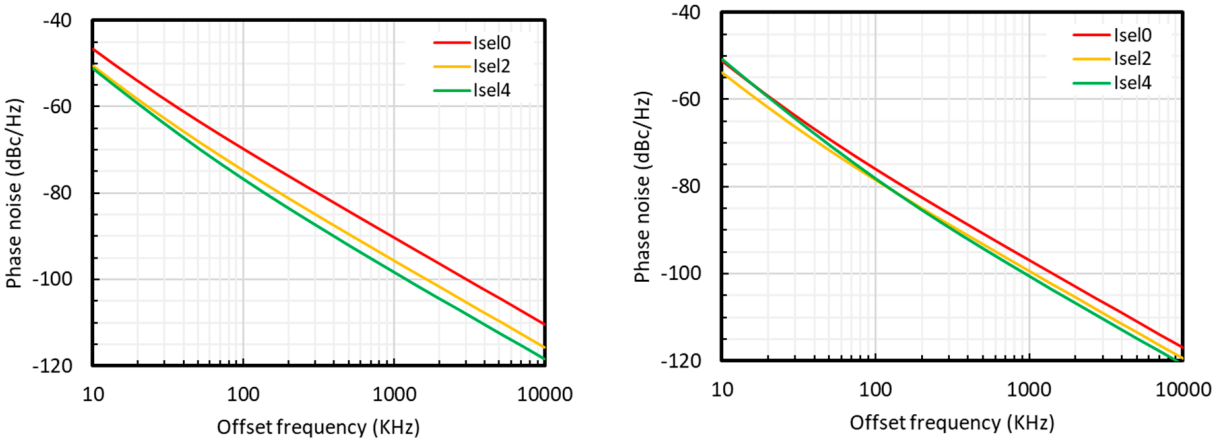
Due to the lower frequencies, all the calibrations followed in the design of the HF-VCO are applied to this design, obtaining similar or even better compensation results. The most important differences between the core of the VCO are the lower power consumption and, from a layout perspective, the additional 32 fF capacitor array used in the capacitor bank to achieve the lower frequency.

For comparison with the HF-VCO, its performance parameters are presented only at the two frequencies for the SATA mode, as the performance in the PCIe mode is similar. The only difference is the slightly lower power consumption due to the lower speed of PCIe. In Figure 17a,b, the frequency ranges at 1.5 GHz and 0.75 GHz are shown, respectively, in typical. For both cases, the plots depict the responses with linear improvement. In addition, although not included in this paper for the sake of space, the corner correction is also applied in the LF-VCO, keeping the frequency range within the required values over the corner variations. The phase noise for the frequencies of 1.5 GHz and 0.75 GHz is shown in Figure 18a and Figure 18b, respectively.




(**a**) (**b**)

**Figure 17.** Frequency tuning range of LF-VCO at (**a**) 1.5 GHz and (**b**) 0.75 GHz.




(**a**) (**b**)

**Figure 18.** Phase noise of LF-VCO over the bias current at (**a**) 1.5 GHz and (**b**) 0.75 GHz (*Ftune*<2:0> = 4).

The key performance parameters of the SATA protocol at the two frequencies of 1.5 GHz and 0.75 GHz are shown in Tables 7 and 8, respectively. Again, the performance of the PCIe is similar and, therefore, is not shown in this paper. The most important thing is that the phase noise remains almost constant over the process variations, although it can be controlled by the cost of power consumption. In both frequencies, all other parameters are stable over corners and the different bias currents. For example, the phase error is less than 0.6 deg, and the duty cycle error is less than 3.2%.

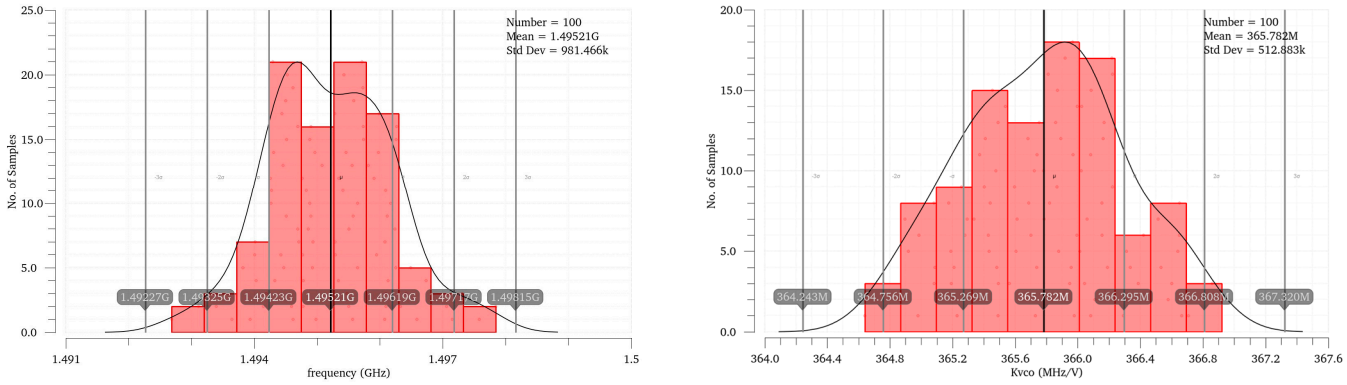
**Table 7.** LF-VCO performance at 1.5 GHz (SATA).

| Current Select | Performance Metric | tt Case | ss Case | ff Case |
|---|---|---|---|---|
| CURSEL0 | Frequency (GHz) | 1.5 | 1.5 | 1.5 |
| | Power consumption (mW) | 2.08 | 1.76 | 2.24 |
| | Phase noise @ 1 MHz (dBc/Hz) | −90.2 | −89 | −90.6 |
| | Duty cycle (%) | 51.6 | 51.7 | 51.4 |
| | Phase error for 90 deg (deg) | 0.08 | 0.02 | 0.05 |
| | Phase error for 180 deg (deg) | 0.2 | 0.1 | 0.05 |
| | Phase error for 270 deg (deg) | 0.4 | 0.06 | 0.02 |
| CURSEL5 | Frequency (GHz) | 1.5 | 1.5 | 1.5 |
| | Power consumption (mW) | 3.68 | 3.12 | 4.08 |
| | Phase noise @ 1 MHz (dBc/Hz) | −98.3 | −97.2 | −99.2 |
| | Duty cycle (%) | 49.4 | 50.1 | 48.2 |
| | Phase error for 90 deg (deg) | 0.01 | 0.2 | 0.05 |
| | Phase error for 180 deg (deg) | 0.01 | 0.3 | 0.03 |
| | Phase error for 270 deg (deg) | 0.1 | 0.01 | 0.01 |

**Table 8.** LF-VCO performance at 0.75 GHz (SATA).

| Current Select | Performance Metric | tt Case | ss Case | ff Case |
|---|---|---|---|---|
| CURSEL0 | Frequency (GHz) | 0.75 | 0.75 | 0.75 |
| | Power consumption (mW) | 1.92 | 1.6 | 2.0 |
| | Phase noise @ 1 MHz (dBc/Hz) | −96.9 | −94.4 | −98.9 |
| | Duty cycle (%) | 52.3 | 53.2 | 51.9 |
| | Phase error for 90 deg (deg) | 0.2 | 0.04 | 0.02 |
| | Phase error for 180 deg (deg) | 0.4 | 0.2 | 0.06 |
| | Phase error for 270 deg (deg) | 0.6 | 0.1 | 0.02 |
| CURSEL5 | Frequency (GHz) | 0.75 | 0.75 | 0.75 |
| | Power consumption (mW) | 3.04 | 2.72 | 3.12 |
| | Phase noise @ 1 MHz (dBc/Hz) | −100.5 | −99.6 | −101 |
| | Duty cycle (%) | 50.3 | 50.6 | 52.5 |
| | Phase error for 90 deg (deg) | 0.08 | 0.08 | 0.02 |
| | Phase error for 180 deg (deg) | 0.2 | 0.07 | 0.05 |
| | Phase error for 270 deg (deg) | 0.1 | 0.05 | 0.03 |

Setting the tuning close to the frequency of 1.5 GHz, Monte Carlo simulations have been performed over local and process mismatches to verify that the frequency and $K_{VCO}$ are not affected by them. The results for 100 samples show for the frequency a mean value of 1.495 GHz with a standard deviation of 0.981 MHz and for $K_{VCO}$ a mean value of 365.782 MHz/V with a standard deviation of 512.9 kHz/V, respectively. The histograms of the Monte Carlo simulation results are depicted in Figure 19a,b.




(**a**) (**b**)

**Figure 19.** The histograms of Monte Carlo simulations at 1.5 GHz oscillation frequency for (**a**) oscillation frequency and (**b**) $K_{VCO}$.

The layout of the HF-VCO core, consisting of four delay cells, is illustrated in Figure 20. The size is about 85 × 86 µm$^2$.

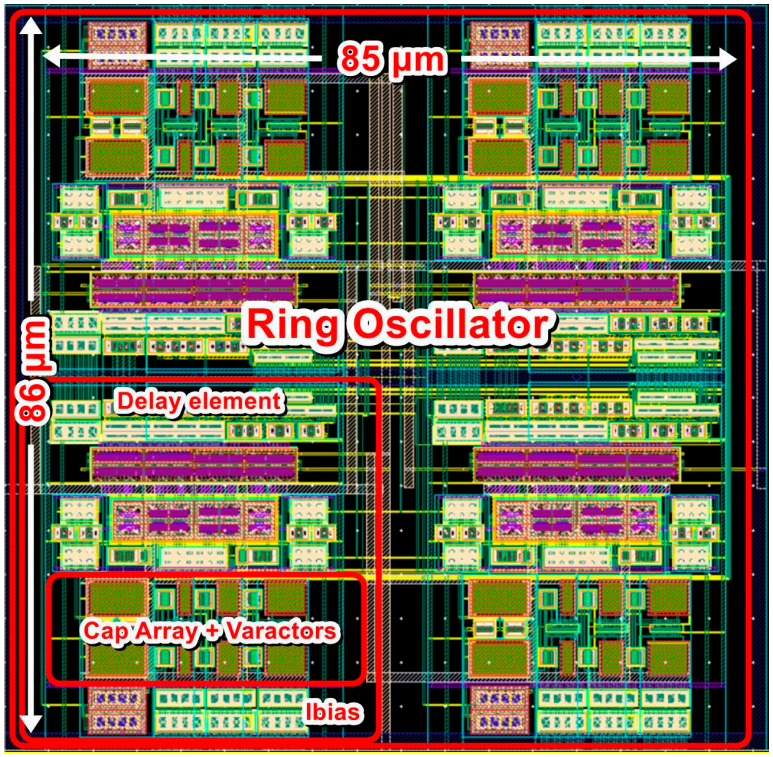



**Figure 20.** The layout of the HF-VCO.

Table 9 summarizes the most important features of the proposed design in comparison with other published ring VCOs working in the range of GHz. The advantages of the proposed VCO are its supply voltage, which leads to decreased power consumption, and the attractive capability of the electronic control of the current consumption against phase noise, depending on the desired application. Another significant advantage of the proposed work, compared with the others, is that it performs with a $K_{VCO,max}/K_{VCO,min}$ ratio of less than 1.5 over the full frequency tuning range, ensuring good PLL stability and constant phase noise shaping.

**Table 9.** Comparison results.

| | This Work | [8] | [9] | [10] | [11] | [13] | [14] |
|---|---|---|---|---|---|---|---|
| Process (nm) | 22 | 180 | 180 | 180 | 180 | 90 | 65 |
| Supply Voltage (V) | 0.8 | 1.8 | 1.8 | 1.8 | 1.8 | 1 | 1.2 |
| Frequency (GHz) | 3 | 3.125 | 5.9 | 3.71 | 5.79 | - | 2.915 |
| Tuning Range (GHz) | 0.6–3.3 | 18% | 18.5% | 78.5% | 3.125 | 1–10 | 0.624–2.915 |
| $K_{VCO,max}/K_{VCO,min}$ | <1.5 | >2 | >2 | - | >2 | >2 | >2 |
| PN (dBc/Hz) @ 1 MHz | −96.1 @ 3 GHz | −91 | −86.7 | −89 @ 3.7 GHz | −99.5 @ 5.79 GHz | - | −94 @ 2.9 GHz |
| Power Consumption (mW) | 6.88 @ 3 GHz | 12.6 | 8.1 | 10.54 @ 3.7 GHz | - | 6.3 | 6.64 @ 2.9 GHz |
| Area ($\mu m^2$) | 14,620 | - | - | 207,000 | - | 215 | 88,200 |
| Results | post-layout simulations | post-layout simulations | simulations | post-layout simulations | fabricated prototype | post-layout simulations | post-layout simulations |

## 4. Conclusions

A VCO topology has been proposed in this paper for SATA, PCIe, and USB applications. The VCO supports multiple speeds as specified by the corresponding protocols and embeds two mechanisms, one for improving tuning linearity and one for compensating the frequency against the technology process variations. Both are very simple, based mostly on a programmable resistor network, although they are very effective. Furthermore, the performance of the VCO is optimized for each band in terms of phase noise and current consumption by employing bias programmability. Through these configurations, the key performance parameters, in terms of phase noise, power consumption, duty cycle, and phase error, are presented for each case. The circuit has been designed in a 22 nm CMOS technology node, operating with a 0.8 V supply voltage. The power consumption depends on the operating frequency, with an average value equal to 3.84 mW at 3 GHz, achieving a phase noise better than −90 dBc/Hz at 1 MHz offset, and less than 2 mW at 0.75 GHz with a phase noise of −96.9 dBc/Hz at 1 MHz offset.

**Author Contributions:** Conceptualization, P.B. and A.T.; methodology, P.B., A.T. and G.S.; software, P.B. and A.T.; validation, P.B., A.T. and G.S.; formal analysis, P.B. and A.T.; investigation, P.B., A.T. and G.S.; resources, P.B., A.T. and G.S.; data curation, P.B., A.T. and G.S.; writing—original draft preparation, P.B., A.T. and G.S.; writing—review and editing, P.B., A.T. and G.S.; visualization, P.B., A.T. and G.S.; supervision, G.S. All authors have read and agreed to the published version of the manuscript.

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