

## Article

# Machine Learning-Based Soft-Error-Rate Evaluation for Large-Scale Integrated Circuits

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**Abstract:** Transient pulses generated by high-energy particles can cause soft errors in circuits, resulting in spacecraft malfunctions and posing serious threats to the normal operation of spacecraft. For integrated circuits used in space applications, it is necessary to first evaluate soft errors caused by transient pulses. Conventional soft-error-rate evaluation tools are designed to simulate the generation of transient pulses using many accurate models, while the propagation of transient pulses is primarily simulated by circuit-level simulation tools. Due to the limitations of simulation tools, conventional evaluation approaches are limited to the circuit scale. The simulation runtime is unbearable for large-scale integrated circuits. This paper presents an approach for evaluating the soft error rate using machine learning. A back propagation neural network is implemented in the proposed approach. It helps to determine the probability of transient pulse propagation. Compared with the conventional soft-error-rate evaluation results, the proposed approach demonstrates a strong correlation in both trend and magnitude. The average difference between the results obtained using the proposed evaluation method and the experimental results is 23.5%, which is 7.5% higher than that between the results obtained using the conventional evaluation method and the experimental results. Compared to the conventional evaluation method, the proposed approach improves the runtime by an order of magnitude. The proposed approach also benefits the locating of highly sensitive circuit nodes in large-scale integrated circuits. Circuit design and radiation hardening are both useful applications.

**Keywords:** machine learning; single event transient; soft error rate; transient pulse propagation



**Citation:** Song, R.; Shao, J.; Chi, Y.; Liang, B.; Chen, J.; Wu, Z. Machine Learning-Based Soft-Error-Rate Evaluation for Large-Scale Integrated Circuits. *Electronics* **2023**, *12*, 4978. <https://doi.org/10.3390/electronics12244978>

Academic Editor: Paul Leroux

Received: 6 November 2023

Revised: 9 December 2023

Accepted: 11 December 2023

Published: 12 December 2023



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## 1. Introduction

When a high-energy particle passes through an integrated circuit in the space radiation environment, it loses energy along its path [1,2]. The lost energy is transferred to the semiconductor material, ionizing electrons of silicon atoms [3]. These ionized electron-hole pairs are subject to both drift and diffusion. They move throughout the entire semiconductor material and are collected by transistors [4–6]. The collected electron-hole pairs produce unexpected transient pulses in circuit nodes [7]. These transient pulses propagate along the circuit path and cause soft errors [8–10]. A soft error is a significant threat to integrated circuits. It alters the logic function and can potentially lead to catastrophic consequences for an entire chip, system, or even a spacecraft.

To mitigate soft errors in integrated circuits for space applications, it is crucial to evaluate the soft error rate (SER) during the circuit design phase. In previous works, several circuit-level evaluation approaches have been proposed to investigate the SER of integrated circuits [11–21]. These works have proposed many accurate models to generate transient pulses in circuit nodes. Then, they utilize simulation tools, such as the Simulation Program with Integrated Circuit Emphasis (SPICE) and Technology Computer-Aided Device (TCAD), to simulate transient pulse propagation and capture. Based on the simulated results, conventional evaluation approaches determine soft errors and calculate

the SER of integrated circuits. Due to the limitations of simulation tools, conventional evaluation approaches are limited to the circuit scale. The simulation runtime is unbearable for large-scale integrated circuits [22].

This paper presents a novel approach for evaluating SER in order to reduce the simulation runtime. A back propagation neural network (BPNN) is implemented to determine the probability of transient pulse propagation. The SER can be determined based on the probability of propagation. The proposed approach does not require determining the probability value of transient pulse propagation to flip-flops through actual circuit-level simulation. Instead, it takes the probability of pulse propagation for each instance in the data path as the input value. This input is then fed into a machine learning model, and the propagation probability value is obtained through the calculation of the machine model. A chip with three test circuits was designed using commercial CMOS technology to investigate the accuracy of the proposed approach. The proposed approach achieves a good consistency in both trend and order of magnitude.

## 2. SER Evaluation Overview

In previous works, several approaches for evaluating soft error rate (SER) have been proposed. These approaches are used to evaluate key circuits, including combination circuits, flip-flops, and SRAM. In general, the existing soft error evaluation approaches are mainly divided into three categories: SPICE-level evaluation approaches, TCAD-level evaluation approaches, and Monte Carlo-based evaluation approaches.

The SPICE-level evaluation approach is widely used. Based on the SPICE device model and the netlist of the evaluated circuit, a separate current source is introduced directly at the sensitive node of the circuit to simulate the transient current caused by incident particles [23–25]. Then, it simulates the corresponding circuit response to obtain soft errors. Correias et al. simulated the evaluation of a 90 nm SRAM circuit using the SPICE circuit-level soft error evaluation tool. The evaluation results obtained are in good agreement with the experimental results [12]. Shambhulingaiah et al. utilized the same tool to simulate sequential instances, such as flip-flops, and identified the sensitive nodes of the flip-flop [13]. Wang and Du et al. utilized the SPICE circuit-level simulation tool to simulate the propagation process of single-event transients in large-scale combinational circuits. Their objective was to assess the impact of single-event transient pulses on soft errors in these circuits [14,15]. Li et al. simulated and analyzed the reliability of integrated circuits using the SPICE tool and proposed a corresponding evaluation process [16].

The TCAD-level evaluation approach differs different from the SPICE-level evaluation approach. It first constructs the TCAD model based on the layout structure and manufacturing process parameters of the circuit instance. Then, the TCAD model simulates the ionization of electron-hole pairs in the incident particles using a specific numerical distribution, such as exponential or Gaussian distribution. The transport process of electron-hole pairs in the TCAD model is calculated using the carrier drift diffusion and other models embedded in the TCAD simulation tool. It simulates the charge collection of the instance and the instantaneous response of the circuit node, and determines whether the circuit instance produces soft errors. Yoni et al. constructed a comprehensive 3D TCAD model using the layout structure of D flip-flops. They subsequently simulated the circuit's response when the D flip-flop cell was exposed to terrestrial neutrons [17]. Xu et al. utilized TCAD simulation tools to investigate the mechanism of soft errors in standard instances. They also employed a combination of TCAD simulation tools and SPICE circuit-level simulation tools [18].

Recently, the Monte Carlo-based evaluation approach has become an important evaluation approach. It utilizes Monte Carlo tools, such as Geant4 and SRIM, to simulate and calculate the interaction between the incident particles and the semiconductor material. Then, it converts the charge accumulated by the incident particles in the material into charge and transient current collected by the device through charge transport and charge collection mechanisms. Finally, it simulates the transient response of the circuit using

additional simulation tools and determines whether a soft error occurs. Many Monte Carlo-based evaluation approaches have been proposed to evaluate the SER of circuits, such as MRED [11], MUSCA SEP3 [22], PHITS-HyENEXSS [19], and IRT [20].

### 3. The SER Evaluation Using Machine Learning Models

#### 3.1. The Transient Pulse Propagation Probability

A conventional register-to-register circuit path in integrated circuits is shown in Figure 1. It is used to explain the evaluation of transient pulse propagation using machine learning models. When a high-energy particle strikes this circuit, some logic instances (such as C0) collect the ionized electron-hole pairs and produce a transient pulse at circuit nodes. Then, the transient pulse propagates to flip-flops along circuit paths. When the transient pulse arrives at the input pin of instance C1, it propagates directly, and the probability of transient pulse propagation  $P_{C1}$  is equal to 1. However, when the transient pulse arrives at the input pin of instances C2 and C3, it may not propagate due to logic masking. For instance, C2 is an OR-gate instance. The transient pulse can only propagate when the value of the other input pin is 0. Similarly, C3 is an AND-gate instance. The transient pulse is able to propagate only when the value of the other input pin is 1. Therefore, the transient pulse propagation probabilities  $P_{C2}$  and  $P_{C3}$  depend on the instance type and input pin values. The values are determined using the following equations:

$$P_{C2} = 1 - P_{otherpin,1} \tag{1}$$

$$P_{C3} = P_{otherpin,1} \tag{2}$$

where  $P_{otherpin,1}$  is the probability when the value of the other pin is 1. If the input vectors are random,  $P_{otherpin,1}$  is equal to 0.5. The transient pulse that can propagate to flip-flops is determined by the propagation probabilities along the circuit path. For instance, the transient pulse that can propagate to flip-flop 1 (FF1) is determined by  $P_{C1}$ ,  $P_{C2}$ , and  $P_{C3}$ . If a relationship between  $P_{FF1}$  and  $P_{C1}-P_{C3}$  can be determined, the transient pulse propagation can be easily evaluated.

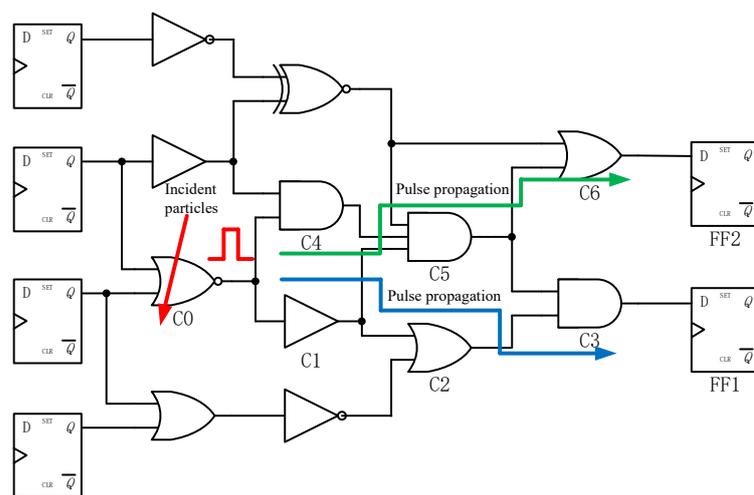
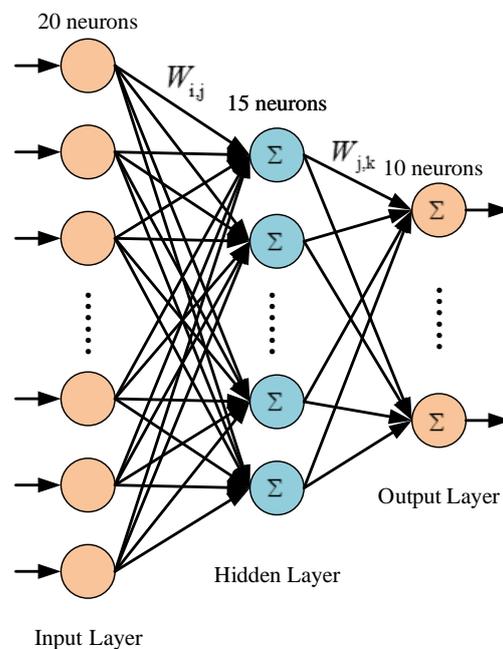


Figure 1. A conventional registers-to-registers circuit path.

Unfortunately, determining the relationship between flip-flops and logic cells along the circuit path is challenging due to the complexity of circuit structures. A simple fitting equation may not be suitable for all circuit structures. Recently, machine learning has been widely used in integrated circuit design [18,26]. Some machine learning models are used to analyze circuit structures in order to identify inherent connections between circuit cells. In this paper, a machine learning model (BPNN) is used to determine the relationship between flip-flops and logic instances along the circuit path. The BPNN is first described

in [27], and its basic structure consists of neurons, interconnection layers, and connection weight values. In this paper, the BPNN model consists of an input interconnection layer, a hidden interconnection layer, and an output interconnection layer. The basic structure is shown in Figure 2. The input layer consists of 20 neurons, which is determined by the maximum number of stages in the data paths. The number of neurons in a hidden layer and the number of hidden layers are adjustable parameters. They can impact the prediction accuracy of the BPNN model. The transient pulse propagation probability calculated by the BPNN model is significantly different from the results of SPICE-level simulations when the number of neurons in one hidden layer is lower (5 to 10). The prediction accuracy is less than 0.6. With an increase in the number of neurons in the hidden layer, the model's prediction accuracy is significantly improved. When the number of neurons exceeds 15, the calculation accuracy of the BPNN model can approach 0.9. However, the prediction accuracy does not improve any further when the number of neurons exceeds 20. Instead, the training time and prediction time increase significantly. In particular, when the number of neurons in the hidden layer reaches 23, the model's prediction accuracy is reduced by 2% to 5%. There was overfitting during the training of the BPNN model. Therefore, the hidden layer consists of 15 neurons. This ensures that the calculations are highly accurate and also allows for a more efficient training and prediction time. Furthermore, the model's prediction accuracy does not significantly improve as the number of hidden layers increases. However, including additional connection weight values required significant adjustments, which led to a substantial increase in training time. Therefore, there is only a single hidden layer used to construct the BPNN model. The output layer consists of 10 neurons, which is determined by the range of propagation probability. The input vectors of the BPNN are the probabilities of transient pulse propagation along the circuit path. The output value of the BPNN is the probability that a transient pulse can propagate to a flip-flop. The basic neuron is activated by the sigmoid function:

$$f(x_i) = \frac{1}{1 + e^{-x}} \quad (3)$$



**Figure 2.** The BPNN structure used in the paper.

Based on Equation (3), the neurons in the input layer can be calculated using the following equation:

$$f(P_{Ci}) = \frac{1}{1 + e^{-P_{Ci}}} \quad (4)$$

The input values of neurons in the hidden layer are determined by the output values of neurons in the input layer. The neurons in the hidden layer can be calculated by the following equation:

$$N_{j,hidden} = \sum_{i=0}^{M-1} w_{ij} f(P_{Ci}) \quad (5)$$

where  $w_{ij}$  represents the connection weight value between the input layer and the hidden layer.  $N_{j,hidden}$  represents the output value of the hidden layer neuron. Similarly, the neurons in the output layer can be calculated using Equation (5), and the transient pulse propagation probability to flip-flops can be determined:

$$P_{FF_k} = \sum_{j=0}^{N-1} w_{jk} N_{j,hidden} \quad (6)$$

The most important aspect of BPNN is training the connection weight value  $w_{ij}$  and  $w_{jk}$ . These connection weight values significantly affect the accuracy of evaluating transient pulse propagation. In this paper, several benchmark circuits from the ISCAS 85 suite are selected. The ISCAS '85 benchmark circuits are ten combinational circuits provided to authors at the 1985 International Symposium on Circuits and Systems. They have subsequently been used by many researchers as a basis for comparing results in test generation. The selected circuits are used to create a training set. The training set is used to calibrate connection weight values. A benchmark circuit structure is shown in Figure 1. It is used to illustrate how to generate the training set. Firstly, one circuit instance is randomly selected, such as C0. Based on the C0, circuit instances C1, C2, and C3 are extracted because they are part of the data path. The probabilities of transient pulse propagation for  $P_{C1}$ ,  $P_{C2}$ , and  $P_{C3}$  are determined. Secondly, a SPICE-level simulation tool is used to simulate the propagation of transient pulses in the benchmark circuit. The input value of the circuit changes randomly with each clock cycle, allowing the value in each circuit instance to be altered. A dual exponential current source is then injected into the C0. The equation of the dual exponential current source can be shown in our previous work [28]. The SPICE-level simulation tool is used to determine whether the transient pulses can propagate to flip-flop 1. This process is repeated multiple times (such as 1000 times) to count the number of pulses that successfully propagate to flip-flop 1. The propagation probability  $P_{FF_1,simulation}$  is obtained by dividing the count data by the total number of injected transient pulses. Finally,  $P_{C1}$ ,  $P_{C2}$ ,  $P_{C3}$ , and  $P_{FF_1,simulation}$  constitute one datum in the training set. Then, another circuit instance is selected, such as C4, C5 or C6. The above steps are repeated to obtain more data in the training set. During BPNN training,  $P_{C1}$ ,  $P_{C2}$ , and  $P_{C3}$  are used as input data. BPNN calculates the transient pulse propagation probability  $P_{FF_1,prediction}$  through Equations (4)–(6). This data will be different from  $P_{FF_1,simulation}$ . Based on the prediction results  $P_{FF_1,prediction}$  and the simulation results  $P_{FF_1,simulation}$ , connection weight values are calibrated using the following equations:

$$E(w) = \frac{1}{2} \sum_{k=0}^{N-1} (P_{FF_k,prediction} - P_{FF_k,simulation})^2 \quad (7)$$

$$w_{ij,new} = w_{ij,old} - \eta_1 \frac{\partial E(w)}{\partial w_{ij,old}} \quad (8)$$

$$w_{jk,new} = w_{jk,old} - \eta_1 \frac{\partial E(w)}{\partial w_{jk,old}} \quad (9)$$

In this paper, parallel simulation is used to accelerate the generation of training data. The cost to obtain the training data is no more than 9 h for each test circuit. Approximately 12,000 training data were generated through the simulations mentioned above. In total, 60% of the data was used to train the BPNN model, and the remainder was used for model validation. The prediction accuracy of the model is calculated using the Equation (10).  $P$  represents the precision value of the prediction.  $TP$  represents the number of positive predictions that are correct, while  $FP$  represents the number of positive prediction errors. The calculation results are detailed in Table 1.

$$P = \frac{TP}{TP + FP} \quad (10)$$

**Table 1.** The results of the training.

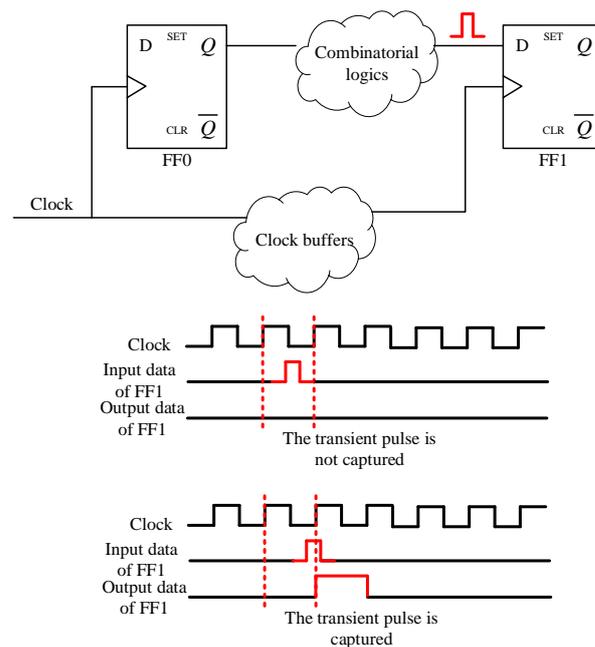
Transient Pulse Propagation Probability Range	Prediction Precision Value
0.1	0.914
0.2	0.922
0.3	0.904
0.4	0.893
0.5	0.877
0.6	0.911
0.7	0.864
0.8	0.844
0.9	0.857
1.0	0.821

### 3.2. The Transient Pulse Capture Evaluation

Another important aspect of SER evaluation is the capture of transient pulses. When a transient pulse arrives at the input pin of flip-flops, such as FF1 in Figure 1, it needs to meet a certain signal–clock relationship to be captured. If the transient pulse is not captured by flip-flops, it will not alter the stored value of the flip-flops and will not result in a soft error. Figure 3 shows the relationship between the transient pulse and the clock waveform. The capture of transient pulses depends on both the width of the pulse and the period of the clock. The probability of capturing transient pulses in flip-flops can be calculated using the following equation:

$$P_{capture,FF_k} = \frac{T_{width}}{T_{period}} P_{FF_k,prediction} \quad (11)$$

where  $P_{FF_k,prediction}$  is calculated by the BPNN.  $T_{period}$  represents the clock period, while  $T_{width}$  denotes the transient pulse width. Since the incident time of high-energy particles is random, it is also random whether the transient pulse and the clock period satisfy the signal–clock relationship. Therefore, a random function in the range of 0 to 1 is used to determine whether the transient pulse is captured by flip-flops. For each flip-flop affected by the transient pulse, the random function generates a value. If the random value is lower than the transient pulse capture probability  $P_{capture,FF_k}$ , the transient pulse can be captured by flip-flops. On the contrary, the transient pulse is not captured when the random value exceeds the probability of capturing the transient pulse.

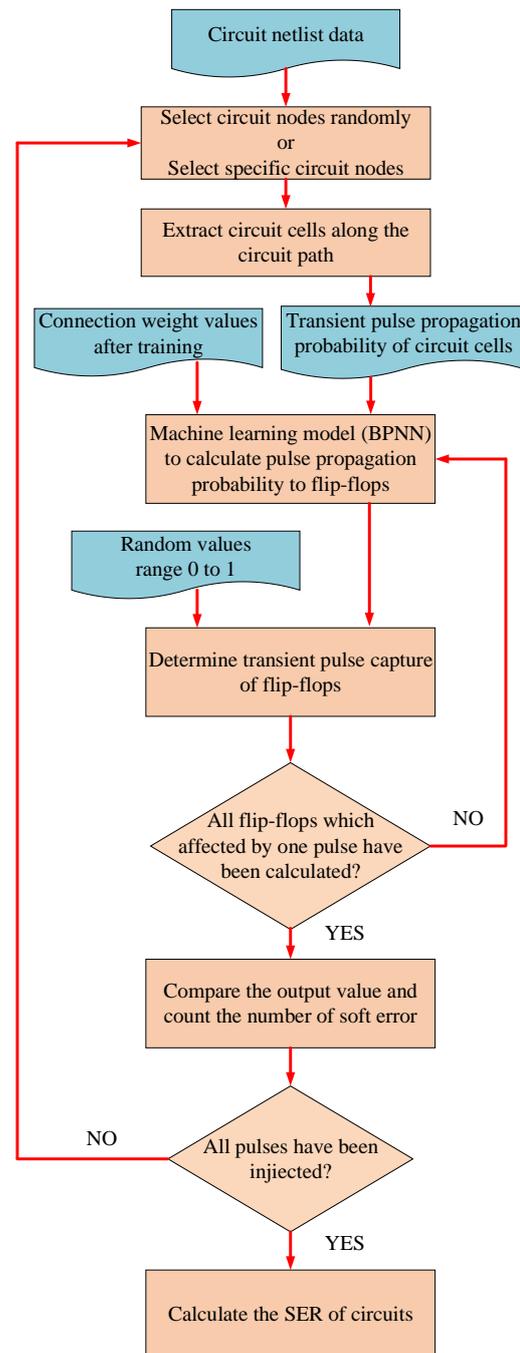


**Figure 3.** The signal–clock relationship to capture a transient pulse.

#### 4. The SER Evaluation Approach

Based on the above SER evaluation principles, a machine learning-based SER evaluation approach is proposed. The basic flow of the proposed approach is shown in Figure 4.

The gate-level netlist of the circuit serves as an input file for the proposed evaluation approach. Before starting SER evaluation, the number of transient pulses that need to be injected is determined based on both the incident particle flux and the area of the circuit (the layout area or the sum of all instance areas). For instance, if the flux of the incident particles is  $1 \times 10^7$  ions/cm<sup>2</sup> and the circuit's layout area is 1 mm<sup>2</sup>, it indicates that  $1 \times 10^5$  ions will strike the circuit. Therefore, when performing SER evaluation, the proposed approach also needs to evaluate the soft errors that occur in the circuit after  $1 \times 10^5$  transient pulse injections. In addition, since the location of the incident particle is random, its impact on the circuit instance is also random. Therefore, for each transient pulse injection, the proposed approach first randomly selects a circuit instance based on the circuit netlist. This means that the circuit instance is affected by the incident particles, resulting in the production of a transient pulse. Secondly, for each data path, all connected logic instance types from the selected instance to flip-flops are extracted. Each logic instance type is then converted into a probability of transient pulse propagation. It is important to note that since the selected logical instance may affect multiple flip-flops, it is often possible to generate multiple input data for the machine learning model in the second step. Thirdly, the data are inputted into the calibrated BPNN model, and the propagation probability of the transient pulse to a flip-flop is calculated using Equations (4)–(6). Fourthly, Equation (11) is used to determine whether the transient pulse will be captured by the flip-flop based on the calculated propagation probability. If the result calculated in Equation (11) is less than the random value generated by the random function, the transient pulse is considered to be captured by the flip-flop. The number of soft errors has increased by one. Fifthly, once all affected flip-flops have been traversed, the number of soft errors in the circuit caused by a transient pulse can be determined. After calculating all transient pulse injections, the total number of soft errors can be determined under a specific incident flux condition. The soft error rate of the circuit can be calculated.



**Figure 4.** The basic flow of the proposed approach.

A comparison between the proposed approach and other conventional evaluation approaches is shown in Table 2. The proposed approach only uses the BPNN model to obtain SER evaluation results. It does not realistically simulate the transient pulse propagation and capture using circuit-level simulation tools. The proposed approach can reduce the run time of SER evaluation and is not limited by the size of the circuit. It is worth noting that the proposed approach not only obtains the SER of the evaluated circuit. It is also useful for locating highly sensitive circuit nodes in the evaluated circuit. For instance, specific circuit nodes are selected in the proposed approach. Then, the SER flow runs to obtain the SER of specific circuit nodes. Compared to the calculated results, the nodes of the high-sensitive circuit are located.

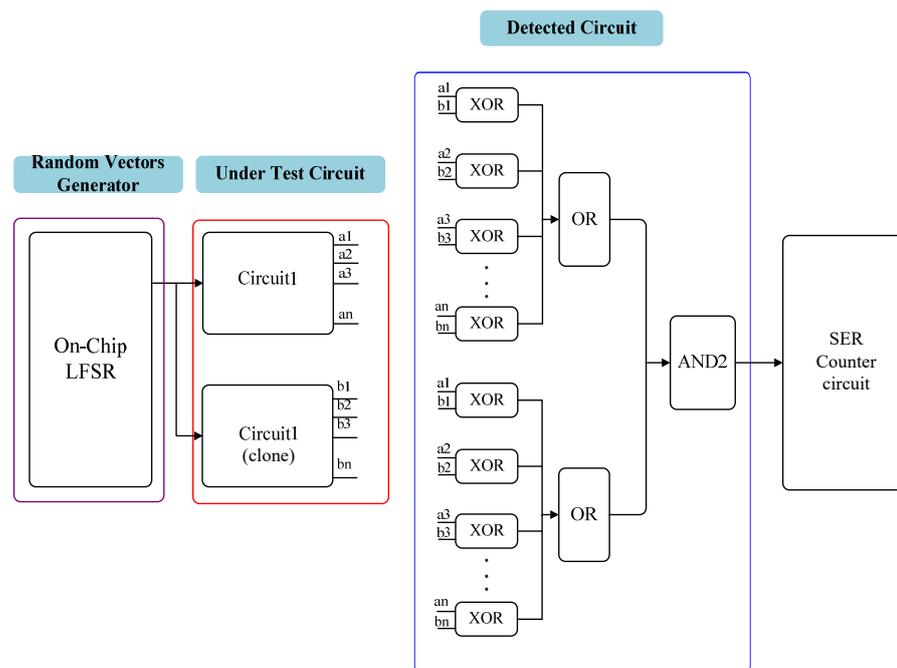
**Table 2.** Comparison of the proposed approach with other state-of-the-art approaches.

SER evaluation approach	The transient pulse generation evaluation	The transient pulse propagation evaluation
SPICE-level simulation approach	The dual exponential current source, etc.	Circuit-level simulation tools
TCAD-level simulation approach	Ionization charge distribution model Carrier transport equation, etc.	Circuit-level simulation tools
Monte Carlo-based simulation approach	Nested sensitive volumes model Drift diffusion equation, etc.	Circuit-level simulation tools
The proposed approach	Pulse width data that vary with LET	Machine learning model

### 5. The SER Evaluation Approach Validation

#### 5.1. Test Chip Design and Experimental Setup

A SER test structure was designed using commercial CMOS technology to investigate the accuracy of the proposed approach. The schematic of the SER test structure is shown in Figure 5. It consists of one random vector generator, two test circuits, and one SER detection circuit. The random vector generator (Linear Feedback Shift Register, LFSR) is used to create the input vectors. The test circuit consists of combinational logic instances and flip-flops. Note that two test circuits have the same topology and layout structures. However, they are spaced out widely to ensure that an incident particle only impacts one test circuit, as shown in Figure 6. The input pins of two test circuits are connected to the random vector generator. It ensures the test circuits have the same input vectors. The SER detection circuit consists of several XOR-gate instances and OR-gate instances. The XOR-gate instances compares the output values of two test circuits. If a test circuit is irradiated by incident particles, the output values are changed. However, the other test circuit is not impacted by incident particles; it can produce correct output values. The XOR-gate instance produces a 1 due to the different output values. The soft error induced by the incident particle is propagated to the SER counter circuit and satisfied.



**Figure 5.** The schematic of the SER test structure.

A test chip with three SER test structures was fabricated using commercial 65 nm CMOS technology. The detailed test chip layout is shown in Figure 6. The test chip was irradiated with heavy ions. Four heavy ions with different parameters were chosen, as shown in Table 3. The heavy-ion dose rate was  $1 \times 10^4$  ions/cm<sup>2</sup>/s, and the flux was  $1 \times 10^7$  ions/cm<sup>2</sup>. Before the radiation experiment, the cover plate from the test chip was removed. The front side of the chip was positioned within the range of the ion beam's influence. During radiation experiments, the ion beams randomly strike their respective targets. Some ions strike the test chips and generate transient pulses. The test system consisted of a test chip and other necessary chips, such as field-programmable gate arrays (FPGAs) and serial communication chips [29,30]. FPGAs connected all signal ports (input, output, and clock) of the test chip to provide input and clock signals. They were also used to capture output signals when the test chip was irradiated. After conducting heavy-ion experiments, the error counts were exported to the computer using the serial communication interface.

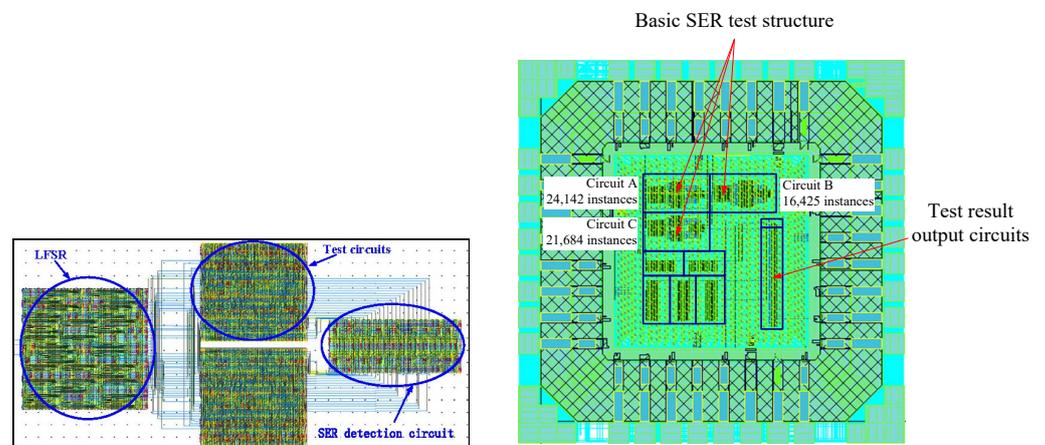


Figure 6. The basic SER test structure layout and the detailed test chip layout.

Table 3. Heavy ions used in the experiment.

Ion	Energy at the Silicon Surface (MeV)	Effective LET (MeV·cm <sup>2</sup> /mg)	Range (um)
Cl	165	15.2	51.8
Ti	185	21.2	37.9
Ge	205	37.6	35.5
Kr	835.5	99.8	41.2

### 5.2. SER Evaluation Setup

The proposed evaluation approach and the SPICE-level evaluation approach were used to investigate the SER of test circuits. The gate-level netlist of three test circuits serves as an input file for the evaluation approaches. The number of transient pulse injections per test circuit is determined by dividing the particle flux by the layout area of the test circuit. The position and moment of transient pulse injection are random. This is due to the fact the location and momentum of the incident particles are random during radiation experiments. The width of transient pulses injected into the test circuit is set to 100 ps, 200 ps, 350 ps, and 500 ps, respectively. It represents the various pulse widths generated by different particles. These data were determined through our previous transient pulse measurements [31–33]. For each test circuit, the number of soft errors can be obtained when the evaluation tool completes the transient pulse width injection simulation. According to the number of soft errors, the soft error cross-section can be calculated using the following equation:

$$SER = \frac{N_{error}}{f_{ions} \times N_{instances}} \quad (12)$$

where  $N_{error}$  represents the number of soft errors that is calculated by the evaluation approaches.  $f_{ions}$  represents the flux of ions.  $N_{instances}$  represents the total instance number of test circuits.

### 5.3. SER Evaluation Results Comparison

The evaluation results of the proposed approach and the conventional SER evaluation approach are compared first. The connection weight values were saved after training the BPNN model. They are imported again into the BPNN model during the evaluation of test circuits. The BPNN model is used to calculate the pulse propagation probabilities in circuits A, B, and C. The calculated results are compared with the transient pulse propagation probabilities simulated by the circuit-level simulation tool. The prediction accuracy is calculated using Equation (10) and the results are shown in Table 4. The average prediction accuracy of the three test circuits is approximately 0.8. Although the three circuits have different circuit structures, the trained BPNN model can still accurately calculate the probability of transient pulse propagation.

**Table 4.** The prediction accuracy of three test circuits.

Transient Pulse Propagation Probability Range	Circuit A Prediction Precision Value	Circuit B Prediction Precision Value	Circuit C Prediction Precision Value
0.1	0.832	0.807	0.821
0.2	0.829	0.811	0.825
0.3	0.813	0.824	0.817
0.4	0.824	0.803	0.813
0.5	0.809	0.795	0.808
0.6	0.805	0.792	0.811
0.7	0.789	0.801	0.804
0.8	0.775	0.789	0.796
0.9	0.764	0.773	0.792
1	0.765	0.768	0.788

Figure 7 shows the comparison between the evaluation results and experimental results. The evaluation results obtained by the proposed approach show good consistency in both trend and order of magnitude. The difference between the results obtained using the proposed approach and the experimental results is calculated. The average value is 23.5%, which is 7.5% higher than that between the conventional evaluation approach and the experimental results. When the LET value is 15.2 MeV·cm<sup>2</sup>/mg, there is a greater discrepancy between the simulation results and the experimental results. With the increase in LET value, the simulation results are in good agreement with the experimental results. Some reasons may cause this difference. The first reason is that the proposed approach does not consider the transient pulse reshaping and reconvergence. Transient pulse reshaping or reconvergence results in a change in the width of the transient pulse, which in turn change the data value of  $T_{width}$  in Equation (11). Circuit-level simulations are used to investigate the difference in circuit A at low LET values. When particles strike most instances, it only generates a transient pulse that propagates to the input of the flip-flop. However, when a particle strikes a specific instance with a large fanout, although it only produces one transient pulse, more than one transient pulse is propagated to the input of the flip-flop due to pulse reconvergence, as shown in Figure 8. For the proposed approach, it is still evaluated based on the pulses that propagate independently on different data paths. As a result, the evaluation results may not accurately reflect soft errors and may differ from the experimental results. When the LET value increases, the transient pulse width generated by the ions also increases. It reduces the change in the width and number of transient pulses caused by the pulse reconvergence. The evaluation results obtained using the proposed evaluation method are closer to the experimental results.

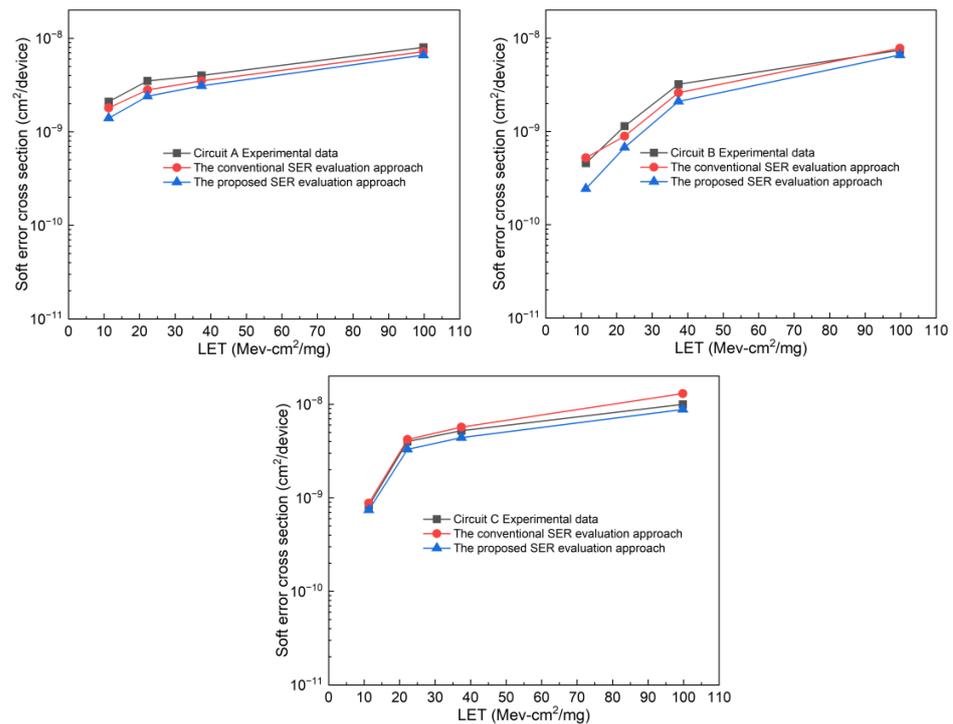


Figure 7. The simulated SER results with different evaluation approaches.

The other reason for this difference is the evaluation accuracy of the transient pulse propagation. The transient pulse propagation is evaluated using the BPNN. The training accuracy of connection weight values is the key factor that affect the evaluation accuracy. In our previous works, we observed a significant decrease in the prediction precision value when the probability of transient pulse propagation exceeded 0.7. It indicates that the propagation probability obtained by the BPNN are significantly different from the conventional transient pulse simulation results [34]. Because fewer combinational logic cells with large circuit stages have a high probability of transient pulse propagation, the training set does not include enough data, and the connection weight values are not effectively trained for this situation. Increasing the train set data can improve the training accuracy of connection weight values. It may be an effective way to solve this difference.

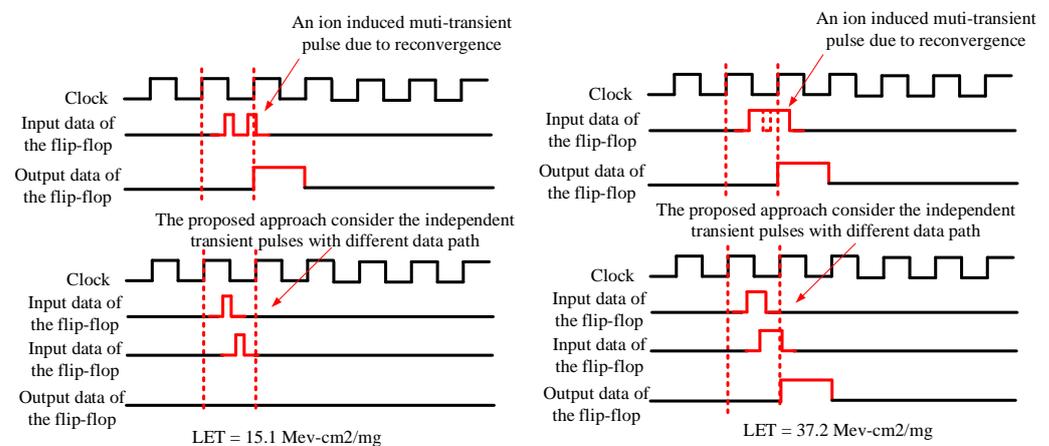
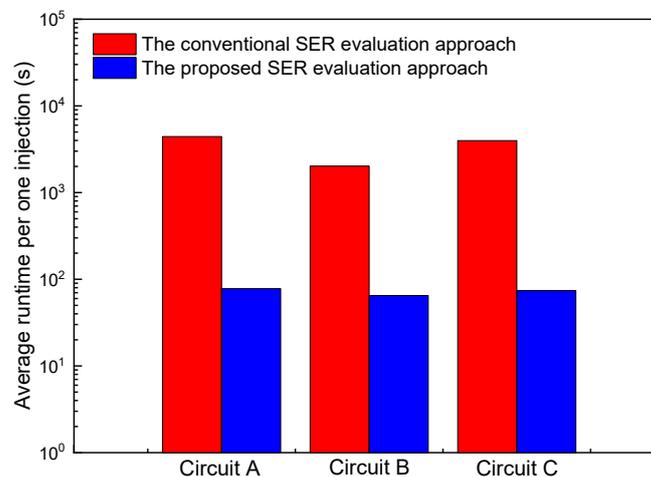


Figure 8. The width and number variation of transient pulses due to pulse reconvergence.

Figure 9 shows the average simulation runtime of the proposed approach and the conventional SER evaluation approach. For the conventional evaluation approach, the circuit-level simulation tool is used to simulate the propagation of transient pulses. This

simulation helps determine if the flip-flops can capture the transient pulses. Although the size of the test circuit is only 10,000 instances, it results in a significant increase in time cost for a single circuit-level simulation. The significant time cost greatly reduces the evaluation performance of the conventional evaluation approach. For the proposed approach, a machine learning model (Equations (4)–(6)) is utilized to calculate the probability of transient pulse propagation. Subsequently, the transient pulse is captured using the transient pulse probability equation (Equation (11)). The proposed method can determine the soft error of the circuit solely through equation calculations. Therefore, the proposed method can significantly reduce the time required and enhance the performance of soft error evaluation.

In addition, Circuit C has only 5000 more instances than Circuit B. However, the simulation time for the conventional evaluation methods is nearly doubled. When the circuit size increases further, the evaluation time of traditional evaluation methods becomes unacceptable, limiting the size of the circuit that can be supported by this approach. For the proposed approach, as the circuit size increases, the evaluation time only shows a slight improvement. The proposed approach can support larger scale circuits, which improves the performance of the soft error evaluation method.



**Figure 9.** The average simulation runtime of two SER evaluation approaches.

## 6. Conclusions

This paper has presented an approach to evaluate the SER of integrated circuits. A machine learning model (BPNN) is implemented in the proposed approach. It helps to evaluate the transient pulse propagation and capture. Some commercial integrated circuits are designed and fabricated to validate the capability of the proposed approach. Compared to experimental data and the conventional SER evaluation results, the proposed approach also demonstrates a strong correlation in terms of trend and magnitude with the improvement in simulation runtime. The proposed evaluation tool has been used to evaluate the SER of circuits with more than 10,000 gates, which demonstrates that the proposed model can be applied to evaluate logic circuits with more than 10,000 gates. It is useful for circuit design and radiation hardening.

**Author Contributions:** Conceptualization, test chip design, writing—original draft preparation, R.S.; writing—review and editing, J.S.; heavy-ion experiment, Y.C. and J.C.; experimental results analysis and validation, B.L. and Z.W. All authors have read and agreed to the published version of the manuscript.

**Funding:** This research was funded by the National Natural Science Foundation of China (Grant No. 62174180) and the National University of Defense Technology research project (Grant No. ZK20-11).

**Institutional Review Board Statement:** Not applicable.

**Data Availability Statement:** The datasets used and/or analyzed during the current study are available from the corresponding author on reasonable request.

**Acknowledgments:** We wish to acknowledge the HI-13 team and the HIRFL team for heavy-ion experiment support.

**Conflicts of Interest:** The authors declare no conflict of interest.

### Abbreviations

The following abbreviations are used in this manuscript:

BPNN	back propagation neural network
SER	soft error rate
SPICE	Simulation Program with Integrated Circuit Emphasis
LFSR	Linear Feedback Shift Register
TCAD	Technology Computer-Aided Device

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