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Implementation of Background Calibration for Redundant FLASH ADC

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Abstract: Flash converters are suitable analog-to-digital converter architectures for high-speed applications. However, the benefits in terms of the frequency of smaller technology nodes are hampered by variability, which necessitates the use of large transistors. Comparator redundancy was introduced to overcome this trade-off; the best comparators were selected upfront (either at start-up or in the factory), and the unused comparators could be switched off. This work studies the possibility of performing comparator selection in the background concurrently with normal conversion to increase the converter lifetime. Thus, the system can automatically recover its performance from drifts or failures due to aging, temperature, etc. This paper proposes an embedded solution that includes a calibration stimulus generator (which only requires some external passive elements) and develops system design requirements. In addition, mathematical equations and error sensitivities of the system elements were derived. A 6b flash converter is implemented in UMC180nm technology, and transistor-level simulations of the system are provided to demonstrate the feasibility of the proposed system.

Keywords: calibration stimulus generator; control unit algorithm; flash converter; online calibration; redundancy system

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1. Introduction

Data converters can be used in almost any modern electronic system to communicate electronic devices with the physical analog world [1]. Many different architectures exist, and their selection depends on application and design requirements [2]. For analog-to-digital converters (ADC), the so-called flash architecture is known to be the fastest (both for latency and throughput); thus, it is suitable for high-speed applications, typically in communication [2,3]. It consists of a references generator, comparators vector (one per quantization level), and a thermometer-to-binary encoder. The length of the comparator vector is determined by the converter resolution (i.e., N-bits converter implies $2^N - 1$ comparators). Obviously, for such a straightforward architecture, the comparator circuit is the most critical block [3]. Small and fast transistors must be used to satisfy the highest speed requirements. The use of small transistors also reduces power consumption and total area. Unfortunately, small transistors suffer from process variability, which affects their thresholds. This effect translates into a random offset of the comparators, which in turn degrades converter linearity [4].

Many methods have been developed to solve this problem. The most straightforward approach is to sacrifice area and power using larger transistors. However, such a solution does not maximize the benefits of technology scaling. Recently, trimming, foreground calibration, and background calibration were developed as alternative solutions. The trimming method permits the correction only once after calibration. In the foreground calibration; the error estimation and corresponding correction parameter are conducted

while the conversion process is idle. In the background calibration; any deviations in the converter output can be corrected simultaneously [5].

An attractive solution is to introduce comparator redundancy. This solves the problem by breaking the trade-off between speed and accuracy. This was achieved by implementing replicas of small comparators for each level. Using a calibration system, the real transition voltage is determined for each comparator, and a control unit assigns the best comparator for each level to the conversion operation. The remaining candidates were then switched off.

Figure 1 shows the differences between the original and modified converter block diagrams. In this approach, the use of small comparators allows the speed requirements of the design to be satisfied. The dimensions of the redundant comparator bank are determined to ensure an acceptable yield, depending on the mismatch analysis and standard deviation of the comparator offset. Moreover, if the standard deviation of the comparator offset is superior or in the order of the least significant bit (LSB) of the converter, the comparators initially assigned to adjacent levels can also be considered candidates for the level. In addition, the overall area and power after adding calibration and extra comparators are still less than those of the direct approach and can even be reduced with upcoming technologies. An example of this approach can be found in [4]. Note that this redundancy method can be applied to domains other than the flash converters. For example, the concept of selecting the best candidate was applied to a differential pair in [6].

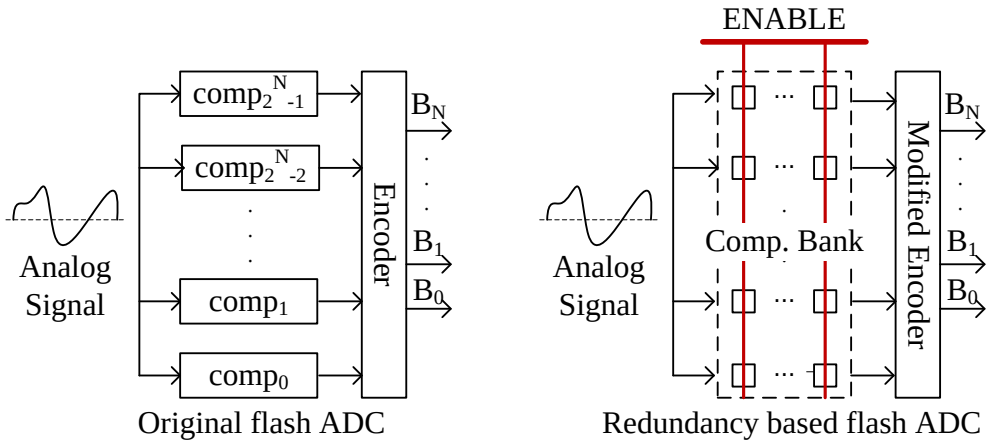

Figure 1. Block diagram that shows the difference between the original converter and that with a redundancy system.

In this study, we propose a robust, almost on-chip calibration system to perform comparator selection. Such a calibration system relies on the generation of an exponential signal as a calibration stimulus and is thus mainly on-chip, except for a couple of passive components and the system control. As a result, this opens the door to periodic in-field calibration or even concurrent background calibration, as will be shown later. Running the calibration continuously increases the lifetime of the system and makes it more robust to any sudden failure owing to aging or temperature drifts. A comparison between this work and some available works is summarized in Table 1.

The remainder of this paper is organized as follows: the next section describes the proposed system. More details about the calibration algorithm and design of the calibration circuit are explained in Sections 3 and 4, respectively. Section 5 presents simulations to verify this idea. Finally, the conclusions are presented in Section 6.

Table 1. Comparison between the different available background calibration techniques and this work.

Ref.	Advantages	Drawbacks
[7]	Uses only one additional comparator to replace the one being calibrated. The calibration is performed using successive approximation (fast). High working frequency achieved and measurement results obtained. Low overhead.	Has a low resolution (4b). Comparator calibration is performed at zero input, which may introduce errors for levels at the extremes. There is no sufficient information about the calibration circuit design.
[8]	High resolution from a low-resolution flash converter. High working frequency was achieved and measurement results were obtained.	This is not a FLASH converter strictly speaking. There is little information about the calibration circuit design.
[9]	No additional comparator needed. Elegant statistical estimation of the offset (random chopping). High precision was achieved and measurement results were obtained.	Adjusts the offset controlling the capacitive charge at the output nodes of the latch (slows down the latch). Statistical estimation puts constraints on the input signal density.
This work	The calibration stimulus is low-cost, based on external passives. The system corrects any static error (including the level references). The comparators are calibrated in their operating conditions. The system is resilient against failures thanks to redundancy [10]. A complete error study for the design parameters is provided. The design can accommodate changes in the full-scale range and pre-distortion.	It is a prototype to demonstrate the idea. It was not designed for maximum performance so it is difficult to compare it with the state of the art in this respect. Redundancy has an area penalty (in our case, 8×).

2. Proposed System

This section explains the essential modifications that must be performed on the converter to introduce redundancy and permit the online calibration and self-healing of the system. In addition, we describe the main hardware required to implement the function and design guidelines. The proposed system can be divided into three main parts: the converter block, calibration block, and control unit. The converter block is a basic flash converter system with some modifications. The calibration block is responsible for generating the calibration stimulus and delivering it to the system. The control unit is responsible for the work organization and results analysis and prevents any overlap between the two tasks (calibration and conversion). The description and design details of each block are as follows.

The basic redundancy system shown in Figure 1 consists of a references generator, a bank of comparators, and a modified encoder. Converter references were generated in our system using the basic resistive ladder. The extremities of the resistive ladder are connected to two voltage sources to determine the full scale of the converter. Note that it can be implemented using any other technique without affecting the system. The bank of comparators is formed by a set of small fast comparators. The comparator design was relatively simple. The main design goal is to minimize the cell size and maximize the operating speed. In this design, the comparator offset (related to mismatching) is not a concern, owing to the introduction of redundancy. However, additional elements are required to complete the new functionality. Each comparator can be assigned to either a conversion or calibration process or switched off. The comparator circuit input can be connected to either the analog or calibration stimuli. Simultaneously, the output

can be delivered for conversion or calibration analysis. Both switching operations were implemented using local multiplexers. If the comparator was not connected to either function, it was switched down to save power. CMOS switches were selected to implement the switching function to ensure good information delivery throughout the input range. The gates of the switch transistors are connected to the control signal, where the analog/calibration signals flow between the drain and the source. Once the speed requirement of the comparator circuit is achieved, the offset standard deviation can be characterized by a Monte Carlo simulation to properly determine the dimensions of the bank to complete the desired yield, as explained in [10]. The total number of comparators in the bank is referred to as *C* in the remainder of this paper. It depends on the redundancy factor (the number of comparators implemented per level), as well as the number of comparators that must be added at the extremities of the full scale to maintain a high probability of finding an adequate candidate. After determining the next block dimensions and their corresponding input capacitances, output buffers are added to the comparator circuit. Figure 2 shows the modifications to the original dynamic latch to fit the system requirements.

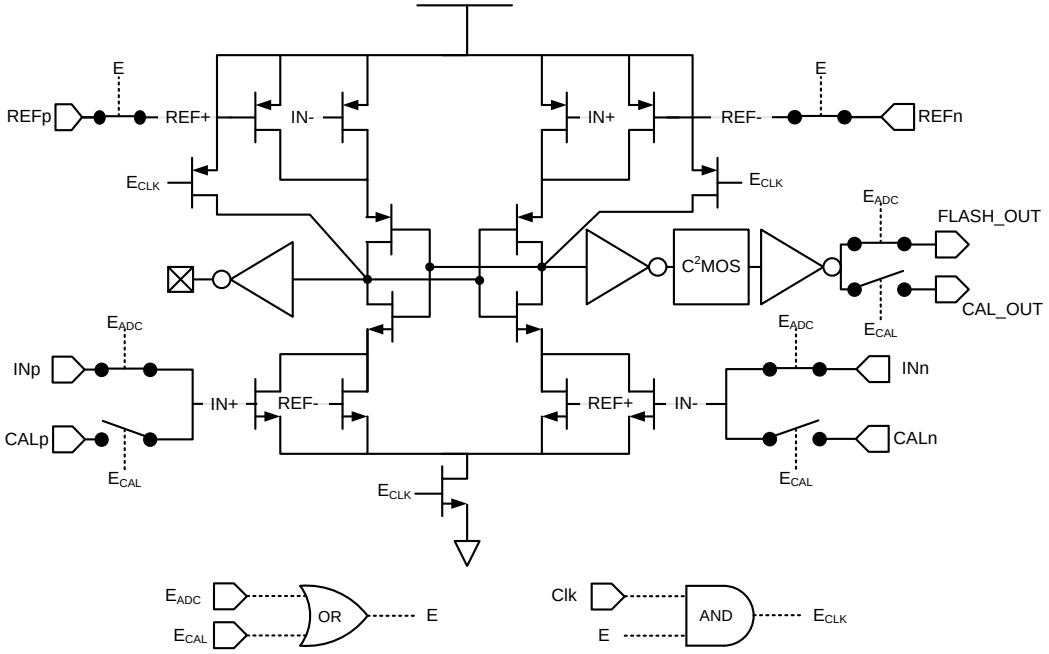

Figure 2. Modified comparator circuit.

As shown in Figure 2, the comparator cell has two control signals, E_{ADC} and E_{CAL}. The first is responsible for incorporating the comparator circuit into the conversion and the second is responsible for incorporating the comparator circuit into the calibration. Normally, there are $(2^N - 1)$ comparators that are active for conversion, one comparator is active for calibration, and the remaining ones are inactive. When $E_{ADC} = E_{CAL} = V_{SS}$, the comparator is inactive and its clock is disabled. The generation of these signals is one of the duties of the control unit, but their values can be saved for each comparator in a memory bank for E_{ADC} and another for E_{CAL}. This is efficient for E_{ADC}, but not optimal for E_{CAL}, as will be explained later. Thus, the E_{ADC} signal of each comparator is saved in a single-bit memory cell. If the memory cell contains "one", this means that the corresponding E_{ADC} is active for the conversion process. If it contains "zero", this means that the corresponding E_{ADC} is reset and hence the comparator cell is disconnected from the conversion process. The memory cells that feed all comparators in the bank are grouped into one memory called "COMP ENABLE MEM". The dimension of this memory is a one-bit memory repeated for the *C* locations. Note that for an N bit converter, this memory has $2^N - 1$ locations containing "one" and the rest containing "zero". In addition, this memory is formed using simple registers. This can be edited whenever the

calibration results change. The E_{CAL} signal will be explained when discussing calibration. The next step in the conversion process is to generate a thermometer code. The well-known weighted summer encoder [11] cannot be used directly here, because it adds the output of the calibration comparator. In addition, as explained previously, each thermometer level code can be generated from one of the several comparator candidates in the redundancy system. A multiplexer can be used to select one specific comparator and associate its output to generate the corresponding thermometer level. Because an N-bit flash converter has $(2^N - 1)$ thermometer levels, $(2^N - 1)$ multiplexers are required. The number of inputs for each multiplexer was determined by the number of available candidates for each thermometer level, which was determined as in [10]. Note that this number is not necessarily equal to the redundancy factor, as comparators originally designed for other reference levels can also be considered candidates. The required address length was calculated using the basic formula, log_2 (no. of inputs). Note that the address of a given multiplexer selects candidates for the corresponding thermometer level. This means that the same comparator, which can be a candidate for more than one thermometer level, has different addresses in different multiplexers depending on its candidacy order at each level. The multiplexers group is called "OUT MUX VECTOR" and its output is the converter thermometer code. The select lines of these multiplexers are saved in "MAIN MUX MEM". This memory is similar to the "COMP ENABLE MEM" in the sense that it can be edited whenever the calibration results change, and all its contents are always connected to the "OUT MUX VECTOR". Once the thermometer code is generated, a binary code can be obtained using any thermometric-to-binary converter available in the literature. There were no architectural restrictions.

To summarize the conversion process flow, some comparators were assigned for conversion. The control unit enables these comparators for conversion by activating their E_{ADC} signals. Simultaneously, the control unit selects these comparators to generate the thermometer code of the converter; therefore, they must be selected by the multiplexers of the "OUT MUX VECTOR" and assigned to their adequate levels. Then, the outputs of the multiplexers pass to the thermometric-to-binary encoder, which generates the output digital bits. Figure 3 presents the summary.

The next block in the system was responsible for the calibration process. This process requires a calibration stimulus generator, activation of the comparator under the calibration CUC, and collection of its output for analysis. The calibration stimuli generator generates the stimulus that will be fed to the CUC as differential calibration inputs, which are called CAL_p and CAL_n in Figure 2. The generator design is detailed in Section 4. The activation of the CUC for calibration requires setting its E_{CAL} to V_{DD}. Note that the E_{CAL} signal is zero for all comparators in the bank, except for that of the CUC at the time of calibration. Therefore, it is more efficient to use a decoder rather than a memory bank, similar to that of E_{ADC}. The decoder has C outputs, and the address of $log_2(C)$ bits selects which of the C comparators is assigned $E_{CAL} = 1$ while the rest are assigned $E_{CAL} = 0$. The decoder has an enable signal to switch down the decoder when it is not used (i.e., when no calibration is being performed) to reduce power consumption.

The output of the CUC is delivered to be analyzed by the calibration Finite-State-Machine by a "calibration multiplexer". The CAL_OUT pin of each comparator in the bank was connected as an input for the calibration multiplexer and was driven by the same E_{CAL} signal.

Finally, a control unit is needed to organize the workflow, assign comparators for conversion, prepare CUC for calibration, analyze the calibration results, and most importantly, prevent any conflict between the calibration and conversion processes. This means that the control unit must avoid the selection of the same comparator for the conversion process during its calibration. To minimize the sources of error and open the possibility of trying several versions of the calibration algorithm, we decided to implement the control unit off-chip, in a field-programmable-gate-array (FPGA). However, the control unit can be perfectly implemented on-chip and take full advantage of technology scaling. Indeed, this

redundant self-healing ADC is meant to be digitally friendly. More details regarding the control unit functionality and resources are discussed in the next section.

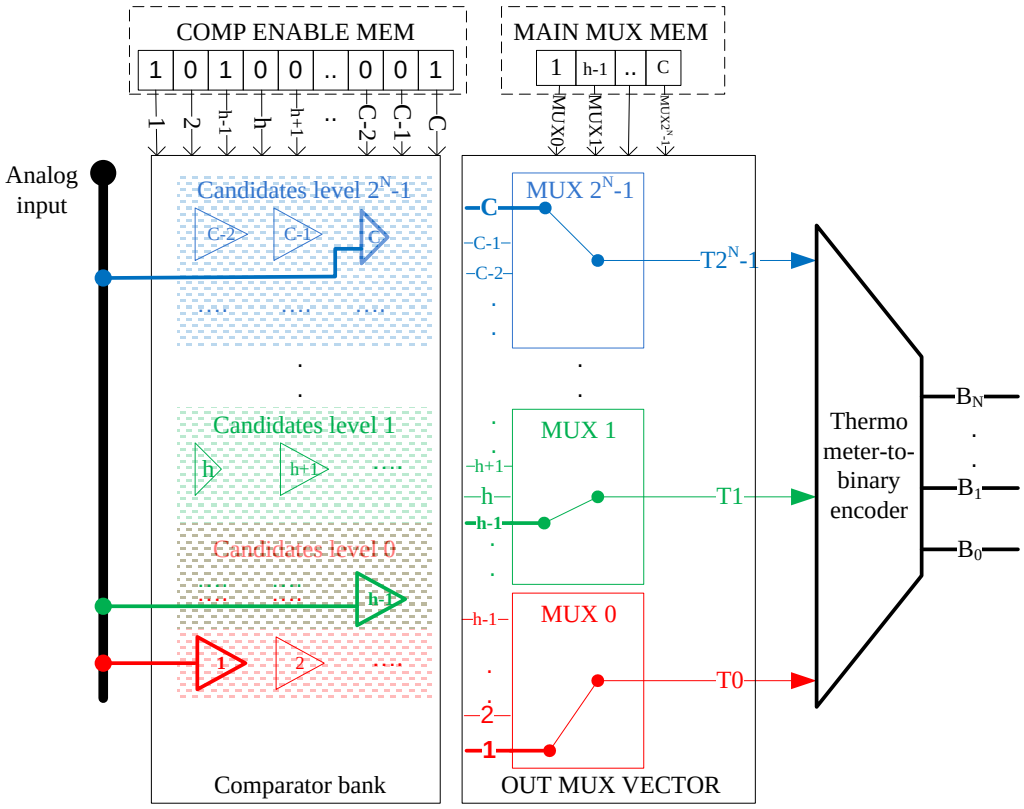

Figure 3. Summary of the conversion process.

Figure 4 shows a block diagram of the proposed system. Note that the line thickness refers to the bus size: thin lines are single data lines and thicker lines are data buses.

To validate this approach, we will consider as a case study the design of a redundant 6b FLASH ADC.

The first step in system design is determining the required redundancy for each reference level and a suitable number of reference levels for each thermometer level. The number of comparators in the comparator bank can be calculated according to the results. Once the bank dimensions are fixed, the "COMP ENABLE MEM", the multiplexers of the "OUT MUX VECTOR", "MAIN MUX MEM", calibration multiplexer, and calibration decoder dimensions are fixed. From the results published in [10], eight comparator redundancies were sufficient, and 32 reference levels were suitable for obtaining each thermometer level. This means that we have 752 comparators in the comparator bank (after adding extra comparators at both array extremes). Therefore, the "COMP ENABLE MEM" dimension was 752 locations $\times$ 1 bit. The "OUT MUX VECTOR" consists of 63 multiplexers with dimensions of 8 select lines $\times$ 256 inputs. The conventional thermometer-to-digital code converter has 63 thermometer levels and 6 digital outputs. The calibration decoder must access 752 comparators; therefore, it has 10 input lines and 752 output lines. It works only when it is enabled; therefore, it requires an enabling signal. In addition, the calibration multiplexer shared the same 10-bit address lines.

The design was implemented using UMC180nm CMOS technology with 1.8 V supply voltage. The full-scale of the converter is selected to be 0.8 V with a common mode of 0.9 V and a sampling frequency of 200 MHz.

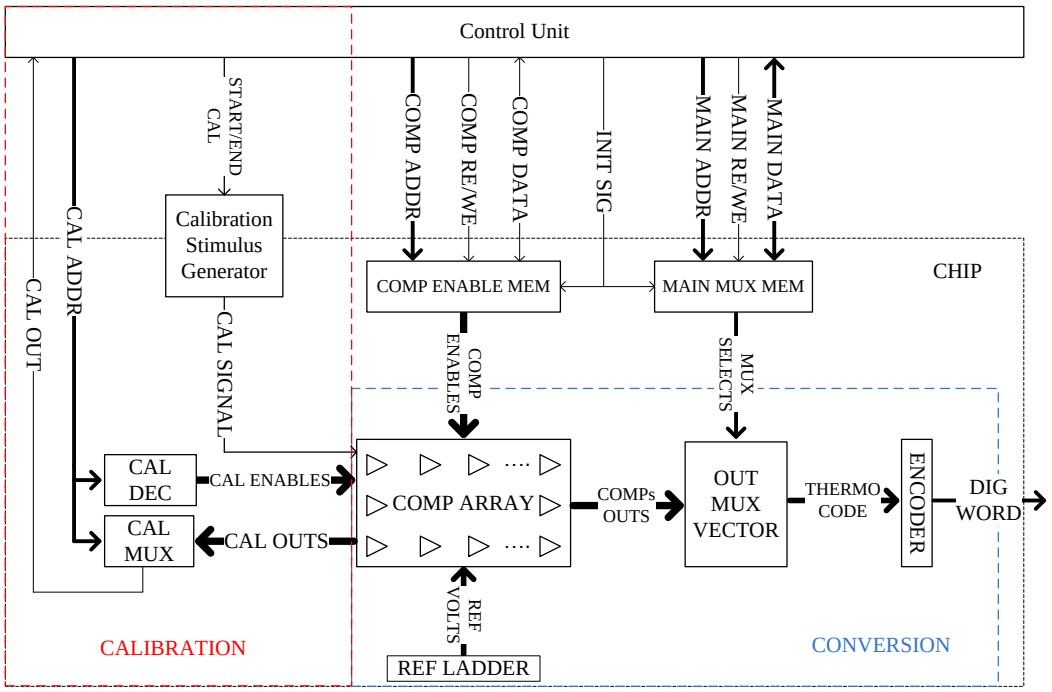

Figure 4. Proposed self-healing redundancy-based flash converter.

3. Calibration Algorithm

The control unit is responsible for organizing the flow of the calibration (evaluating the comparator offset), analysis (identifying the best candidate for each level), and repair (substituting the comparators for the best candidates) processes.

These processes are conducted in the background and run periodically in parallel with the conversion process. Any deterioration in the system performance owing to changes in comparator offsets of reference drifts (because of aging, temperature, etc.) should be solved automatically, with the latency associated with the duration of the calibration cycle. This is valid even under catastrophic comparator failures, as shown in [10]. The control-unit algorithm can be implemented in various forms. Initially, default comparators were assigned for the conversion operation until the calibration results were obtained. This means that at the start-up of the system, the "COMP ENABLE MEM" is set to a predetermined value. Also, the "MAIN MUX MEM" is set to connect these default comparators for the corresponding thermometer levels. In this design, the first candidate for each level was selected as the default candidate for that level. Subsequently, both the conversion and calibration processes start working.

The calibration algorithm consisted of two nested iterative loops. The outer loop cycles through the different thermometer levels of the FLASH ADC, while the inner loop goes through the comparator candidates available for each level. In this algorithm, one can save the error values only regardless of the exact value. The error here means the deviation between the ideal value for that level and the measured one, and the error value is relatively small; therefore, it can be expressed precisely using a small memory size. The size of the error register can be determined by the maximum error that we are willing to tolerate in the system in the worst usage case. Indeed, the redundancy has been sized such that there should be several candidates in 1 LSB around the ideal value. Taking a safety margin, one could thus size the error word length to saturate at $[-2; 2]$ LSBs. The drawback of this algorithm is that the comparators are measured several times because they are candidates not only for the levels to which they are physically attached, but also for adjacent levels. The results show that the full calibration cycle was longer.

Another possible algorithm is to calibrate each comparator in the bank only once. If the exact values of the comparator transitions are stored with sufficient resolution, the

control unit can directly identify the best comparator for each level (and the second best, as we will see later).

From a time perspective, this will reduce the system calibration period, but at the expense of hardware resources. In addition to the size of the transition measurement register, analysis would still require looping across different levels, taking into account which comparators are candidates for which level.

Table 2 summarizes the differences between the two options for the calibration algorithm. The first is the algorithm selected in this study, and the second has a reduced calibration time. For this concrete design, the calibration time for the compact algorithm was 16,128 ×CCT, whereas that of the faster algorithm was 752 × CCT. However, the difference between the required hardware in both cases is a memory with 752 locations. This memory saves the real cross-time of all the comparators in the bank. The resolution of this memory is determined by the acceptable error resolution (ER), time full-scale range, and clock frequency. This implies that for a linear signal, the full-scale time is equal to $V_{DD} \times$ Tclock ÷ ER. For this design, V_{DD} is 1.8 V, T_{clock} is 5 ns and ER is 0.1 LSB. Therefore, the full-scale time was 708.66 ns. This implies that the required word resolution is 10 bits. Therefore, the required memory size in this case is 752 locations × 10 bits words.

Table 2. Comparison between the selected algorithm and the faster one where CCT is single comparator calibration time, NCL is the number of candidates per thermometer level, CHW are common memories in both algorithms (which are ideal cross time memories, best candidates error memories and second best candidates error memories) and RCTMEM is a memory to save the real cross times for all comparators in the bank.

Algorithm	Calibration Time	Hardware
compact	$(2^N - 1) \times$ NCL $\times$ CCT	CHW
faster	$C \times$ CCT	CHW + RCTMEM

As explained in detail in Section 4.1, direct comparator voltage-offset measurement requires complex circuitry, while time-offset measurement can serve this purpose. Therefore, the calibration algorithm was built based on the time-offset measurement.

A flow chart of the calibration, analysis, and repair for each comparator is shown in Figure 5.

- Comparator preparation
  Because the design targets a background calibration scheme, the normal operation of the converter cannot be stopped. Therefore, some comparators were incorporated into the conversion process. Hence, before calibrating any comparator, its status must be verified. This is carried out by reading the contents of "COMP ENABLE MEM" for the comparator ID of the CUC. If the comparator is not involved in the conversion process, it can be directly calibrated. If CUC is active, it must be disconnected from the conversion process. To maintain the calibration in the background, a substitute is required to maintain performance. In addition to the memory bank that stores the ID of the best comparator for each level, another bank is used to save the ID of the substitute candidates (i.e., the second-best comparators for each level). Note that this memory at system start-up is reset to predetermined candidates until the calibration results. Any redundant comparators physically attached to that level can be used as reset values for the best and second-best candidates because they all have the highest probability of providing a good offset value. However, after a complete calibration cycle, a given comparator may be selected for the thermometer level, to which it was not physically attached. If the CUC is active, we must find the level at which it corresponds. Then, we determine the correct substitute. Finding the level is accomplished by reading the contents of the "MAIN MUX MEM". When the corresponding substitute had been determined, it was enabled for conversion, and assigned to the output multiplexer of the corresponding level. Finally, the CUC is

disconnected (disabled) from the conversion to be ready for calibration. In practice, it may occur that a given comparator can be assigned to several levels simultaneously. This is very unlikely because redundancy has been sized to provide several candidates close to the ideal transition. However, to cope with this possibility, we would simply repeat the substitution operation for all levels for which the CUC is found to be active.

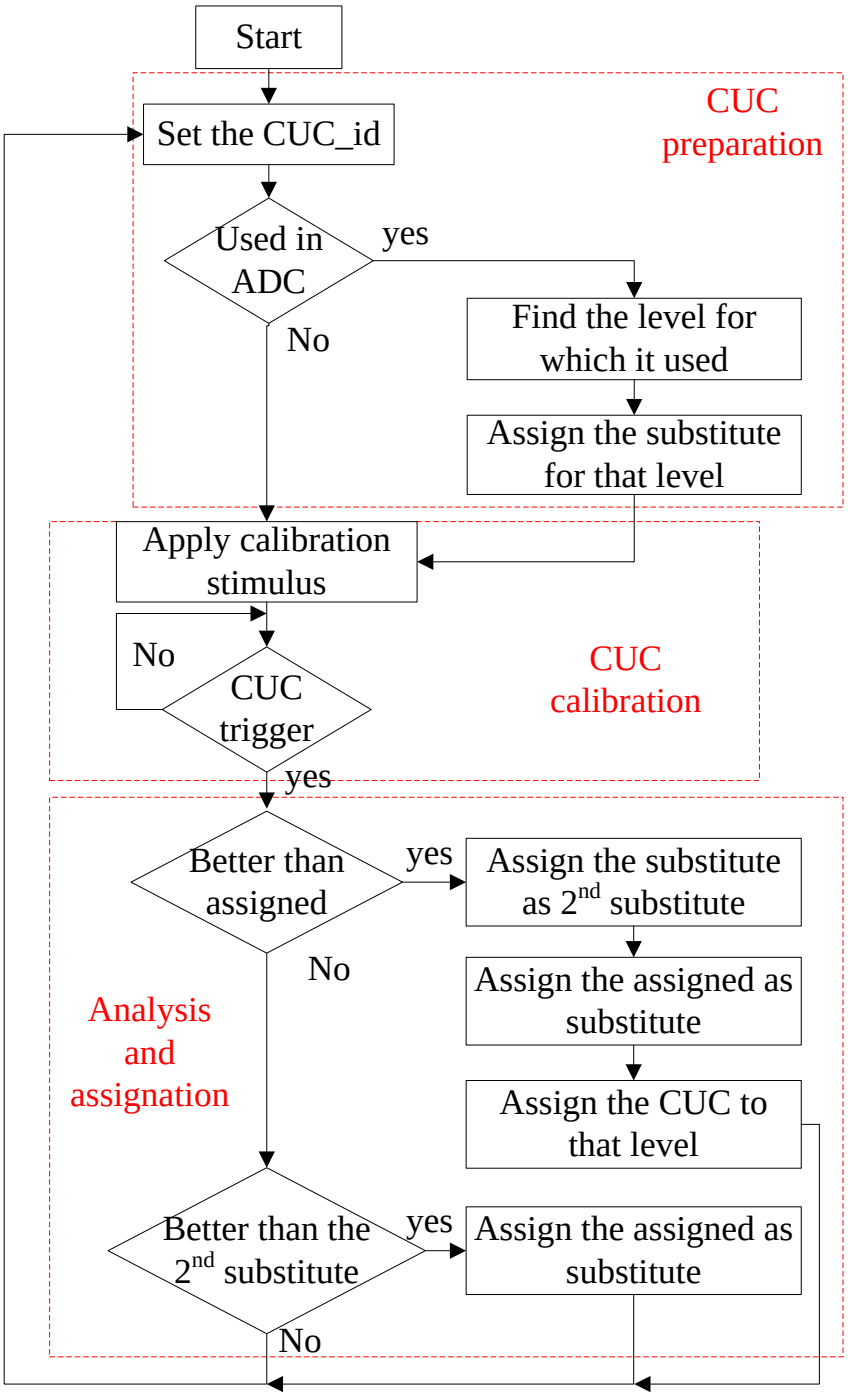

Figure 5. Flowchart of the calibration process.

- Comparator calibration
  In this step, the control unit sends a calibration enabling signal to the calibration stimulus generator, calibration decoder, calibration multiplexer, and calibration counter. When the calibration stimulus generator receives this signal, it starts generating the calibration stimulus and feeds it to the CUC. When the calibration decoder receives this signal, it generates an E_{CAL} signal to connect the CUC for calibration. When the calibration multiplexer receives this signal, it collects the CUC output and delivers it for the analysis. Finally, when the calibration counter receives this signal, it begins counting until it receives the trigger signal of the CUC output, which marks the end of the calibration process for that CUC.
- Calibration result analysis
  Once the output of the CUC is toggled, the calibration counter output is captured and the error value can be computed. This value is then compared with the values of the best and second-best candidates stored for that level. If it is better than the best candidate value, the contents of the best memory, both the comparator ID and error value, are transferred to the second best memory, and the resulting values are saved in the best memory. If the result is better than the second-best candidate, the results are saved in the second-best memory.
- Wrap-up
  The CUC can then disconnect from the calibration process. However, the tasks to be performed depend on the situation: If the CUC is not initially used for any level and is not the new best comparator for the level under calibration, then it is simply disconnected from the calibration stimulus and disabled ($E_{ADC} = E_{CAL} = 0$ in Figure 2). If the CUC was initially used for the level under calibration and remains the best comparator for this level, or if it was initially used for a different level, it is disconnected from the calibration stimulus but remained enabled and connected to the input stimulus ($E_{ADC} = 1$ and $E_{CAL} = 0$ in Figure 2). The address of the output multiplexer(s) for the level(s) that uses the CUC is also modified to select the CUC output. Subsequently, the substitute(s) that had been used during the CUC calibration can be disconnected and disabled. If the CUC is not initially used but happens to be the new best comparator for the level under calibration, the situation is the same as before, with the former best comparator being treated as a substitute. As mentioned above, the probability that a comparator is used for several levels is very low, but not zero. Thus, it may occur that substitute(s) have already been used for other levels. In such a case, when they are connected during the "comparator preparation" step, we must check whether they were already in use. If so, they must not be disabled or disconnected by the end of the cycle.

4. Design of the Calibration Scheme

This section discusses the calibration scheme starting from the selection of the type of stimulus signal passing through its circuit design and its accuracy in reaching the dimensions of the elements.

4.1. Choice of the Stimulus

A generic solution for precisely measuring the comparator offset on-chip requires some medium- to high-resolution DAC [12]. This implies a complex circuity that consumes both area and power. This power must be added to the main converter consumption because the online calibration is always on. If such a DAC uses the same references as FLASH, it can not calibrate the gain error either. This prompted us to investigate the possibility of expressing the offset by using time measurements. The idea is to measure the comparator flip-time and compare it with the ideal value to obtain the error value. A high-resolution counter can be used to measure the absolute cross time, as shown in Figure 6.

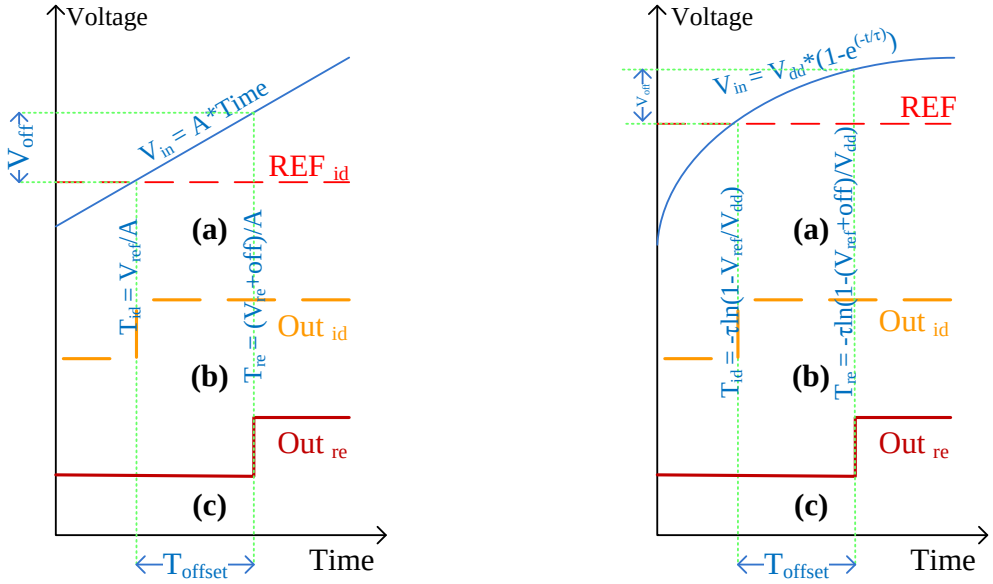

Figure 6. Ideal vs. real comparator response due to ramp input signal and exponential input signal. (**a**) Comparator input signal. (**b**) Ideal comparator response. (**c**) Real comparator response.

For a linear ramp stimulus, as seen in the left part of Figure 6, there is a proportional relation between the voltage offset and the difference between the real and ideal flip times, as given in (1). Therefore, the measurement of the difference between ideal and real flip times can be used to refer to the comparator voltage offset.

$$\text{offset} \propto (T_{re} - T_{id}) \tag{1}$$

If the ideal flip times can be evaluated and stored, the exact value of the ramp slope does not need to be stored, because only a comparison between offsets is necessary.

To guarantee a proper in-field operation, the calibration stimulus must be more robust than the circuit under test. Ideally, it should be immune to process variations. The fabrication of a precise on-chip ramp signal generator can be complex [13] and is likely to be sensitive to external conditions such as temperature. This may require a very careful design of the buffer to feed the loading capacitance [14]. This led us to replace the ramp stimulus with an exponential one. The latter can be implemented with two off-chip passive elements with low-temperature coefficients, while the controlling circuitry (the charging and discharging switches) remains on-chip. The shape of the calibration stimulus is only determined by the exponential time constant and charging voltage; therefore, there are few parameters. Thus, the ideal flip times can be evaluated easily, either computed analytically or precisely measured in the foreground with the real calibration stimulus, which provides a robust solution. The proposed calibration circuit is illustrated in Figure 7.

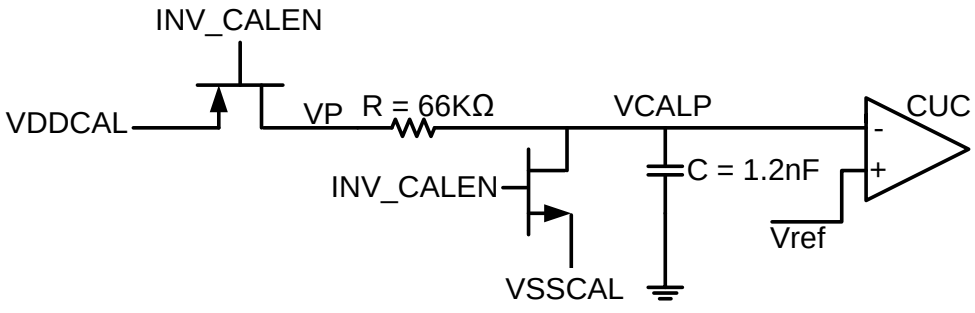

Figure 7. Proposed calibration circuit.

The saturation levels in the proposed circuit can be set externally by using external pins. The lower limit is determined by the full scale of the converter, and the upper limit is determined by the technology voltage limits. The exponential signal is defined by Equation (2). In this study, for the sake of simplicity, we consider that the calibration capacitor is charged and discharged between the ground and the supply voltage V_{DD}.

$$V_C = V_{DD} \times (1 - e^{-t/\tau}) \tag{2}$$

where τ is the time constant of the exponential signal and is equal to $(R \times C)$. The value of τ determines the maximum slope of the exponential signal, and thus, the calibration speed. A fast calibration is desirable, but there is a trade-off between calibration resolution and speed.

4.2. Impact of Stimulus Non-Linearity

The choice of the non-linear stimulus also imposes some approximations when used to rank the best comparators. The voltage of the non-inverting node of the CUC is equal to the capacitor voltage (V_C) in Figure 7, as given by (2).

Let us denote T_{id} as the ideal time at which the comparator output should toggle when $V_C = V_{id}$ in (2). With a real comparator with an offset, the output will flip at T_{re} such that:

$$V_C = V_{DD} \times (1 - e^{-T_{re}/\tau}) = V_{id} + \text{offset} \tag{3}$$

After some calculation, we can express the flip-time difference as a function of the offset:

$$\Delta T = T_{re} - T_{id} = -\tau \ln\left(1 - \frac{\text{offset}}{V_{DD} - V_{id}}\right) \tag{4}$$

The calibration algorithm compares the absolute value of the flip time deviation (ΔT_i) of the comparator under calibration with the flip-time deviation of the best (and second-best) comparator (ΔT_b). This is an approximation, because (4) is not an odd function. To determine its validity range, the error committed by considering the absolute crossing times is calculated as follows. Suppose that we read a flip time value equal to the best candidate:

$$|\Delta T_i| = |\Delta T_b| \tag{5}$$

If $\Delta T_i = \Delta T_b$, no error is committed, and we have $\text{offset}_i = \text{offset}_b$. However, if $\Delta T_i = -\Delta T_b$, using (4), we obtain

$$\frac{1}{\left(1 - \frac{\text{offset}_i}{V_{DD} - V_{id}}\right)} = 1 - \frac{\text{offset}_b}{V_{DD} - V_{id}} \tag{6}$$

Let us call δ_o the error committed on the offset

$$\text{offset}_i = -\text{offset}_b + \delta_o \tag{7}$$

Equation (6) reduces to

$$\delta_o = \frac{-\text{offset}_b{}^2}{V_{DD} - V_{id} - \text{offset}_b} \tag{8}$$

We plot the error δ_o versus the best comparator offset for different levels $(V_{DD} - V_{id})$ across the input range. The results are shown in Figure 8. It can be observed that the error is very small near the ideal level (small offset_b), as expected for a continuous function with a small second derivative. In fact, the redundancy system has been sized to maximize the yield; therefore, there is a very high probability of finding more than one comparator within the range $([-0.5, 0.5]$ LSB). The errors for comparators located farther away can be

neglected because they will not be selected. Consequently, we can estimate the worst-case error as

$$\delta_{max} = \frac{(0.5\text{LSB})^2}{\text{V}_{\text{DD}} - \text{V}_{\text{FS}^+} - 0.5\text{LSB}} \tag{9}$$

where V_{FS^+} is the top of the full-scale range.

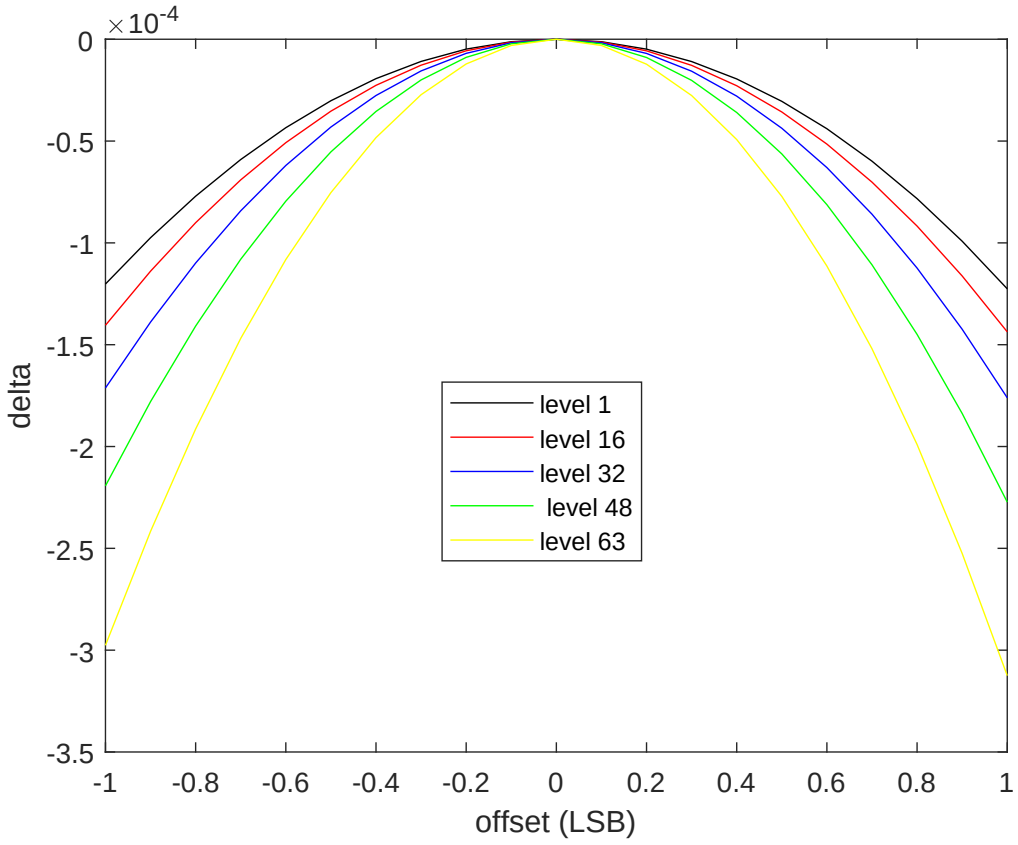

Figure 8. Time offset error due to measuring the absolute crossing time difference.

In our case study, the FLASH ADC is not designed to work in rail-to-rail, so we have that $(\text{V}_{\text{DD}} - \text{V}_{\text{FS}^+}) >> 0.5$ LSB. The full-scale range was designed to be approximately one-half of the rail-to-rail range, so the minimum value of $(\text{V}_{\text{DD}} - \text{V}_{\text{FS}^+})$ is approximately $2^{(N-2)} = 16$ LSB (for $\text{N} = 6$). The worst-case comparison error ($\delta_{max} \cong 0.016$ LSB) was negligible.

4.3. Error Sensitivity to the Design Parameters

From Equation (2), the calibration stimulus is defined by three parameters: the supply voltage itself, the instant at which charging begins, and the time constant τ of the exponential. A drift in any of these values will unduly alter the comparator flip time and thus cause an error. To calculate this error, we first consider that an ideal comparator (with zero offset) will trigger its output when its input (V_C) is equal to the reference voltage associated with the ideal voltage (V_{id}) of the level under calibration.

$$\text{V}_{\text{DD}} \times (1 - e^{-T_{id}/\tau}) = \text{V}_{\text{id}} \tag{10}$$

So, the ideal flip time T_{id} can be written.

$$T_{id} = -\tau \ln\left(1 - \frac{\text{V}_{\text{id}}}{\text{V}_{\text{DD}}}\right) \tag{11}$$

Now, let us consider that the real calibration stimulus is

$$V^*(t) = V^*_{DD}\left(1 - e^{\frac{-(t-\delta)}{\tau^*}}\right) \tag{12}$$

Here, all parameters are real: we consider a non-nominal supply voltage V^*_{DD}, delay δ in the signal that controls the charging of the calibration capacitor, and effective time constant τ^*.

The calibration algorithm selects the comparators that are closest to the ideal flip times that have been stored; thus, the comparator transition voltages can be explicitly computed as

$$V^*(T_{id}) = V^*_{DD}\left(1 - e^{\frac{\delta}{\tau^*}}\left(1 - \frac{V_{id}}{V_{DD}}\right)^{\frac{\tau}{\tau^*}}\right) \tag{13}$$

For an error in the supply voltage, assuming that $\delta = 0$ and $\tau = \tau^*$, we obtain

$$V^*(T_{id}) = V_{id}\frac{V^*_{DD}}{V_{DD}} \tag{14}$$

This is a gain error that can be neglected. Thus, the specification of the stability of the supply voltage is the same as that of the full-scale range of the converter.

For an error in the charging instant, assuming that $V^*_{DD} = V_{DD}$ and $\tau = \tau^*$, we obtain

$$V^*(T_{id}) = V_{id}e^{\frac{\delta}{\tau}} + V_{DD}\left(1 - e^{\frac{\delta}{\tau}}\right) \tag{15}$$

In this case, an offset term is associated with the gain error. Neither affects the linearity of the converter. Again, we can deduce the constraint on the precision of the charging instant from the offset and full-scale stability requirements.

For an error in the time constant, the situation becomes more complicated. Assuming that $\delta = 0$ and $V^*_{DD} = V_{DD}$, we obtain

$$V^*(T_{id}) = V_{DD}\left(1 - \left(1 - \frac{V_{id}}{V_{dd}}\right)^{\frac{\tau}{\tau^*}}\right) \tag{16}$$

This error introduces non-linearity. However, to retrieve an expression of the INL, we first perform a least-squares regression to obtain the effective offset and gain, and then derive the error expression to find the extreme of the function and identify the maximum INL. This is complicated to perform analytically. Instead, we can use mathematical software to compute the INL as the residue of the best linear fit of (16). Figure 9 shows the maximum INL as a function of the time constant drift, considering that the full-scale is set to be $[25\%;\ 75\%] \times V_{DD}$, and that the ADC resolution is six bits.

Under these circumstances, the INL remains below 0.5 LSB for deviations of the time constant within $[-7.3;\ 8.8]\%$, which is quite easy to guarantee with external *RC* components. As we will see later, this margin also accounts for the contribution of the input capacitance of the ADC, which should be orders of magnitude smaller than the external calibration capacitor.

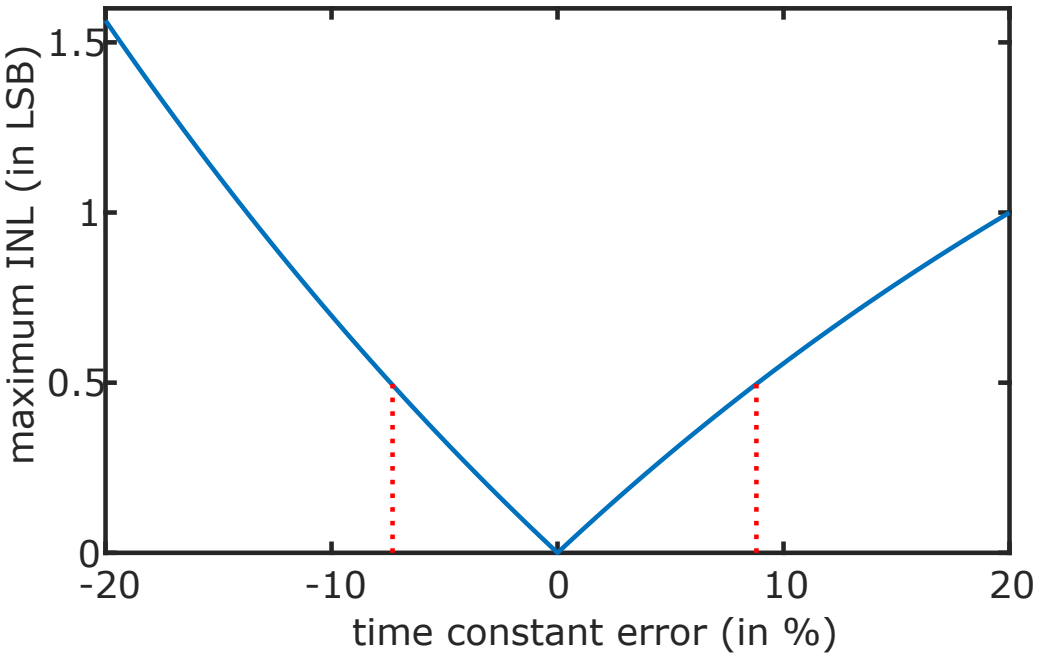

Figure 9. Maximum INL as a function of the time constant error.

4.4. Parameter Sizing

The system requirements set constraints on the design parameters of the calibration stimulus. The discrete step between consecutive samples was used to express the lower limit of the required calibration. For a linear signal, the voltage step between two consecutive samples is constant and is determined by the slope of the ramp signal. For an exponential stimulus defined by (2), we can simply consider the maximum slope to obtain the largest voltage step, which gives us the worst-case offset resolution to determine the best candidate and set a minimum value for the exponential time constant.

$$\frac{dV_C}{dt} = \frac{1}{\tau} \times V_{DD} \times (e^{-t/\tau}) \tag{17}$$

The lowest starting time for comparator calibration corresponds to the minimum of the full-scale (V_{FS-})

$$t_{FS-} = -\tau \times \ln(1 - \frac{V_{FS-}}{V_{DD}}) \tag{18}$$

Combining (17) and (18), the maximum voltage step at this time is reduced to

$$\Delta V_{max} = \frac{T_S}{\tau} \times V_{DD} \times (1 - \frac{V_{FS-}}{V_{DD}}) \tag{19}$$

If we express V_{max}, the desired resolution of the offset measurement, as a fraction α of an LSB, we can calculate the minimum time constant τ_{min} that is required to meet this target as follows

$$\tau_{min} = T_S \times \frac{2^N V_{DD}}{\alpha \times (V_{FS+} - V_{FS-})} \times (1 - \frac{V_{FS-}}{V_{DD}}) \tag{20}$$

where T_s is the period of the ADC sampling clock.

In this design, $V_{FS+} - V_{FS-} \approx \frac{V_{DD}}{2}$ and $V_{FS-} \approx \frac{V_{DD}}{4}$. If the worst offset resolution is set to $\alpha = 0.1$, it means that the minimum time constant should be approximately three orders of magnitude greater than the sampling period. For a converter operating at 200 MS/s, this corresponds to the minimum time constant of 5 µs.

Separate values of R and C must be determined. The resistance must be sufficiently large to neglect the resistance effect of the switch on the resulting τ. At the same time, the capacitance must be sufficiently large to neglect the input capacitance of the comparator circuit and the parasitic associated with the input multiplexer array. A simple simulation test bench is used to estimate the resistance of the calibration switch. This test bench consisted of a typical RC circuit generator, including a calibration switch. By charging the calibration capacitance from V_{SS} to V_{DD}, we measure the resistance of the switch across the entire range. The maximum resulting resistance in our design is 102 Ω.

To estimate the capacitive parasitic, we simply ran an AC analysis feeding the comparator array with a sine source and a known resistor. The resulting cutoff frequency is 3.5 MHz and hence the input capacitance of the comparator bank is 1.88 pF. After determining the parasitic resistance and capacitance of the converter, the resistance and capacitance values of the calibration stimulus were determined. Starting from the real-time constant equation, which is given by (21)

$$(\tau + \Delta\tau) = (R + \Delta R) \times (C + \Delta C) \tag{21}$$

where $\Delta\tau$ is the deviation in the time-constant owing to the parasitic resistance and capacitance, ΔR is the parasitic resistance (102 Ω), and ΔC is the parasitic capacitance (1.88 nF). By neglecting the term $\Delta R \times \Delta C$ because of its small value with respect to the rest of the terms, it can be deduced that

$$\Delta\tau = (R \times \Delta C) + (C \times \Delta R) \tag{22}$$

Replacing the capacitance term with its equivalent $C = \tau/R$, and considering that ΔR and ΔC are the switch resistance and parasitic capacitance, respectively, we can find the resistor value that minimizes (22) as

$$R = \sqrt{\frac{(\Delta R \times \tau)}{\Delta C}} \tag{23}$$

The objective time constant is set in this work to be 80 µs, so the resulting R is equal to 66 KΩ and the calibration capacitance is 1.2 nF.

5. Simulations Results

To verify this idea, we designed a six-bit flash ADC based on the proposed system. The design provides eight redundancy comparators for each level. In addition, 16 adjacent levels are considered to identify comparator candidates who benefit from high comparator offsets. The system is implemented using UMC180nm CMOS technology and consists of two main parts: the converter part and the calibration stimulus part. The verification of the system performance implies studying the effect of circuit modification and the corresponding deviation of its performance due to parallel processing. In this section, we also present a validation test for the idea of using the RC response as a calibration signal and time-offset measurement instead of a voltage-offset measurement. A Monte-Carlo simulation is performed to ensure that under mismatch and process variations the calibration method keeps working.

5.1. Front-End Circuit Verification

Switches are used to switch on/off and connect/disconnect the comparators for one of the two modes of operation. These were used to charge/discharge the calibration stimulus. The effects of the extra parasites induced by these switches were verified.

5.1.1. Switches Effect on the Conversion Operation

The ideal performance of the core converter was obtained from the reference circuit, which consisted of core comparators without redundancy. The comparator circuit is the original dynamic latch circuit without switches and has only one operation mode,

which is the converting mode. Note that this is a best-case scenario because we do not include a mismatch in the simulation; therefore, the effect of the comparator's offsets is not considered.

In contrast, the proposed circuit consists of all comparators (active and inactive) with the comparator circuit shown in Figure 2. This test studies not only the effect of the additional input resistance, but also the loading effect of the switched-off comparator bank.

In both circuits, the encoder that converts the thermometer code into binary code is an ideal circuit. The converter supply voltage was 1.8 V, the common-mode voltage was 0.9 V, and its full scale was 0.8 V. The input analog signal amplitude was 75% of the full scale of the converter. The simulation was run for two input signal frequencies: low input frequency (9 MHz) and near Nyquist frequency (90 MHz). A register of 4000 samples of the reconstructed analog signal was used to generate the spectrum, which was analyzed using MATLAB to determine the converter's effective number of bits (ENOB) and signal-to-noise ratio (SNR). The first circuit was considered as the reference circuit for the conversion mode in this study.

For the 9 MHz input frequency, the resultant ENOB is 5.9 bits and the SNR is 35.7 dB for the reference circuit, while the proposed circuit gives an almost identical result of = 5.9 bits for ENOB and 35.3 dB for SNR. The resulting spectra are shown in Figure 10.

For the 90 MHz input frequency, the resultant ENOB is 5.8 bits and the SNR is 34.8 dB for the reference circuit. The proposed circuit provides the same performance = 5.8 bits for ENOB and 34.8 dB for SNR. The resulting spectra are shown in Figure 11.

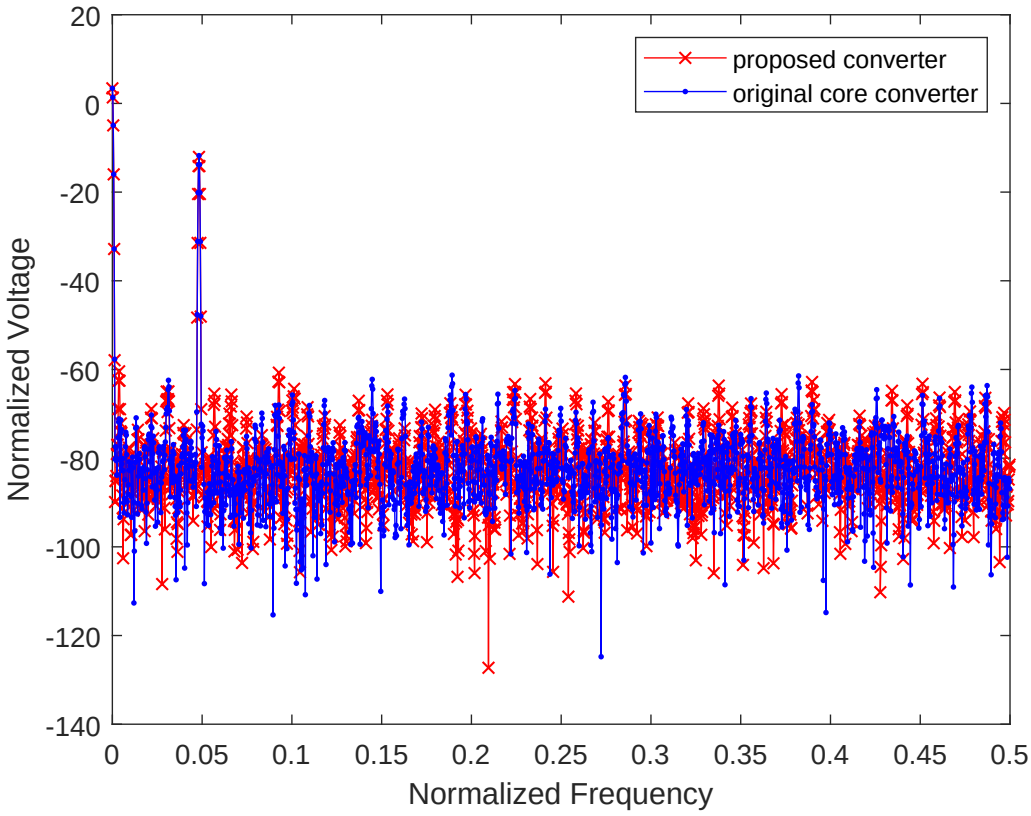

Figure 10. Spectrum of the output signal at low-frequency input signal.

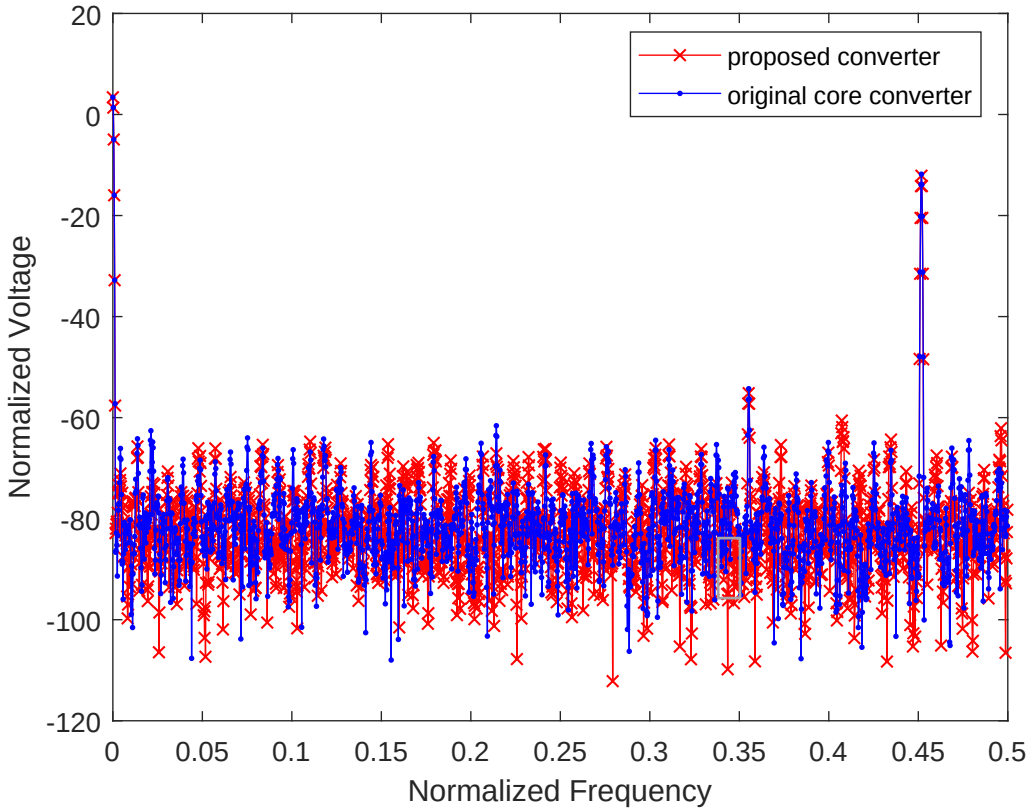

Figure 11. Spectrum of the output signal at high-frequency input signal.

5.1.2. Switches Effect on the Calibration Stimulus and Calibration Results

As mentioned above, the calibration stimulus was generated by charging and discharging the *RC* circuit using switches. The objective of this test is to ensure that adding switches to the calibration stimulus generator does not significantly affect the calibration results. In other words, the resistance and capacitance of the switches are negligible compared to those of the *RC* generator. In addition, we tested the loading effect of the complete array on the calibration stimulus and output.

We compared an ideal generator and the proposed generator. The ideal generator consists of an *RC* circuit connected directly to the calibration supply voltage and loaded by a single comparator. The comparator reference is fed directly from an ideal voltage source. On the other hand, the proposed generator includes the switches between the calibration supply and the *RC* circuit. The load is a full comparator array, and the comparator reference is generated using the resistive ladder. The comparator circuit consists of the proposed comparator with its input multiplexer.

The comparison is run at both converter extremes to ensure that the difference over the converter range is small. The calibration supply is set to 1.8 V and the differential lowermost reference voltage of the loading comparator is 0.787 V. The simulation results are shown in Figure 12. Figure 13 shows the trigger point, and we find that the output of the comparator circuit is triggered after 27.43 µs in the proposed circuit and 27.47 µs in the reference circuit. Therefore, the resulting difference between the comparator output trigger points is approximately 40 ns. This implies an error in the offset measurement of 0.0797 LSB, which can be neglected.

The same test was repeated at the uppermost reference limit to determine the range of error over the converter full-scale. The output of the comparator circuit was triggered after 91.06 µs in the proposed circuit and 91.15 µs in the reference circuit. Therefore, the resulting difference between the comparator output trigger points is approximately 95 ns.

The error in time is larger, but because the derivative of the calibration stimulus is smaller, the voltage error remains less than 0.5 LSB.

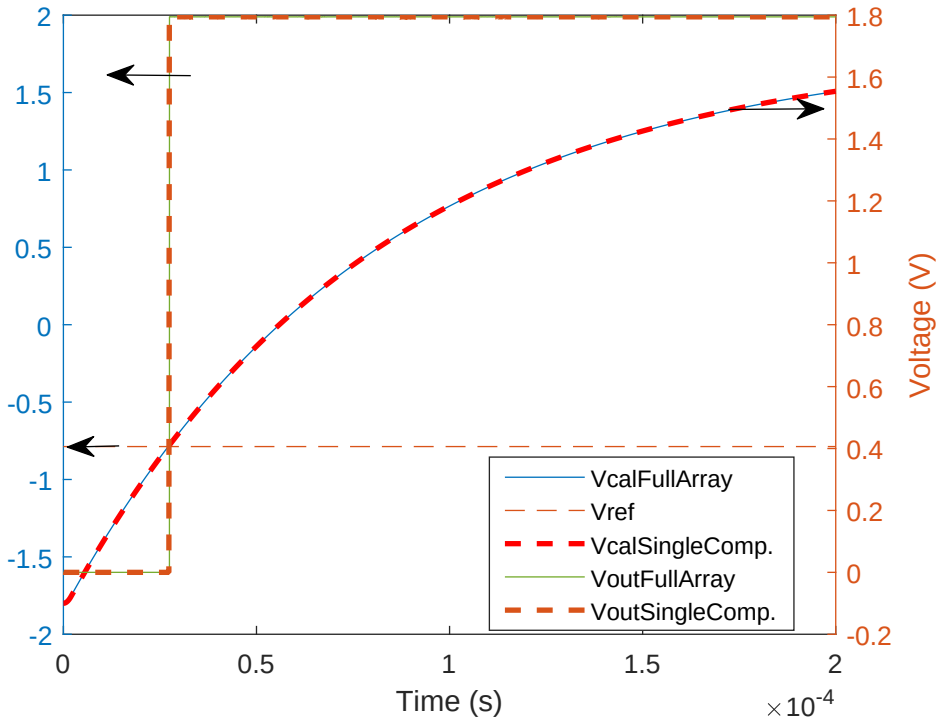

Figure 12. Simulation result for the effects of adding switches in the calibration generator circuit and comparator array loading on calibration stimulus and calibration output.

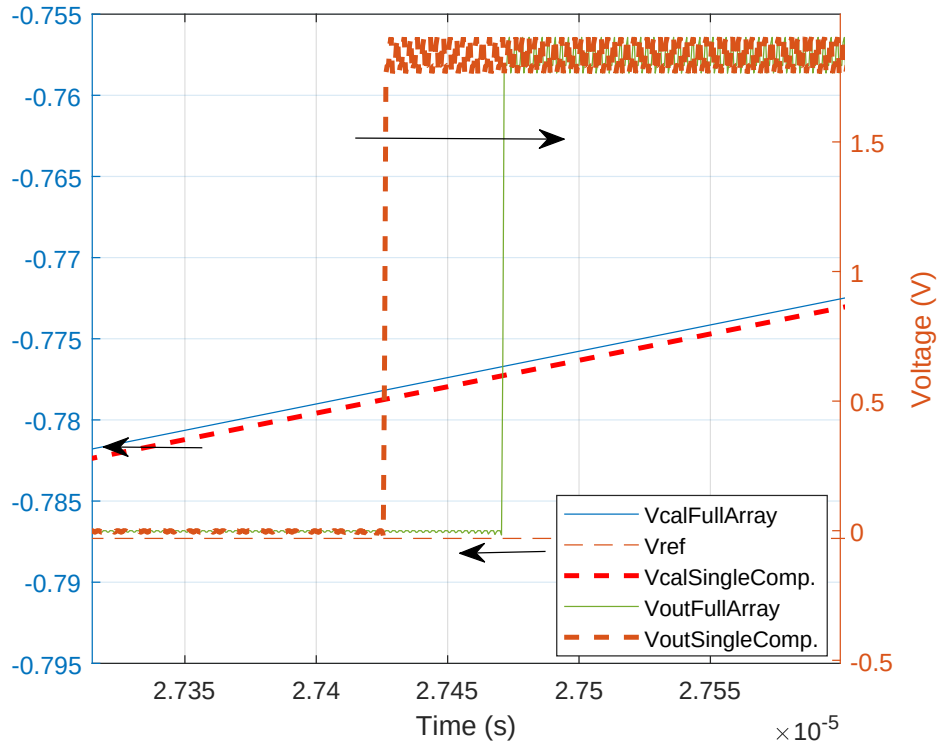

Figure 13. Simulation result for the effects of adding switches in the calibration generator circuit and comparator array loading on calibration stimulus and calibration output focusing at the output toggle moment.

5.2. Calibration and Conversion Cross-Talking

Online calibration imposes a concurrent operation of the A/D conversion and calibration processes. This subsection studies the performance impact of one process on the other: the deviation in the converter precision due to online calibration and the deviation in the calibration output result due to conversion operation.

The test bench consisted of a calibration stimulus generator and a complete comparator bank connected to a resistive ladder. The calibration process is enabled by an ideal pulse on the selected comparator under calibration (to E_{CAL}), instead of using the decoder, to reduce the simulation time. For the same reason, the comparators selected for the conversion process are enabled by an ideal DC voltage source at the supply voltage (to E_{ADC}), without using the comparator enable memory. The remaining comparators were switched off by connecting their E_{CAL} and E_{ADC} to the ground.

A full-scale input sine wave at 9 MHz was presented at the normal input of the array, and the calibration stimulus was the one described above, with a time constant of 80 µs.

The conversion performance without concurrent calibration operations was previously analyzed. For the concurrent operation, we considered three different windows of 4000 samples to perform the FFT: before and after the flipping of the comparator under calibration, and the window in between, for which the comparator flipping instant is in the center. Table 3 summarizes the results, and the spectra are shown in Figure 14. The calibration process only minimally affects the performance of the converter by increasing the noise floor, which is probably associated with the comparator under calibration switching kicking back into the input signal through the multiplexers.

Table 3. Converter performance before, during, and after calibration process.

Case	ENOB (Bits)	SNR
Reference circuit	5.915	35.709
Before calibration	5.831	34.835
During calibration	5.827	34.824
After calibration	5.827	34.828

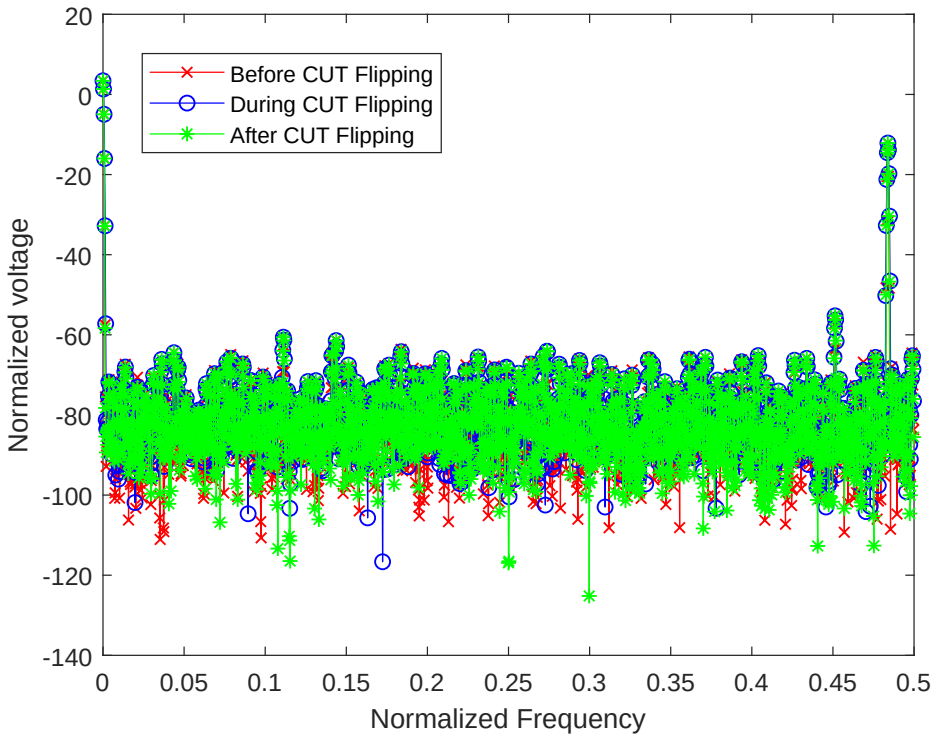

Figure 14. Converter output spectrum before/during/after CUT flipping.

Now, we examine the effect of running the conversion process on the calibration results. The test bench consisted of two identical systems (reference ladder, comparator bank, ideal encoder, and calibration stimulus generator). To reduce the simulation netlist, the E_{ADC} and E_{CAL} signals were generated from ideal voltage sources. The first system had only one active comparator connected for calibration, and the rest of the comparators in the bank are inactive. In the other system, there were 63 comparators active for conversion and one comparator active for calibration. Note that the ID of the CUC was the same in both systems. The calibration stimuli in both systems, as well as both outputs of the CUCs, were compared. The test was run at the upper reference extreme and there was a small deviation between the exponential signals; however, its maximum value was 1.9 mV. This deviation is due to the kickback effect of the open switches in conversion comparators. This affected the trigger point. This deviation acts on the conversion system as a DC gain error, but its value is less than 0.1 LSB. By repeating the same simulation at the other extreme of the converter, the results in Figure 15 were obtained.

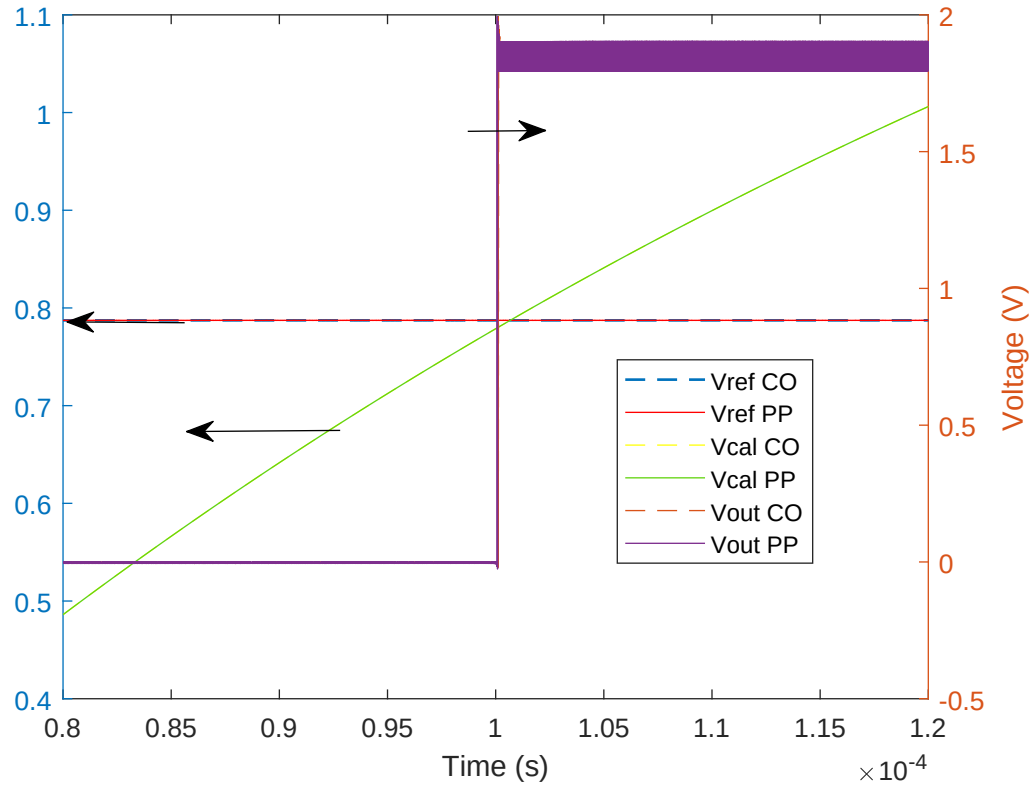

Figure 15. Conversion effect on calibration results.

5.3. Monte-Carlo Simulations Results

The objective of this simulation is to demonstrate that the calibration stimulus (exponential signal) is robust (maintains its curve) against the process variation and mismatch and the error of the calibration results is below the 0.2 LSB.

The test bench consists of the converter circuit including the bank of comparators and the calibration stimulus circuit. The calibration of one comparator is conducted and the rest of the comparators are switched off to reduce the simulation time. The time constant of the exponential was set much slower than necessary with respect to the sampling frequency of the ADC. This was conducted to minimize the impact of the input capacitance and resistance of the multiplexer. While this is not an issue from a practical realization viewpoint, it is very cumbersome to perform transient simulations, since each clock edge forces many time steps. Hence, we reduced the clock signal frequency to accelerate the simulation but maintained the duration of the pulse to 2.5 ns to keep the same requirement for the comparator decision as for a 200 MHz sampling clock. The minimum permitted

clock frequency for certain exponential calibration signals can be determined by the error budget: the maximum voltage step between two consecutive points. In our design, the desired detection sensitivity is 0.1 LSB. So, the voltage step between two consecutive points can be expressed as follows:

$$\text{step} = \text{V}_{\text{DD}} \times (1 - e^{-1/F_{smin}\tau}) \tag{24}$$

where the step is the difference between two consecutive points over the exponential calibration signal and is equal to 0.1 LSB and F_{smin} is the minimum acceptable frequency of the clock signal.

So, one can obtain the F_{smin} expression as

$$F_{smin} = \frac{-1}{\tau \times \ln(1 - \frac{step}{\text{V}_{\text{DD}}})} \tag{25}$$

In our design, τ = 79.2 µs, step = 0.1 LSB, and V_{DD} = 1.8 V which gives F_{smin} = 9.1 MHz. Based on this result, the clock frequency was set to 10 MHz (with a pulse duration of 2.5 ns), and a Monte-Carlo simulation of both the process and mismatch parameters was run to measure the flip voltage and time. The resulting vectors are used to reconstruct the best fit exponential and determine the error between the best fit exponential and the crossing points. The maximum error value is less than 0.04 LSB, as can be seen in Figure 16.

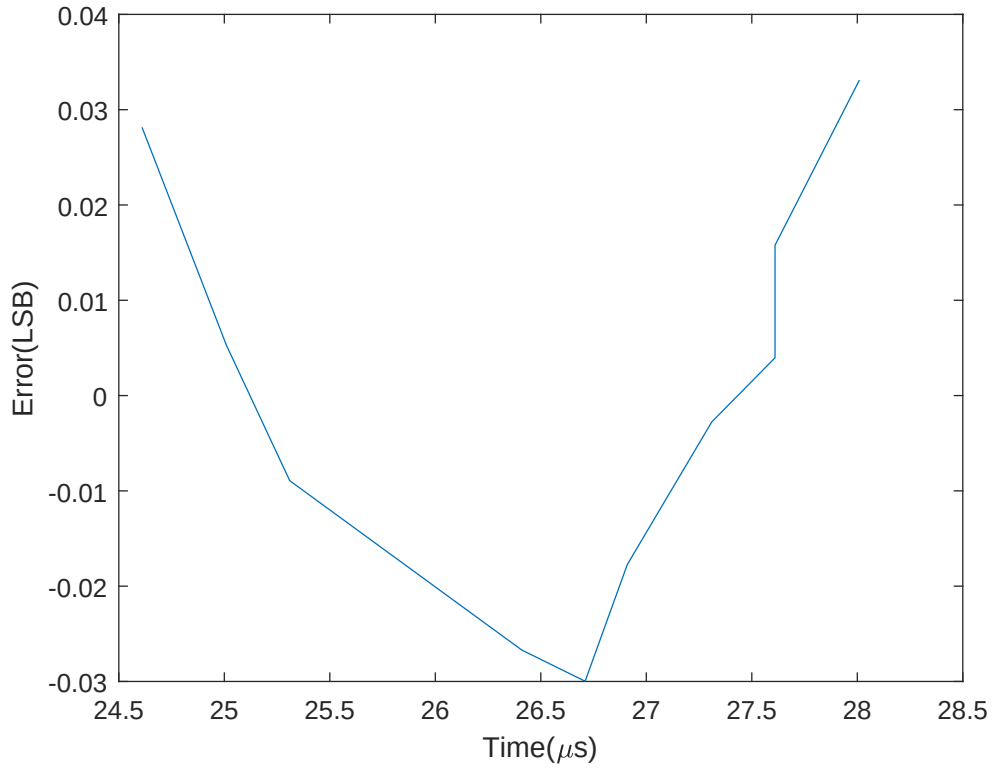

Figure 16. Error in calibration signal results due to mismatch and process variation as a function of LSB.

6. Conclusions

The efficiency of flash converters is primarily determined by the precision of their comparators. This precision can deteriorate (even drastically) with time or environmental variation. A redundancy-based flash converter is an available architecture that provides an unusual solution. It has a bank of substitute candidates that can heal the system by introducing an online calibration algorithm to determine the best candidates for the

converter operation. The calibration algorithm is run periodically to improve the converter performance without external intervention. To provide robust and efficient calibration, we propose the use of an exponential stimulus determined by off-chip components. The control unit in this study was implemented on an FPGA. This article discusses the proposed idea, defines the required hardware, and develops design equations to properly size the calibration system. In addition, we present the simulation results of the effect of the modifications on the original redundancy system and cross-talk effect. These results show that the modifications do not affect the converter performance and that the parallel operations are successful.

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