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A Q-Band CMOS Image-Rejection Receiver Integrated with LO and Frequency Dividers

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Abstract: This paper presents a Q-band image-rejection receiver using a 65 nm CMOS technology. For a high image-rejection ratio (IMRR), the Q-band receiver employs the Hartley architecture which consists of a Q-band low-noise amplifier, two down-conversion mixers, a 90° hybrid coupler, and two IF baluns. In addition, a Q-band fundamental voltage-controlled oscillator (VCO) and a frequency divider chain divided by 256 are integrated into the receiver for LO. A charge injection technique is employed in the mixers to reduce the DC power while maintaining a high conversion gain and linearity. The VCO adopts a cross-coupled topology to secure stable oscillation with high output power in the Q-band. The frequency divider chain is composed of an injection-locked frequency divider (ILFD) and a multi-stage current-mode logic (CML) divider to achieve a high division ratio of 256, which facilitates the LO signal locking to an external phase-locked loop. An inductive peaking is employed in the ILFD to widen the locking range. The Q-band image-rejection receiver exhibits a peak conversion gain of 16.4 dB at 43 GHz. The IMRR is no less than 35.6 dBc at the IF frequencies from 1.5 to 5 GHz.

Keywords: CMOS; Q-band receiver; image rejection; low-noise amplifier; down-conversion mixer; voltage-controlled oscillator; frequency divider

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1. Introduction

The development of mobile devices and the need for high-speed communication have resulted in considerable research on receivers operating in the mm-wave frequency bands [1–17]. In [2–4], the beamforming receivers were implemented by combining four channels [2,3] and eight channels [4], respectively. In [5,6], direct-conversion receivers were presented for low power consumption and small chip area. Although the direct conversion was free from the image problem, the architecture suffered from high DC offset, even-order distortion, and flicker noise [18]. In [13], a high image-rejection ratio (IMRR) over a wide bandwidth was obtained using a single-sideband receiver structure with a high IF. However, such a high IF frequency would require additional down-conversion to the baseband, and the first down-conversion mixer may suffer from compression or self-mixing due to the LO frequency interference. In [14,15], a high IMRR was achieved in the low-IF band by using a Hartley-structured receiver with a quadrature generator that minimized the I-Q mismatch. However, these studies did not include an LO circuit integrated in the receiver, so additional VCO and frequency dividers were required for phase-locked LO generation.

This paper presents a Q-band image-rejection receiver employing the Hartley architecture for a high IMRR [19]. Furthermore, the receiver integrates an on-chip voltage-controlled oscillator (VCO) and frequency divider chain for LO generation. The divider chain is composed of an injection-locked frequency divider (ILFD) and a seven-stage current-mode logic (CML) divider, which fulfill a high division ratio of 256. This facilitates the LO locking to an external phase-locked loop (PLL). This Q-band image-rejection receiver

was implemented using a 65 nm bulk CMOS technology, which is relatively cost-effective and easily accessible. The remainder of the paper is organized as follows. In Section 2, the architecture of the Q-band image-rejection receiver is described. The design and measurement of each circuit block of the receiver is presented in Section 3. Section 4 presents the measurement of the Q-band image-rejection receiver. Finally, the conclusions are presented in Section 5.

2. Q-Band Image-Rejection Receiver Architecture

Figure 1 shows the block diagram of the Q-band image-rejection receiver. The image-rejection receiver is composed of a Q-band low-noise amplifier (LNA), two down-conversion mixers, a 90° hybrid coupler, two IF baluns, a Q-band VCO, and a frequency divider chain. The receiver adopts the Hartley image-rejection architecture for a high IMRR. The RF input is amplified and divided with a phase difference of 180 degrees through the single-to-differential Q-band LNA and applied to the two Q-band down mixers. The LO signal generated by the Q-band VCO is divided with a phase difference of 90° through the 90° hybrid coupler and drives two down-conversion mixers, respectively. The differential IF outputs generated by each mixer are added in-phase at the output of the IF balun, and combined through the off-chip IF 90° hybrid coupler. The desired IF signal down-converted through the two down-conversion mixers is added in-phase, and the image signal is canceled out by out-of-phase.

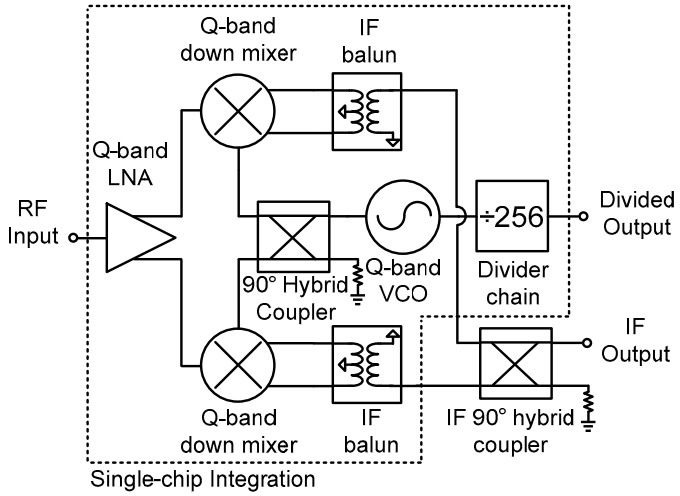


Figure 1. Block diagram of the Q-band image-rejection receiver.

The Q-band VCO operates in the fundamental mode to suppress the spurious spectral components compared to the harmonic-mode VCOs. The following frequency divider chain provides a low-frequency LO signal divided by 256. Thus, the LO signal can be readily locked to an off-chip PLL circuitry.

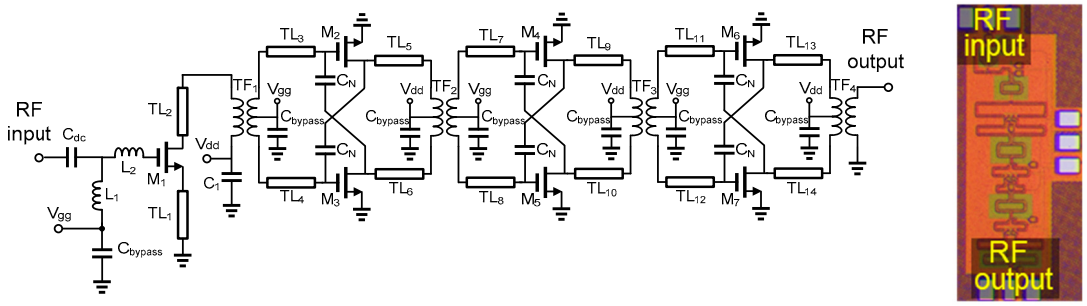
3. Circuit Blocks of the Q-Band Image-Rejection Receiver

In this section, the design details and measurement results of each individual circuit block of the Q-band image-rejection receiver are described.

3.1. Q-Band LNA

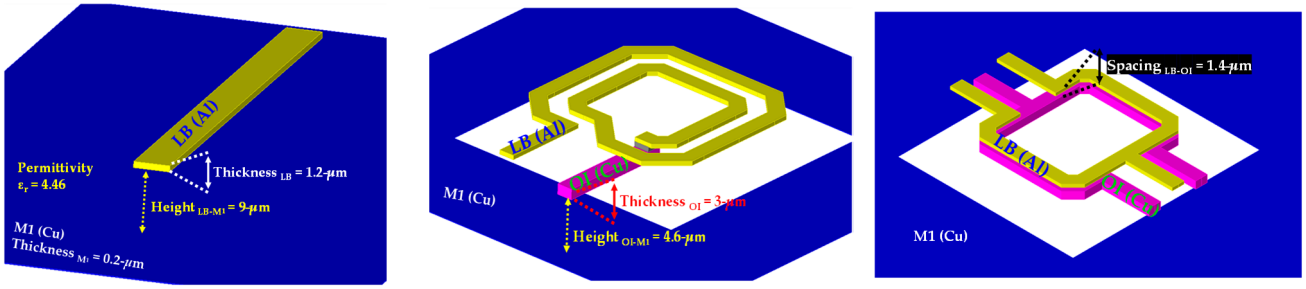
A schematic of the Q-band LNA is depicted in Figure 2a. The first stage of the LNA employs a single-ended structure to eliminate the noise figure (NF) component which would be otherwise contributed by an input balun. The NF is further improved by the source degeneration of a transmission line (TL_1). The input is matched to the optimum NF point through L-section matching, which is composed of parallel and series inductors (L_1 and L_2). All transmission lines are designed in a microstrip structure using the top

metal with a 1.2 µm thickness to minimize the loss and chip area, as shown in Figure 3a. The layout of the inductor and transformer are shown in Figure 3b,c, respectively. The inductors were designed in an octagonal shape using the top metal and the inductance was extracted through EM simulation. The transformers were designed using a broadside coupling structure composed of the top two metals (LB and OI).



(**a**) (**b**)

Figure 2. (**a**) Schematic diagram and (**b**) chip micrograph of the Q-band LNA.



(**a**) (**b**) (**c**)

Figure 3. Layout of the (**a**) transmission line, (**b**) inductor, and (**c**) transformer.

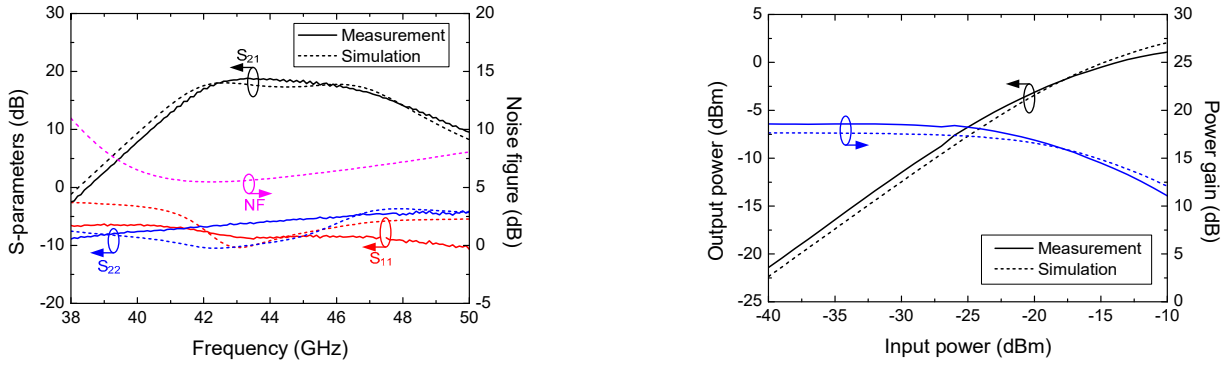
The second to last stages were designed using a differential common-source structure with the capacitive neutralization technique to improve gain and stability. The interstage matching between the first and second stages was implemented using transmission lines (TL_2–TL_4) and a transformer-based balun (TF_1) connected to a balancing capacitor (C_1). The other interstage and output matching networks are also composed of transmission lines and transformers to reduce the chip area. The output impedance is conjugately matched to the RF input of the following Q-band down-conversion mixer. A chip micrograph of the Q-band LNA is shown in Figure 2b. The chip area is 1.7 × 0.6 mm^2, which includes the probing pads. The differential output is combined into a single-ended signal using a balun (TF_4) for single-ended measurement purposes. The LNA chip consumes DC power of 30 mW at the drain bias voltage of 1.2 V. The parameter value of each component is presented in Table 1.

Table 1. Parameter values of the Q-band LNA.

Parameter	Value	Parameter	Value
M_1–M_7	1 × 10 µm	C_{dc}, C_{bypass}	880 fF
L_1	380 pH	C_1	160 fF
L_2	460 pH	C_N	8.8 fF

The measurement results for the Q-band LNA are shown in Figure 4. The measurement was performed by an on-chip probing method. Figure 4a shows the S-parameters and

NF. A peak gain of 18.8 dB was measured at 43.3 GHz with a 3 dB bandwidth of 5.6 GHz (41.7–47.3 GHz). The input matching was measured below 7.2 dB over the entire 3 dB bandwidth while the simulated NF was below 6.9 dB. Figure 4b presents the power measurement of the LNA at 43.5 GHz. The measured input and output 1 dB compression power (IP_{1dB} and OP_{1dB}) were −22 dBm and −4.5 dBm, respectively.

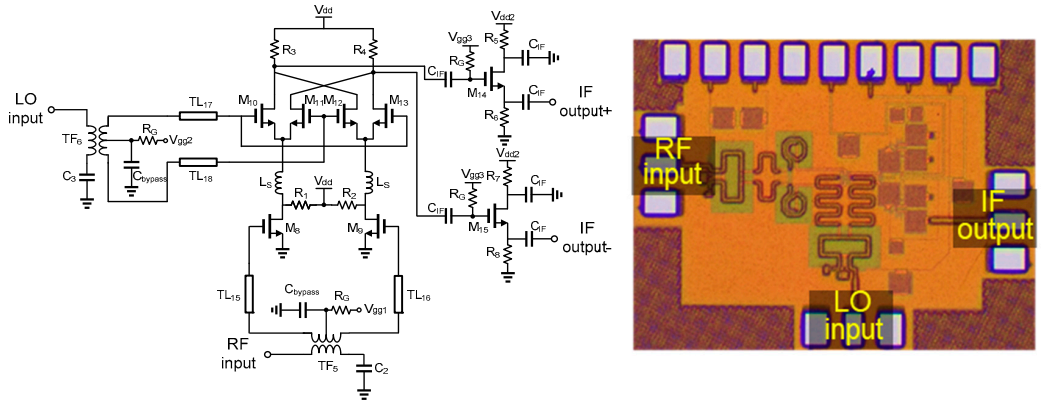


(**a**) (**b**)

Figure 4. Measurement results of the Q-band LNA: (**a**) S-parameters and NF; (**b**) output power and power gain versus input power at 33.5 GHz.

3.2. Q-Band Down-Conversion Mixer

The Q-band down-conversion mixer was designed using a Gilbert-cell topology for a high conversion gain and isolation performance [20,21]. A schematic of the mixer is shown in Figure 5a. The charge injection through R_1 and R_2 is adopted at the transconductance stages to reduce DC power consumption while maintaining a high conversion gain. The RF and LO matching networks are composed of transformer-based baluns (TF_5 and TF_6) and series transmission lines (TL_{15}–TL_{18}) for broadband impedance matching and chip area reduction. Series inductors (L_S) are inserted between the transconductance and switching-quad stages to extend the RF bandwidth. A source-follower buffer was added at the output to improve the isolation and IF matching performance. The transistor sizes of the transconductance, switching-quad, and source-follower stages were 2 × 20 µm (M_8 and M_9), 2 × 12 µm (M_{10}–M_{13}), and 2 × 30 µm (M_{14} and M_{15}), respectively. A chip micrograph of the Q-band down-conversion mixer is shown in Figure 5b, occupying a chip area of 1 × 0.8 mm^2 including the probing pads. For a single-ended testing purpose, one of the differential output is terminated by a 50-ohm resistor. The Q-band down-conversion mixer consumes DC power of 4.57 mW at the mixer core and 3.89 mW at the source-follower buffer. The parameter value of each component is presented in Table 2.



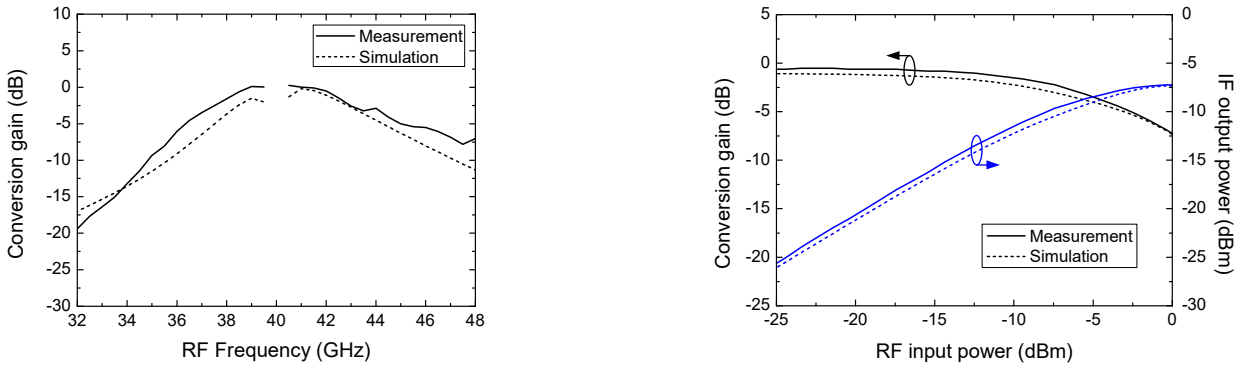
(**a**) (**b**)

Figure 5. (**a**) Schematic diagram and (**b**) chip micrograph of the Q-band down-conversion mixer.

Table 2. Parameter values of the Q-band down-conversion mixer.

Parameter	Value	Parameter	Value	Parameter	Value
M_8, M_9	2 × 20 µm	R_3, R_4	730 Ω	C_3	203 fF
M_{10}–M_{13}	2 × 12 µm	R_5, R_7	68 Ω	C_{bypass}	880 fF
M_{14}, M_{15}	2 × 30 µm	R_6, R_8	92 Ω	C_{IF}	5 pF
R_G	5 kΩ	L_S	240 pH		
R_1, R_2	340 Ω	C_2	139 fF		

Figure 6 presents the measurement result of the Q-band down-conversion mixer. Figure 6a shows the measured conversion gain versus RF frequency with the LO power of 0 dBm applied at 40 GHz. The conversion gain exhibited a peak value of 0.25 dB at 40.5 GHz and the 3 dB bandwidth was 6.8 GHz (37.3–43.3 GHz). The conversion gain and IF output power at 1.0 GHz versus RF input power at 41.0 GHz are plotted in Figure 6b. The IP_{1dB} of the mixer was measured to be −6.5 dBm. Since the OP_{1dB} of the LNA was −4.5 dBm, as given in Section 3.1, the input drive power to the mixer would be −7.5 dBm taking into account a 3 dB difference due to the output balun of the LNA (TF_4 in Figure 2a). Therefore, no gain compression was expected from the mixer.



(**a**) (**b**)

Figure 6. Measurement of the Q-band down-conversion mixer: (**a**) conversion gain versus RF frequency with f_{LO} = 40 GHz and P_{LO} = 0 dBm, and (**b**) conversion gain and IF output power versus RF input power with f_{IF} = 1 GHz, f_{RF} = 41 GHz and P_{LO} = 0 dBm.

3.3. Q-Band Voltage-Controlled Oscillator

Generally, there are three oscillator topologies used in the mm-wave frequency band: ring topology [22,23], Colpitts topology [24], and cross-coupled topology [25]. In this work, the cross-coupled topology was adopted as shown in Figure 7a because it provides a sufficient negative resistance, differential operation, and high output power [25]. The total gate width was set to 1.5 × 12 µm considering the trade-off between DC power consumption and output power. The LC tank was implemented using transmission lines (TL_{19} and TL_{20}) and MOS varactors (C_{var}). The dimensions were optimized to resonate with the input capacitance of the cross-coupled pair and the buffer transistors (M_{18} and M_{19}) at 40 GHz. The C_{var} tuned the capacitance from 51.6 to 146 fF with a Q-factor ranging from 4 to 7.6 at 40 GHz. The oscillation core was followed by two cascaded buffer amplifiers. The first buffer is a source follower that improves isolation and stability. Subsequently, a common-source amplifier (M_{20} and M_{21}) was followed to boost the output power to the level required for pumping the Q-band down-conversion mixer. A chip micrograph of the Q-band VCO is shown in Figure 7b. For a single-ended testing purpose, the differential output was combined using the output balun (TF_7). The Q-band VCO occupied a chip area of 0.7 × 0.8 mm^2 including the probing pads. The DC power consumption levels of the oscillation core and buffer stage were 21.1 mW and 31.7 mW, respectively. The parameter value of each component is presented in Table 3.

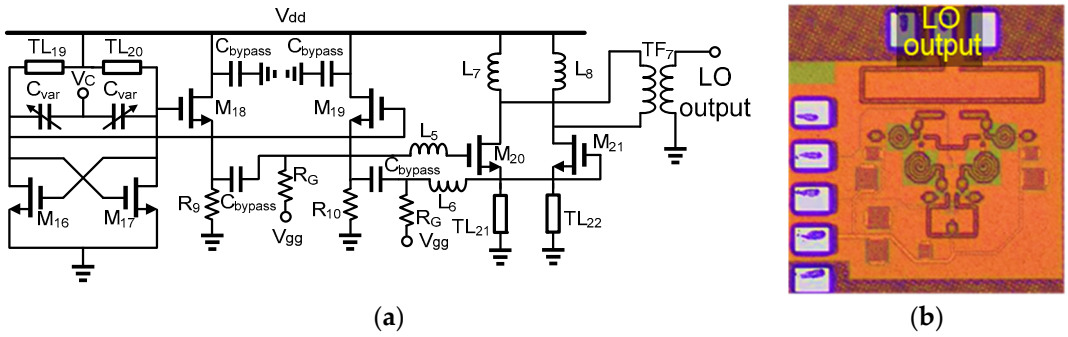


Figure 7. (**a**) Schematic diagram and (**b**) chip micrograph of the Q-band VCO.

Table 3. Parameter values of the Q-band VCO.

Parameter	Value	Parameter	Value
M_{16}, M_{17}	1.5 × 12 µm	L_5, L_6	250 pH
M_{18}, M_{19}	1.5 × 20 µm	L_7, L_8	195 pH
M_{20}, M_{21}	3 × 20 µm	C_{bypass}	880 fF
R_G	5 kΩ	C_{var}	51.6–146 fF
R_9, R_{10}	100 Ω		

In Figure 8, the measured oscillation frequency and output power of the Q-band VCO are compared with the simulation. As the varactor control voltage (V_C) varied from 0 to 2.4 V, the oscillation frequency was tuned from 35.6 to 45.6 GHz (24.6%). The measured output power ranged from −2.7 to 0.6 dBm, including 2 dB of balun loss, which was added only for a measurement purpose.

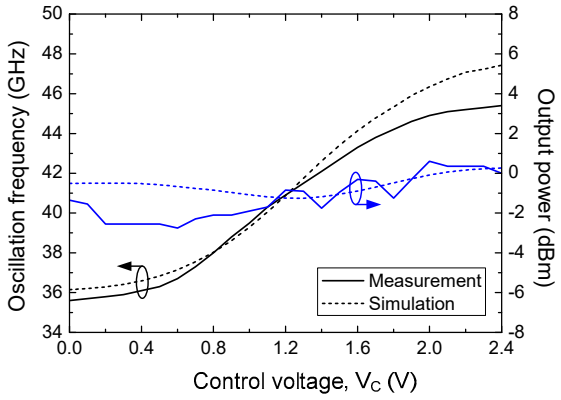


Figure 8. Measured oscillation frequency and output power of the Q-band VCO versus the control voltage.

3.4. Frequency Divider Chain

Three different topologies are widely used for a frequency divider at the mm-wave frequency: the injection-locked frequency divider (ILFD), Miller divider, and current-mode logic (CML) divider. Generally, the ILFD operates at the highest frequency with a low DC power consumption at the expense of a narrow bandwidth. On the other hand, the CML divider cannot support a high-frequency operation and consumes high DC power. However, it occupies the smallest chip area, particularly at relatively low frequencies [26,27]. Therefore, in this work, the frequency divider chain adopted a ILFD for the first frequency division in the Q-band, which was followed by seven CML dividers.

Figure 9 shows a schematic diagram of a basic Q-band ILFD, which consists of a cross-coupled oscillation core (M_{22} and M_{23}), a resonator, an injection network (M_{24}), and a source-follower buffer (M_{25} and M_{26}). The resonator, composed of an inductor (L_{res})

and parasitic capacitances of $M_{22–23}$, M_{24}, and $M_{25–26}$, resonates at f_0, a half frequency of the injection signal (LO_{in}). The LO_{in} is injected directly into the differential oscillation core through M_{24}. This direct injection enables the extension of the locking range (LR) at a higher operating frequency compared to conventional injection through a tail current source [28]. The LR of the direct ILFD can be expressed as [29]

$$LR \propto \frac{2\pi f_0 I_{in}}{Q I_{osc}} \tag{1}$$

where I_{in} and I_{osc} denote the injection current by LO_{in} and oscillation current, respectively, flowing through M_{inj}, and R_{ds} denotes the drain-to-source resistance of M_{inj}. Q is defined as follows:

$$Q \approx \frac{R_{ds}}{2\pi f_0 L_{res}} \tag{2}$$

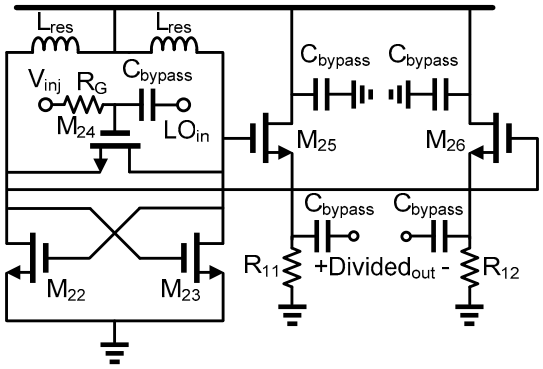


Figure 9. Schematic diagram of a basic Q-band ILFD.

According to Equation (1), the LR can be widened by increasing the injection current I_{in}.

To improve LR of the basic ILFD shown in Figure 9, two variations of ILFD employing a peaking inductor and a varactor, respectively, are presented. In Figure 10a, a peaking inductor (L_{peak}) is connected in series with M_{29j}, so that the swing of V_{ds} and thus I_{in} of M_{29} increase. This leads to a wider LR. In Figure 10b, a varactor (C_{var}) is added to tune the free-running oscillation frequency. Therefore, the LR can be extended by adjusting the oscillation frequency in accordance with the injection frequency. The parameter value of each component is presented in Table 4.

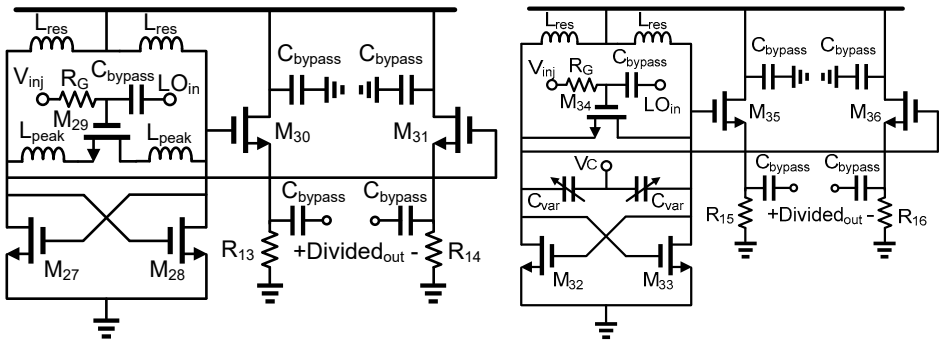
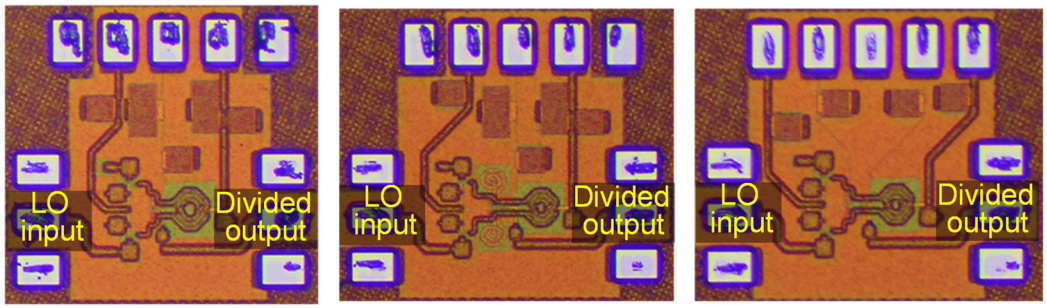


Figure 10. Schematic diagram of (**a**) ILFD with a peaking inductor and (**b**) ILFD with a varactor.

Table 4. Parameter values of the ILFDs.

Parameter	Value	Parameter	Value
M_{22}, M_{23}, M_{27}, M_{28}, M_{32}, M_{33}	3 × 13 µm	L_{res}	290 pH
M_{24}, M_{29}, M_{34}	2 × 24 µm	L_{peak}	120 pH
M_{25}, M_{26}, M_{30}, M_{31}, M_{35}, M_{36}	3 × 20 µm	C_{bypass}	1.4 pF
R_G	5 kΩ	C_{var}	41–167 fF
R_{11}–R_{16}	80 Ω		

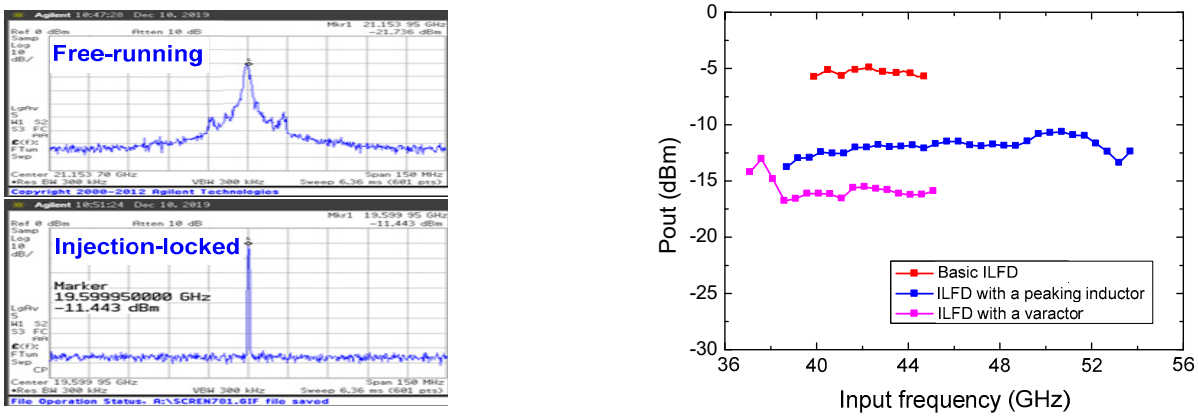
Figure 11 shows the chip micrographs of the basic ILFD, ILFD with a peaking inductor, and ILFD with a varactor. The chip sizes were 0.62 × 0.58 mm^2, 0.67 × 0.58 mm^2, and 0.66 × 0.55 mm^2, respectively, excluding the probing pads. All chips consumed 26.1 mW of DC power.



(**a**) (**b**) (**c**)

Figure 11. Chip micrographs of the (**a**) basic ILFD, (**b**) ILFD with a peaking inductor, and (**c**) ILFD with a varactor.

Figure 12 shows the measurement result of the ILFDs. Figure 12a shows the measured output spectrum in the free-running and injection-locked modes. It was observed that the output signal at 19.6 GHz was clearly locked to the injection signal of P_{LO} = 0 dBm at 39.2 GHz. Figure 12b presents a comparison of the LR and output power of the three ILFDs at P_{LO} = 0 dBm. The ILFD with a peaking inductor achieved the widest LR of 35.1% (19.4–26.9 GHz). The output power of the ILFD was no lower than −13.8 dBm over the LR.

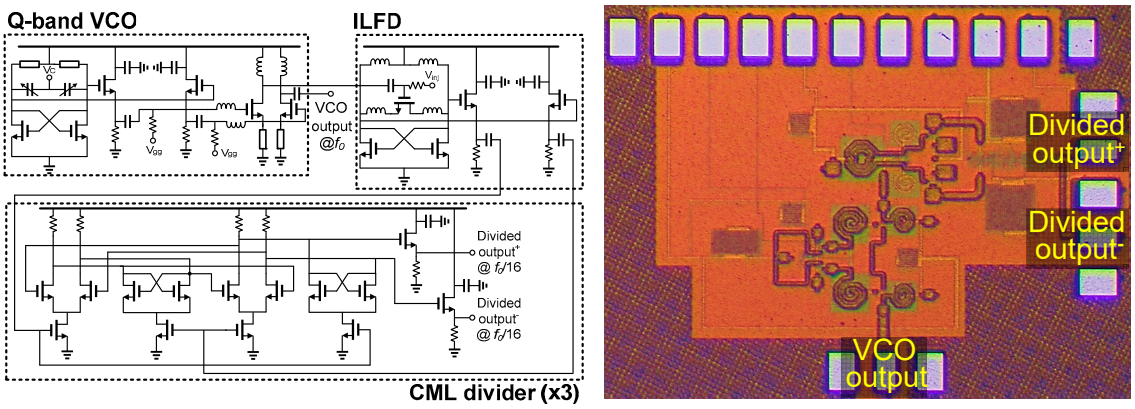


(**a**) (**b**)

Figure 12. Measurement result of the ILFDs: (**a**) output spectrum in the free-running and injection-locked modes; (**b**) LR and output power at P_{LO} = 0 dBm.

To achieve a sufficient frequency division ratio, the output of the ILFD was further divided by the subsequent CML dividers. Seven CML dividers were connected in cascade, so that the whole divider chain fulfilled a division ratio of 256 in the integrated receiver. To experimentally verify the operation of the divider chain, a reduced version of the LO test

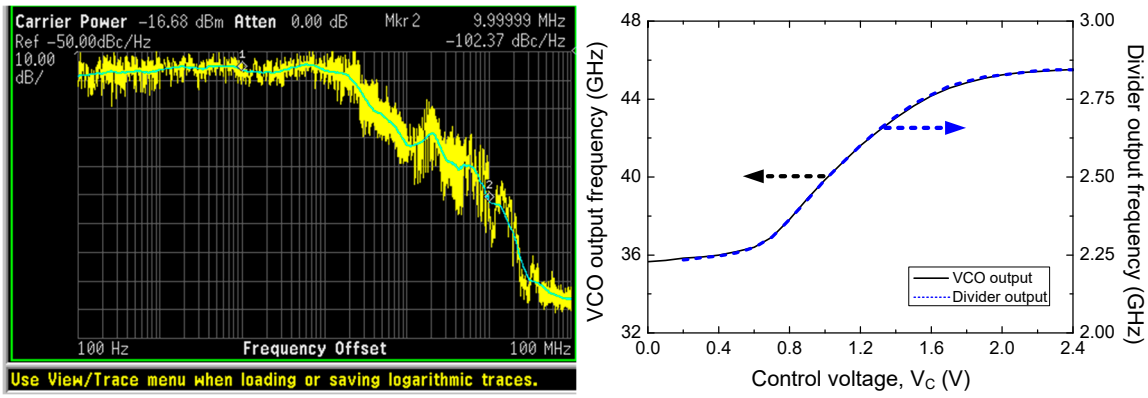
cut consisting of a Q-band VCO and a 1/16 divider chain shown in Figure 13 was tested. The divider chain was composed of the ILFD with a peaking inductor and three-stage CML divider employing a master-slave structure. One of the differential VCO output signals was monitored to check the oscillation frequency.



(**a**) (**b**)

Figure 13. (**a**) Schematic diagram and (**b**) chip micrograph of the Q-band VCO followed by a 1/16 divider chain.

Figure 14 shows the measurement results of the Q-band VCO followed by a 1/16 divider chain. The phase noise of the divided signal was −102.37 dBc/Hz at 10 MHz offset as shown in Figure 14a. Figure 14b shows the output frequency of the VCO and the divider versus the VCO control voltage. It was observed that the frequency division by 16 was exactly performed.



(**a**) (**b**)

Figure 14. Measurement results of the Q-band VCO followed by a 1/16 divider: (**a**) phase noise at 10-MHz offset and (**b**) output frequency of the VCO and divider versus the VCO control voltage.

4. Measurement of the Q-Band Image-Rejection Receiver

A Q-band image-rejection receiver integrated the circuit blocks described in Section 3 on a single chip, as shown in Figure 15. The chip area was 2.5 × 1.6 mm^2 including the probing pads.

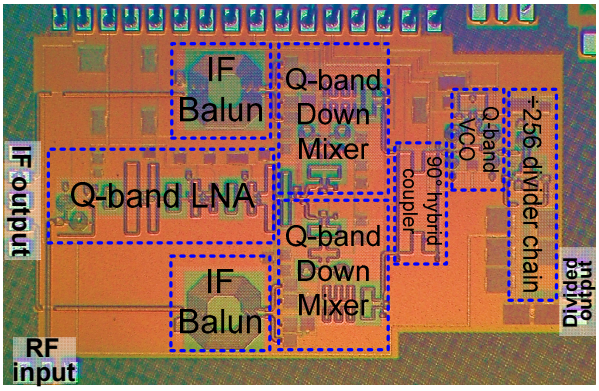


Figure 15. Chip micrograph of the Q-band image-rejection receiver.

The measurement result of the image-rejection receiver is shown in Figure 16. The conversion gain was measured versus the IF frequency while the LO frequency was fixed at 40 GHz. As shown in Figure 16a, the receiver exhibited a peak conversion gain of 16.4 dB at 43 GHz and a 3 dB bandwidth of 3.5 GHz (1.5–5 GHz). The noise figure was simulated to be 5.8–7.8 dB over the 3 dB bandwidth. Figure 16b shows the measured IMRR, which ranged from 35.6 to 55.1 dBc over the same bandwidth. The input 1 dB compression power (IP_{1dB}) was −28 dBm at the IF frequency of 2.5 GHz.

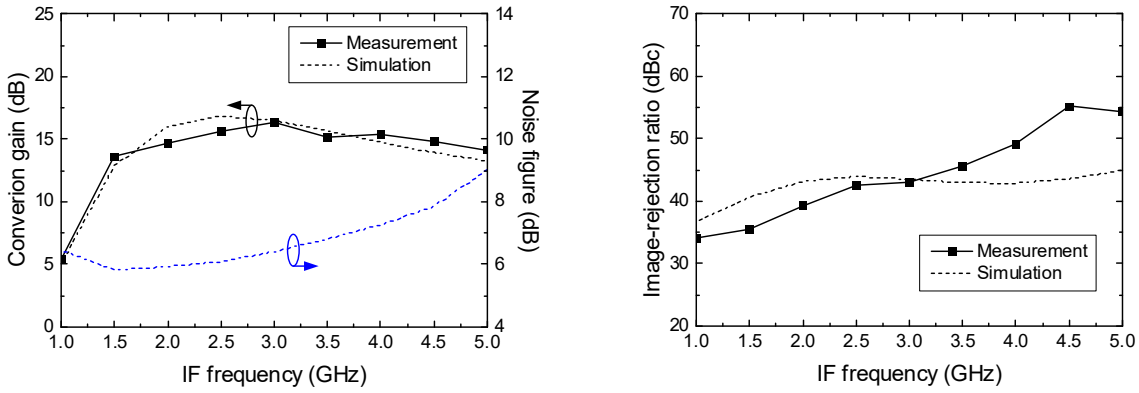


Figure 16. Measurement of the Q-band image-rejection receiver: (**a**) conversion gain, noise figure, and (**b**) image-rejection ratio.

In Table 5, the performance of the Q-band image-rejection receiver is summarized and compared with those of previously reported silicon-based receivers in a similar frequency band. Compared with other image-rejection receivers, this work achieved a high IMRR at a reasonably low IF frequency below 5 GHz using the Hartley structure. It should be noted that a high IMRR was achieved in [13] by using a high IF frequency of 16 GHz. In addition, the LO circuit consisting of a VCO and a 1/256 divider chain was integrated in this work, which facilitated locking to a low-frequency LO reference.

Table 5. Performance summary and comparison.

Ref.	Process	RF Freq. (GHz)	Architecture	CG [1] (dB)	NF [2] (dB)	IP_{1dB} (dBm)	IMRR (dBc)	P_{dc} (mW)
[6]	65 nm CMOS	22.5–26.1	LNA + Mixer + AMP_{IF} [3] + AMP_{LO} [4] + PPF_{LO} [5]	31.5	4.8	−35.2	-	127.44
[9]	0.12 µm SiGe	10–40	LNA + Mixer + VGA_{IF} [6] + ×4 + AMP_{LO} [4]	39	6.8	−33	-	130
[10]	0.13 µm SiGe	25–45	LNA + Mixer + ×3 + AMP_{LO} [4]	21	5	-	30	-
[11]	45 nm SOI CMOS	24–44	LNA + Mixer + AMP_{IF} [3] + AMP_{LO} [4]	35.2	3.2	−25.5	32	60
[13]	22 nm SOI CMOS	20–44	LNA + Mixer + AMP_{IF} [3] + AMP_{LO} [4]	28.5	3.3	−25	75	70
[16]	22 nm SOI CMOS	19.5–42	LN-VGA + mixer + LPF + AMP_{IF} [3] + AMP_{LO} [4] + IQ_{GEN} [7]	25.3	2.7	−23	-	102
[17]	65 nm CMOS	26.5–32.5	LNA + Mixer + $Buff_{IF}$ [8] + AMP_{LO} [4] + PPF_{LO} [5]	29.5	5.3	−28	-	33
This work	**65 nm CMOS**	**41.5–45**	**LNA + Mixer + VCO + 1/256 divider**	**16.4**	**5.8**	**−28**	**35.6**	**91.9 + 294 (divider chain)**

[1] Maximum conversion gain over the bandwidth. [2] Lowest NF over the bandwidth. [3] IF amplifier. [4] LO amplifier. [5] LO poly phase filter. [6] IF variable gain amplifier. [7] I-Q generator. [8] IF buffer.

5. Conclusions

In this paper, a Q-band image-rejection receiver was developed using a 65 nm bulk CMOS technology, which is relatively cost-effective and easily accessible. The Q-band receiver employing a Hartley architecture for a high IMRR integrates a Q-band LNA, two Q-band down-conversion mixers, a 90° hybrid coupler, two IF baluns, and an LO circuit. The integrated LO consists of a Q-band fundamental VCO followed by a 1/256 divider chain, which fulfills a high division ratio. This facilitates the LO locking to an external phase-locked loop (PLL). The Q-band image-rejection receiver exhibits a peak conversion gain of 16.8 dB and a high IMRR of 35.6 dB with IP_{1dB} of −28 dBm. This receiver can be employed for future 5G mm-wave communication.

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References

1. Kim, S.; Kim, B.; Lee, Y.; Kim, S.; Shin, H. A 28 GHz direct conversion receiver in 65nm CMOS for 5G mmWave radio. In Proceedings of the International System-on-Chip Design Conference (ISOCC), Jeju, Korea, 6–9 October 2019; pp. 29–30.
2. Wong, A.C.-W.; Devita, G.; Wu, S.-M.; Lauria, F.; Eid, M.; Illuromi, O.; Ogunkunle, S.; Modigliana, A. A 4Rx, 4Tx Ka-band transceiver in 40 nm bulk CMOS technology for satellite terminal applications. In Proceedings of the IEEE Radio Frequency Integrated Circuits Symposium (RFIC), Atlanta, GA, USA, 7–9 June 2021; pp. 211–214.

3. Liu, X.; Yang, C.; Yang, Z.; Guo, Y.; Jin, J.; Shi, L.; Xu, Q.; Wu, L.; Zhou, J. Area-Efficient 28-GHz Four-Element Phased-Array Transceiver Front-End Achieving 25.2% Tx Efficiency at 15.68-dBm Output Power. *IEEE Trans. Microw. Theory Tech.* **2023**, *71*, 654–668. [CrossRef]
4. Yuan, Y.; Li, N.; Zhou, J.; Gao, H.; Wang, S.; Lu, H.; Gu, Q.J.; Song, C.; Xu, Z. A Compact Ka-Band Eight-Element Four-Beam Receiver for Low-Earth-Orbit Satellite Communications in 65-nm CMOS. *IEEE Microw. Wireless Tech. Lett.* **2023**, *33*, 883–886. [CrossRef]
5. Kim, H.-T.; Park, B.-S.; Song, S.-S.; Moon, T.-S.; Kim, S.-H.; Kim, J.-M.; Chang, J.-Y.; Ho, Y.-C. A 28-GHz CMOS Direct Conversion Transceiver with Packaged 2 × 4 Antenna Array for 5G Cellular System. *IEEE J. Solid State Circ.* **2018**, *53*, 1245–1259. [CrossRef]
6. Lee, Y.; Kim, S.; Shin, H. A 24 GHz CMOS Direct-Conversion RF Receiver with I/Q Mismatch Calibration for Radar Sensor Applications. *Sensors* **2022**, *22*, 8246. [CrossRef] [PubMed]
7. Shiramizu, N.; Nakamura, T.; Masuda, T.; Washio, K. A 24-GHz low-power fully integrated receiver with image-rejection using rich-transformer direct-stacked/coupled technique. In Proceedings of the IEEE Radio Frequency Integrated Circuits Symposium (RFIC), Anaheim, CA, USA, 23–25 May 2010; pp. 369–372.
8. Fonte, A.; Plutino, F.; Moquillon, L.; Razafimandimby, S.; Pruvost, S. 5G 26 GHz and 28 GHz bands SiGe:C receiver with very high-linearity and 56 db dynamic range. In Proceedings of the 2018 13th European Microwave Integrated Circuits Conference (EuMIC), Madrid, Spain, 23 September 2018; pp. 57–60.
9. Ma, Q.; Chung, H.; Rebeiz, G.M. A 4-channel 10–40 GHz wideband receiver with integrated frequency quadrupler for high resolution millimeter-wave imaging systems. In Proceedings of the 2018 IEEE MTT-S International Microwave Symposium (IMS), Philadelphia, PA, USA, 10–15 June 2018; pp. 883–886.
10. Milner, L.E.; Harvey, J.T.; Parker, M.E.; Hall, L.T.; Rodriguez, M.C.; Heimlich, M.C.; Mahon, S.J. A 25 to 45 GHz SiGe receiver MMIC. In Proceedings of the 2016 11th European Microwave Integrated Circuits Conference (EuMIC), London, UK, 3–4 October 2016; pp. 548–551.
11. Huang, M.-Y.; Chi, T.; Wang, F.; Li, S.; Huang, T.-Y.; Wang, H. A 24.5–43.5 GHz compact RX with calibration-free 32-56 dB full-frequency instantaneously wideband image rejection supporting multi-Gb/s 64-QAM/256-QAM for multi-band 5G massive MIMO. In Proceedings of the IEEE Radio Frequency Integrated Circuits Symposium (RFIC), Boston, MA, USA, 2–4 June 2019; pp. 275–278.
12. El-Nozahi, M.; Amer, A.; Sanchez-Sinencio, E.; Entesari, K. A Millimeter-Wave (24/31-GHz) Dual-Band Switchable Harmonic Receiver in 0.18-µm SiGe Process. *IEEE Trans. Microw. Theory Tech.* **2010**, *58*, 2717–2730. [CrossRef]
13. Li, G.; Ma, Q.; Rebeiz, G.M. A 20–44-GHz Image-Rejection Receiver With >75-dB Image-Rejection Ratio in 22-nm CMOS FD-SOI for 5G Applications. *IEEE Trans. Microw. Theory Tech.* **2020**, *68*, 2823–2832.
14. Huang, M.-Y.; Chi, T.; Li, S.; Huang, T.-Y.; Wang, H. A 24.5–43.5-GHz ultra-compact CMOS receiver front end with calibration-free instantaneous full-band image rejection for multiband 5G massive MIMO. *IEEE J. Solid State Circ.* **2020**, *55*, 1177–1186. [CrossRef]
15. Quadrelli, F.; Manente, D.; Seebacher, D.; Padovan, F.; Bassi, M.; Mazzanti, A.; Bevilacqua, A. A Broadband 22–31-GHz Bidirectional Image-Reject Up/Down Converter Module in 28-nm CMOS for 5G Communications. *IEEE J. Solid State Circ.* **2022**, *57*, 1968–1981. [CrossRef]
16. Gao, L.; Rebeiz, G.M. A 20–42-GHz IQ Receiver in 22-nm CMOS FD-SOI With 2.7–4.2-dB NF and −25-dBm IP1dB for Wideband 5G Systems. *IEEE Trans. Microw. Theory Tech.* **2021**, *69*, 4951–4960. [CrossRef]
17. Singh, R.; Mondal, S.; Paramesh, J. A Millimeter-Wave Receiver Using a Wideband Low-Noise Amplifier with One-Port Coupled Resonator Loads. *IEEE Trans. Microw. Theory Tech.* **2020**, *68*, 3794–3803. [CrossRef]
18. Razavi, B. *RF Microelectronics*; Prentice Hall: Hoboken, NJ, USA, 2012.
19. Hartley, R. Modulation System. U.S. Patent 1,666,206, 17 April 1928.
20. Gilbert, B. A precise four-quadrant multiplier with subnanosecond response. *IEEE J. Solid State Circ.* **1968**, *3*, 365–373. [CrossRef]
21. Sulivan, P.J.; Xavier, B.A.; Ku, W.H. Low voltage performance of a microwave CMOS Gilbert cell mixer. *IEEE J. Solid State Circ.* **1997**, *32*, 1151–1155. [CrossRef]
22. Lee, S.-J.; Kim, B.; Lee, K. A novel high-speed ring oscillator for multiphase clock generation using negative skewed delay scheme. *IEEE J. Solid State Circ.* **1997**, *32*, 289–291.
23. Castañeda-Aviña, P.R.; Tlelo-Cuautle, E.; De la Fraga, L.G. Phase noise optimization of integrated ring voltage-controlled oscillators by metaheuristics. *AIMS Math.* **2022**, *7*, 14826–14839. [CrossRef]
24. Maggio, G.M.; Feo, O.D.; Kennedy, M.P. VCOs can be designed using ring-type, colpitts, and cross-coupled structures. *IEEE Trans. Circ. Syst. I Fundam. Theory Appl.* **1999**, *46*, 1118–1130. [CrossRef]
25. Hajimiri, A.; Lee, T.H. Design issues in CMOS differential LC oscillators. *IEEE J. Solid State Circ.* **1999**, *34*, 717–724. [CrossRef]
26. Razavi, B. *Design of Integrated Circuits for Optical Communications*; McGraw-Hill: New York, NY, USA, 2003.
27. Alioto, M.; Palumbo, G. *Model and Design of Bipolar and MOS Current-Mode Logic: CML, ECL and SCL Digital Circuits*; Springer Science & Business Media: Berlin/Heidelberg, Germany, 2006.

28. Tiebout, M. A CMOS Direct Injection-Locked Oscillator Topology as High-Frequency Low-Power Frequency Divider. *IEEE J. Solid State Circ.* **2004**, *39*, 1170–1174. [CrossRef]
29. Cheng, J.-H.; Tsai, J.-H.; Huang, T.-W. Design of a 90.9% Locking Range Injection-Locked Frequency Divider with Device Ratio Optimization in 90-nm CMOS. *IEEE Trans. Microw. Theory Tech.* **2016**, *65*, 187–197. [CrossRef]