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A Data Weight Averaging-Inspired Digital Calibration Method for a 10-Bit Noise-Shaping Successive Approximation Register

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Abstract: This paper presents a digital calibration method for a 10-bit noise-shaping Successive Approximation Register Analog to Digital Converter (SAR ADC). The proposed calibration method is inspired by its Data Weight Averaging (DWA) counterpart, but stays static, while achieving a similar Integral Nonlinearity (INL) and 1.3 dB better Signal-to-Noise Ratio (SNR) in measurements without oversampling. This advantage in SNR holds until an Oversampling Ratio (OSR) of 2 for the proposed method, which also saves 50 % power. At a 1.2 V power supply, the ADC consumes a power of 70 µW at a conversion rate of 50 kHz. Fabricated using 55 nm Complementary Metal Oxide Semiconductor (CMOS) Metal-Oxide-Metal Capacitor (MOMCAP) technology, it occupies an active area of 370 µm × 350 µm, when achieving an INL of 0.3 Least Significant Bit (LSB) and an SNR of 66.9 dB at an OSR of 8.

Keywords: successive approximation analog-to-digital converters; SAR; ADC; redundancy; digital background calibration; data weight averaging

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1. Introduction

SAR ADCs are energy efficient designs with reasonable accuracy. They are suitable for audio applications that require sampling speeds around 100 kHz [1]. However, two factors, capacitor mismatches and noise, limit their effective resolutions [2,3]. The capacitor mismatches give rise to dynamic and static nonlinearity by making each capacitor's real weight deviate from its nominal one. It is usually believed that the mismatches from the four Most Significant Bit (MSB) capacitors, rather than those from the LSBs, affect the accuracy of a 10-bit SAR ADC [4–7], for instance. For the aforementioned 10-bit SAR, supposing the 5th bit has a 1% mismatch, for its bit weight of 32, the INL may be degraded by approximately 32 × 1% = 0.32 LSB. On the other hand, the minimum unit capacitor selected based on noise considerations has a mismatch worse than 0.1%, for most modern technologies. By quadrupling the unit capacitor size, the mismatch error can by reduced by half [8]. However, this goes against the low power design aim [8]. According to [8–18], currently, there are two mainstream solutions for reducing mismatches: (1) The analog Mismatch Error Shaping (MES) method, where the capacitor mismatches are fed back and 1st or 2nd order shaped. Its advantage lies in its simple architecture. However, its problem is in addition to the mismatch error, its input signal is also fed back. (2) The digital-domain methods, which include Dynamic Element Matching (DEM) and DWA, alternatively select each element. The principle of the DWA is to ensure that each element, among the thermometer capacitors, is used an equal number of times.

Following the aforementioned principle of the DWA, the thermometer capacitors can be selected either in a random or in an elaborate manner to reform the four "8 + 4 + 2 + 1" MSBs [7]. For instance, for the current conversion cycle, the first eight thermometer capacitors can be employed as the MSB while for the next cycle, the first two capacitors can

be used to form the third bit and the MSB can consist of the 3rd to the 10th thermometer capacitors, etc. The DWA method suppresses the mismatches but consumes dynamic power by continuously switching. Another concern is its effects have to be improved with OSR. Inspired by the aforementioned DWA principle and motivated to save both dynamic power and OSR, this paper proposes a digital calibration method that attempts to select the optimum combination of 15 thermometer capacitors to reform the four MSBs, which achieves the best possible dynamic and static linearity. After the selection has been made, the combination stays unchanged for the entire operation of the SAR ADC. In this way, compared to its alternative using DWA, the proposed calibration saves 50% digital power by staying static while achieving a similar INL and a 1.3 dB better SNR, without oversampling. Its advantage in SNR over the DWA holds until OSR = 2 during measurements. In this way, the averaging of mismatches is performed spatially for the proposed method rather than dynamically as for the DWA. In addition, the experimental results verify that the spatial selection of thermometer capacitors to form the four MSBs can be global for the same batch. Therefore, the DWA logic can be removed from the future tape-outs for the same technology. We use noise-shaping SAR architecture [8–18] to alleviate the aforementioned noise limitation.

The detail of the proposed calibration method is explained in Section 2, along with the architecture of the SAR ADC. Section 3 describes the schematic of the proposed ADC. The experimental results of the SAR ADC before and after calibration and when compared to the DWA alternative are presented in Section 4. Section 5 concludes this paper.

2. Principle of the Proposed Calibration Method with MATLAB Modeling

The 10-bit noise-shaping (NS) SAR ADC is shown in Figure 1. Figure 2 shows the layout of its Capacitive Digital-to-Analog Converter (CDAC) array. Assuming the effect of gradient (e.g., for oxide thickness) on the CDAC is linear [19], each of the 15 thermometer capacitors, $C_{M,i}$, can be modelled as

$$C_{M,i} = C_0(1 + \varepsilon_0 i),\ i = 1 \sim 15; \tag{1}$$

where C_0 is the nominal bit weight for the 15 thermometer capacitors and $C_0 = 64C_u$. In addition, over-etching affects the real value of the capacitors [8], especially for those located at the edge of the array, e.g., C_{M1} and C_{M15}, which we re-model as

$$C_{M,i} = C_0(1 + \varepsilon_0 i)(1 - \varepsilon_1),\ i = 1, 15; \tag{2}$$

where $\varepsilon_0$andε_1 are uncorrelated; the former can be positive or negative while the latter is most likely positive. Suppose a 4-bit decoder is connected to the SAR logic that selects $C_{M1\sim15}$ sequentially to reform the four MSBs. For example, when the input of the 4-bit decoder is 0001, C_{M1}~C_{M8}, C_{M9}~C_{M12}, C_{M13}~C_{M14}, and C_{M15} constitute the first, second, third, and fourth largest bits, respectively. Otherwise, if the 4-bit decoder input is 0010, C_{M2}~C_{M9}, C_{M10}~C_{M13}, C_{M14}~C_{M15}, and C_{M1} constitute the first, second, third, and fourth largest bits, respectively, etc.

As C_0 represents the common factors in Equations (1) and (2) and $C_{M1\sim M15}$ form an arithmetic sequence, without considering the over-etching expressed by Equation (2), only the ratio between ε_0 and ε_1 can possibly affects the trend of the resulting error due to mismatches. To verify the aforementioned prediction, we input the models expressed in Equations (1) and (2) into MATLAB along with various ratios between ε_0 and ε_1. Figure 3 shows the simulated summed errors in LSB in MATLAB. It indicates that when the decoder input is around 0010 or 1010, the summed error reaches a minimum. In addition, the exact digital inputs for the minimum error vary within two digits depending on the ratios between the over-etching factor and the oxide thickness gradient ($\varepsilon_1/\varepsilon_0$).

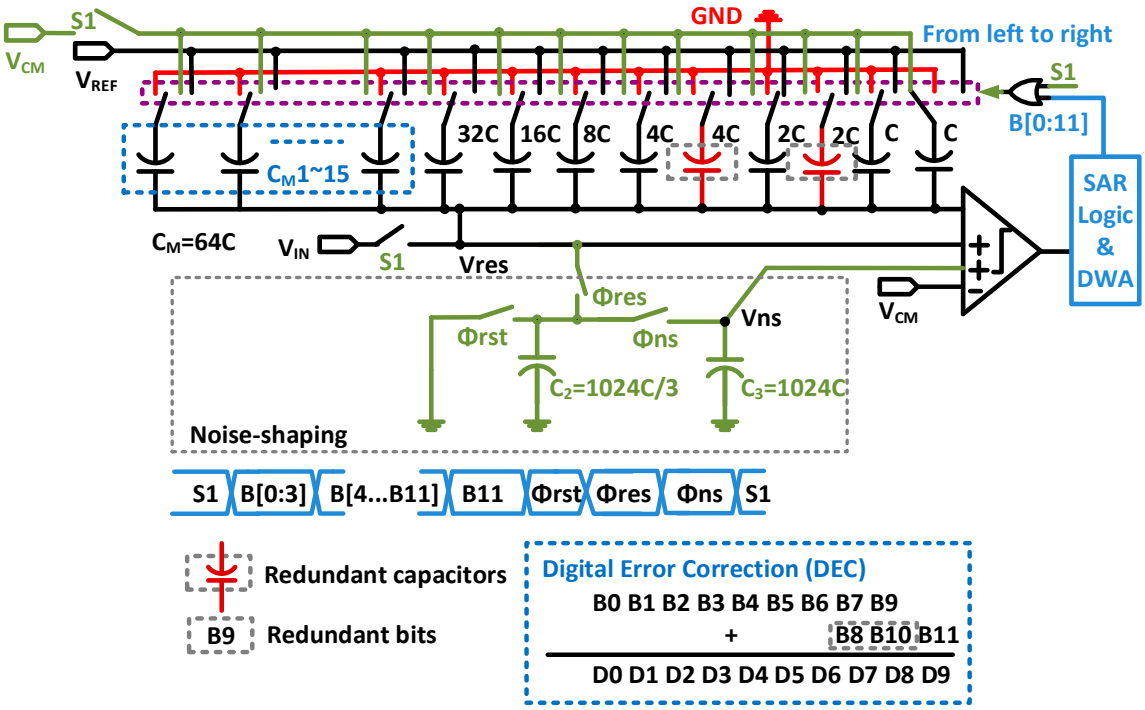

Figure 1. Proposed 10-bit noise-shaping SAR schematic with 15 thermometer capacitors. The ADC is fully differential but drawn as single-sided for simplicity.

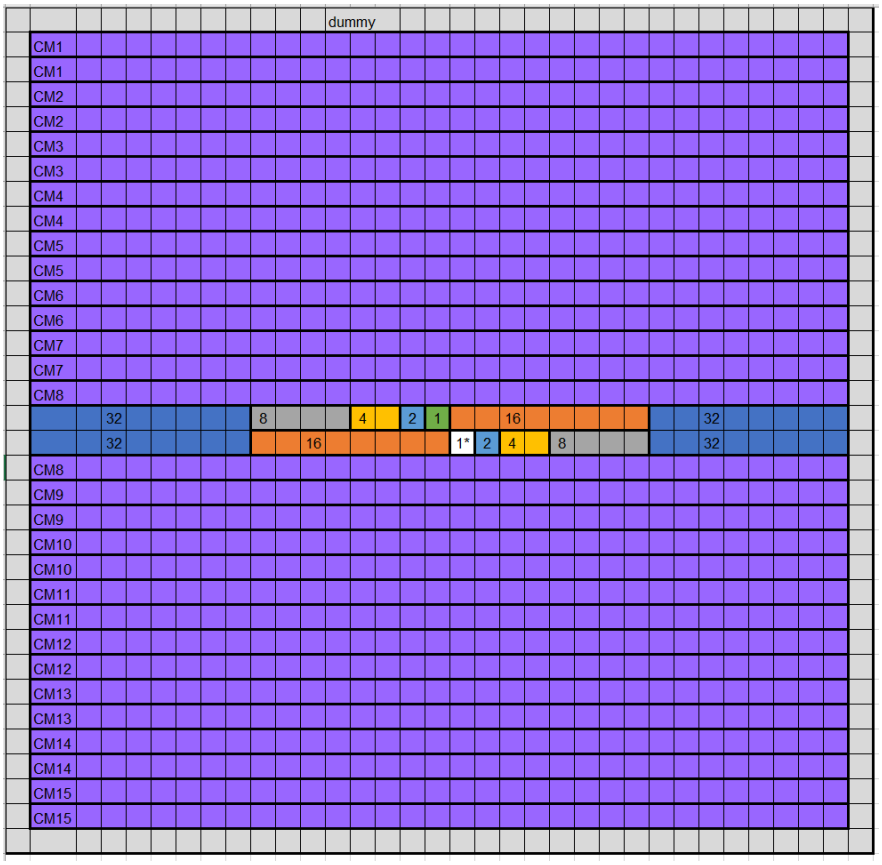

Figure 2. Layout of the CDAC in the proposed SAR ADC. The redundancy is not shown for simplicity. 1* is the unity dummy capacitor.

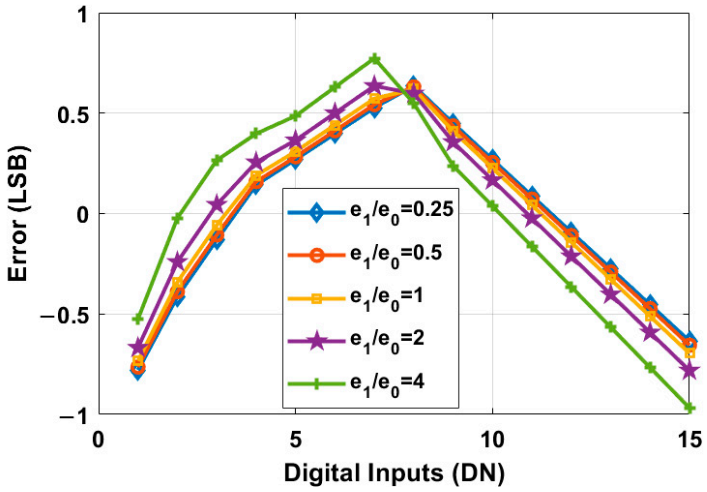

Figure 3. MATLAB-simulated errors in LSB versus the 15 digital inputs of the 4-bit decoder. The error reaches its minimum around the digital inputs of 2 (0010) or 10 (1010).

From Figure 3, we predict that the decoder input where the summed error reaches its minimum is highly spatially correlated despite various $\varepsilon_1/\varepsilon_0$ ratios. It should be noted that the model we present in Equations (1) and (2) is the simplest model for understanding the mismatch problem as well as the proposed solution. In practice, much more complex models may apply.

3. Circuit Implementation

The schematic of the 10-bit SAR ADC in the proposed design is shown in Figure 1. Two redundant capacitors, 4C and 2C, were added. A DWA logic was connected to the 15 thermometer capacitors ($C_{M1\sim M15}$), and its pattern can be controlled off-chip through a Field Programmable Gate Array (FPGA). The pattern can be a Pseudo-Random Number Generator (PRNG), which can be implemented by a Linear Feedback Shift Register (LFSR) that selects 8, 4, 2 or 1 capacitor out of the 15, as the 1st, 2nd, 3rd, and 4th bit, respectively. For the PRNG DWA, for each consecutive conversion, a different combination of eight capacitors is selected as the MSB, although this pattern may repeat itself. Inspired by this DWA method, we propose fixing the combinations of the thermometer capacitors to form the four MSBs and testing the resulting static and dynamic nonlinearity of the ADC. The above measurement is repeated for each of the 15 combinations. Eventually, we chose the one that has the optimum linearity—the lowest INL and the highest SNR—and fixed this choice for the ADC's operation.

To break up the limitation of comparator noise on the ADC performance [2,8–18], a 1st-order noise-shaping was applied to the ADC, as shown in Figure 1. Its noise-shaping transfer function is

$$NTF(z) = 1 - 0.75z^{-1} \quad (3)$$

Through this function, the comparator input is referred and quantization noise is shaped. The NTF zero is located at 0.75.

4. Measurement Results and Discussion

4.1. Prototype and Measurement Setup

A fully differential prototype of the SAR ADC shown in Figure 1 was implemented using 55 nm CMOS MOMCAP technology. Its chip micrograph is shown in Figure 4. The SAR ADC has an area of 370 × 350 μm^2. Each CDAC MOMCAP array occupies 100 × 130 μm^2. Its unit capacitor is 5 fF, whose value is determined by the trade-off between the mismatches and the layout floor plan. Powered by a 1.2 V voltage supply, the ADC's analog and digital parts consume 60 μW and 10 μW, respectively. The DWA's

power consumption is 10 µW. When it stays static for the proposed method, its power is negligible. Figures 5–11 show the measurements for 16.87 Hz, 680 mVp-p (−2.5 dB) differential sinewave inputs.

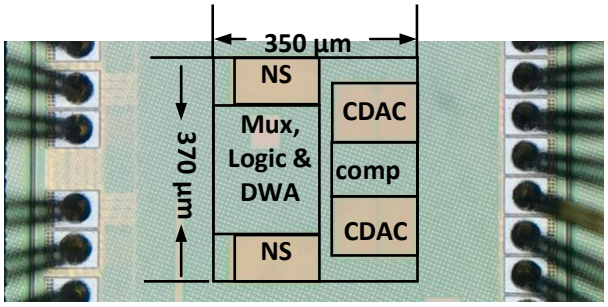

Figure 4. Micrograph of the SAR ADC chip, with each block marked. On the left and right sides are the bonding wires for packages.

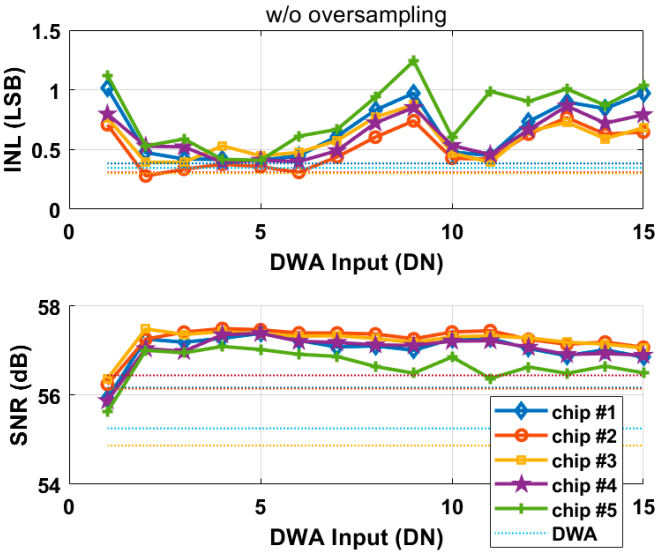

Figure 5. Measured INL and SNR of the ADC when the DWA's selection is fixed, for 15 combinations. It can be seen that the nonlinearity is at its best around the digital inputs of 2 (0010) and 10 (1010).

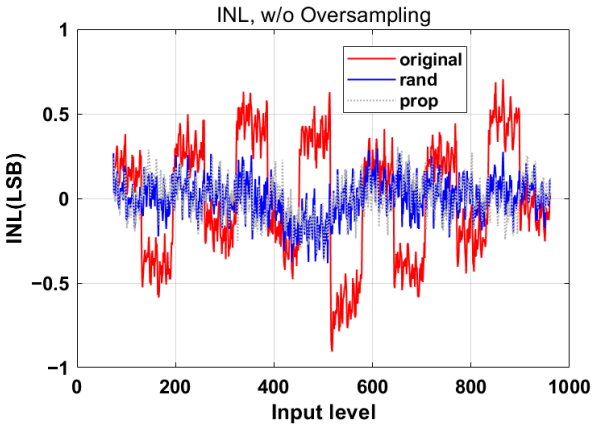

Figure 6. Measured INL of the SAR ADC without oversampling; "original", "rand", and "prop" stand for before calibration, PRNG DWA, and the proposed method, respectively. This is measured from chip #3. Both the proposed and the PRNG DWA can reduce the worst-case INL by approximately 0.6 LSB.

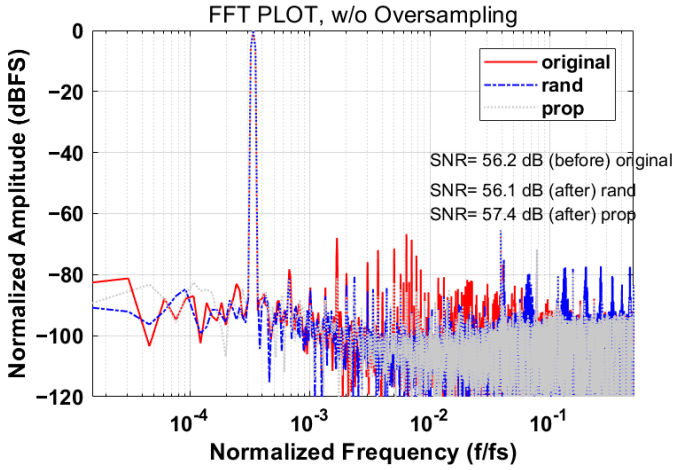

Figure 7. Measured SNR of the SAR ADC, without oversampling, when measured at an input level of −2.5 dB from chip #3. The proposed ('prop') method can improve the SNR by an additional 1.3 dB compared to its DWA ('rand') alternative.

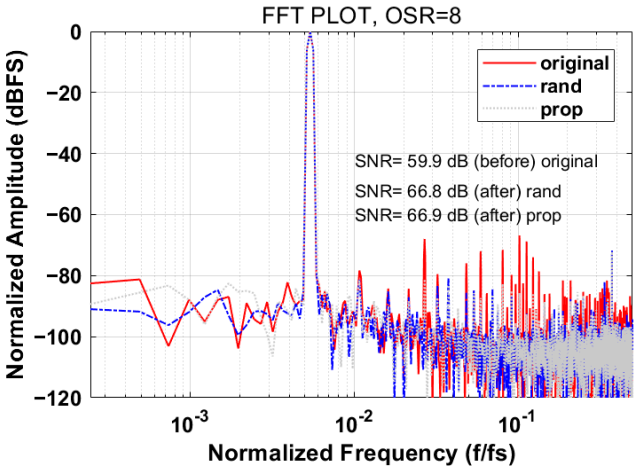

Figure 8. Measured SNR of the SAR ADC versus the OSR, for five chips. OSR = 0.5 means without oversampling. The proposed method's digital input is fixed at 0010. When the OSR is equal to or less than 2, the proposed ('prop') method has better SNR compared to the DWA ('rand').

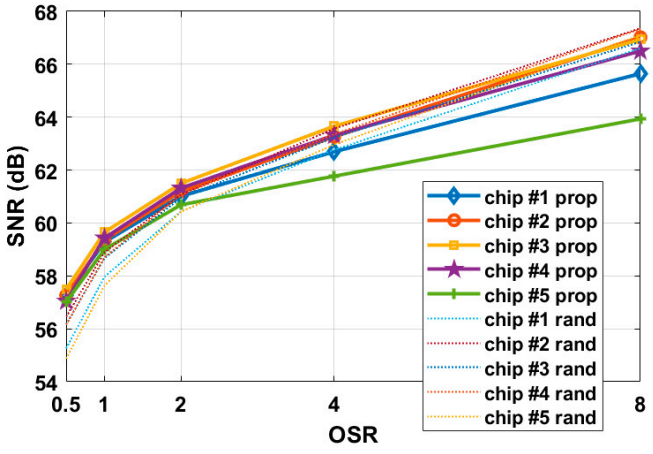

Figure 9. Measured SNR of the SAR ADC, at an OSR of 8, measured at an input level of −2.5 dB, from chip #3. It can be seen both the proposed ('prop') and the DWA ('rand') method can improve the SNR by approximately 7 dB.

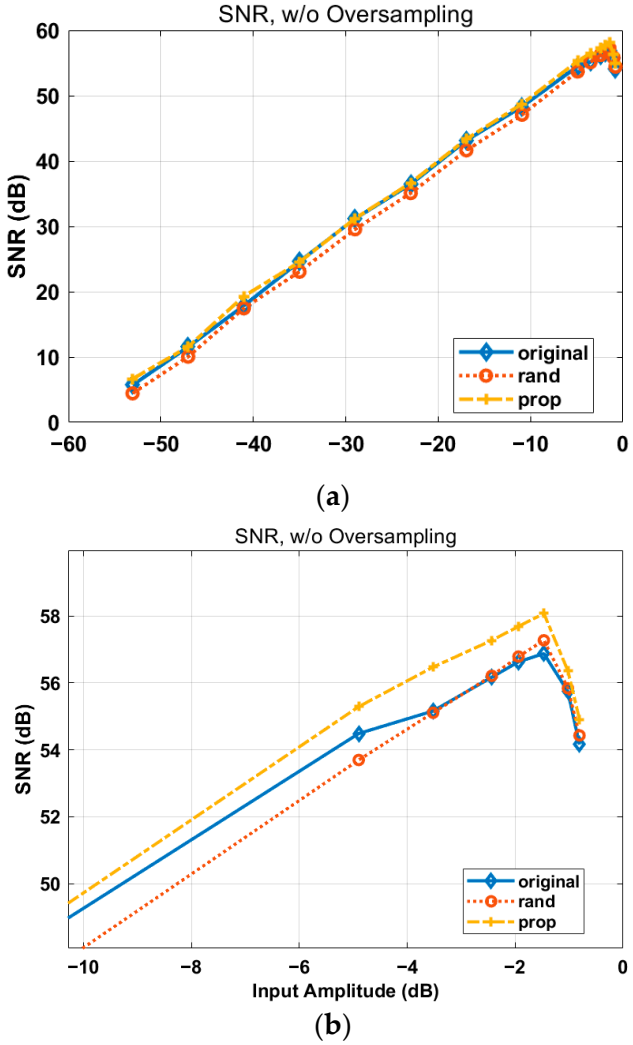

Figure 10. (**a**) Measured SNR of the SAR ADC versus the input amplitude and (**b**) Its zoom-in around −2 dB. This is measured from chip #3 at 0010 and without oversampling. The proposed ('prop') method has better SNR than that of the DWA ('rand').

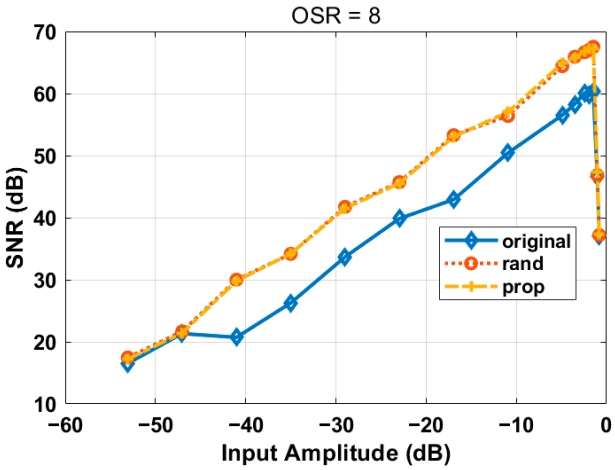

Figure 11. Measured SNR of the SAR ADC versus the input amplitude and its zoom-in around −2 dB; "original", "rand", and "prop" represent before calibration, PRNG DWA, and the proposed method, respectively. This is measured from chip #3 at 0010 and OSR = 8. Both the proposed ('prop') and the DWA ('rand') can improve the SNR by 7 dB, between the −40 dB and −1 dB input level.

4.2. Proposed Method—Static and Dynamic Linearity vs. 4-Digit Inputs

Rather than rotating/shifting the thermometer capacitors to form the four MSBs, as in a DWA method, we propose fixing this selection of the 4-digit DWA inputs, for one measurement, and then obtain its INL and SNR. Later, we rotate and start a new measurement and obtain its INL and SNR. Eventually, INL and SNR for all 15 combinations are measured and compared in Figure 5 for five chips without oversampling. This measured INL is similar to that simulated in Figure 3, in the way that it is smaller for digital inputs around 0010 and 1010 and larger for those around 1000, for all five chips from the same batch. Another observation that can be made is except for the DWA input at 0001, the measured SNR is higher for the proposed method compared to its DWA alternative. This is probably because the proposed method does not introduce additional noise source as in a PRNG DWA [6].

4.3. Proposed Method vs. DWA without Oversampling

As observed at the DWA input of 2 (0010), not only is the measured INL at its minimum, but the SNR is also at its maximum for our proposed method. We selected 0010 for the following experiments, and we fixed this selection and compared it to the PRNG DWA. Figure 6 shows the measured INL of the ADC for three conditions: "original"—without calibration, "rand"—when DWA is on, and "prop"—when the proposed calibration method is on.

Figure 7 shows the SNR measured with the same setup as that in Figure 6. The 1st-order noise-shaping is turned on for all of the above three conditions. From Figure 6, one can observe that without oversampling or calibration, the ADC's INL is measured to be around 1 LSB. With the use of the proposed method, its worst-case INL is reduced by approximately 0.6 LSB, to 0.3 LSB, which is similar to that when using the DWA alternative. Shown in Figure 7, the DWA and the proposed method remove a similar portion of the second-order harmonic distortion despite that the latter removes more third- and fourth-order harmonic distortions. Moreover, the proposed method does not show visible higher-order distortions such as the PRNG DWA without oversampling. As a result, the proposed method achieves a 1.3 dB better SNR. In addition, it consumes 50% less digital power, for staying static, compared to the PRNG DWA. From Figures 6 and 7, we observe that the proposed method may be suitable for SAR ADCs without oversampling.

4.4. Proposed Method vs. OSR

Then, we still fix the digital inputs at 0010 for the proposed method and increase OSR and measure its SNR, for an input amplitude at −2.5 dB. The measurement results shown in Figure 8 compare the measured SNR for the proposed "prop" and the DWA "rand". From Figure 8, one can deduce that until an OSR of 2, the proposed method has better SNR, and beyond OSR = 4, the situation varies among the five chips. For example, as shown in Figure 9, at OSR = 8, chip #3's measured SNR is 0.1 dB better using the proposed method, which suppresses a larger portion of the second-order harmonic distortion. Figure 9 shows that at an OSR of 8, both the proposed and the DWA method improve the ADC's SNR by approximately 7 dB compared to the case before calibration. The reason that the proposed method loses its advantage over the DWA alternative, beyond higher OSR, is that the harmonic distortions caused by the latter are moved to higher frequencies.

4.5. Proposed Method vs. Input Amplitude

The measured SNR versus the input sinewave amplitude, between −53 dB and −1 dB, without oversampling, is shown in Figure 10. It can be observed in Figure 10 that the proposed method ('prop') has slightly better SNR compared to the DWA ('rand') within the measured input range. Figure 11 shows the measured SNR for the same setup as that in Figure 10, except that its OSR is 8. One can deduce from Figure 11 that both the proposed and the DWA method can improve the measured SNR by approximately 7 dB, with an OSR = 8, between the input amplitude of −40 dB and −1 dB.

4.6. Design Complexity

In this design, for flexibility, the DWA logic is implemented by an off-chip FPGA, which may also be replaced by on-chip placed and route-synthesized logic using the same Verilog code for future tape-outs. Alternatively, employing the proposed method, it is also possible to remove the DWA logic that is implemented by the FPGA, especially for the same technology node, as the combination of capacitors for the optimum dynamic and static linearity is fixed and holds for chips from the same batch, as demonstrated in the experimental results shown in Figure 5. In this way, the averaging of mismatches is performed spatially rather than dynamically, and the design complexity can be kept low.

4.7. Potential for Higher Resolution

As the measured INL is around 0.25 LSB for the proposed method, as shown in Figure 6, it is probable that the accuracy of the current design still holds for a 11-bit one, which is 1 bit higher. As illustrated in Figure 8, with noise-shaping and an increased number of OSRs, the ADC's ENOB has the potential to increase further.

5. Conclusions

We propose a DWA-inspired digital calibration method for SAR ADCs. The proposed method achieves similar INL and 1.3 dB better SNR compared to its DWA alternative without oversampling. It manifests better SNR until an OSR of 2. In addition, it saves the DWA switching power and hence the digital power by 50%. Therefore, we conclude that the proposed method can work as a low-power alternative for lower OSRs for SAR ADCs. It is compared with the DWA method in Table 1.

Table 1. Comparison of the proposed method with the DWA and before calibration.

		Proposed Method	**DWA**	**Before Calibration**
Technology		55 nm	55 nm	55 nm
ADC Type		NS SAR	NS SAR	NS SAR
Power Supply		1.2 V	1.2 V	1.2 V
Power Consumption		70 µW	80 µW	70 µW
Sampling Frequency		50 kHz	50 kHz	50 kHz
No Oversampling	INL	0.3 LSB	0.4 LSB	1 LSB
	SNR	57.4 dB	56.1 dB	56.2 dB
	ENOB	9.2 bits	9.0 bits	9.0 bits
	[a] FOM (pJ/conv)	2.4	3.1	2.7
	[b] FOMs	145.9 dB	144.1 dB	144.7 dB
OSR = 8	SNR	66.9 dB	66.8 dB	59.9 dB
	ENOB	10.8 bits	10.8 bits	9.7 bits
	[a] FOM (pJ/conv)	12.6	14.4	26.9
	[b] FOMs	143.4 dB	142.7 dB	136.4 dB

[a] FOM = P/2^ENOB/f, where P and f are the power consumption and the sampling frequency of the ADC. ENOB is the effective number of bits = (SNR−1.73)/6.02. [b] FOMs = SNDR + $10\log_{10}$(f/P).

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Conflicts of Interest: The authors declare no conflict of interest.

References

1. Available online: https://www.ti.com/lit/ds/symlink/pcm1820-q1.pdf?ts=1682840802224&ref_url=https%253A%252F%252Fwww.ti.com%252Faudio-ic%252Fconverters%252Fadc%252Fproducts.html (accessed on 1 June 2023).
2. Fredenburg, A.; Flynn, M.P. A 90-MS/s 11-MHz-Bandwidth 62-dB SNDR Noise-Shaping SAR ADC. *IEEE J. Solid-State Circuits* **2012**, *47*, 2898–2904. [CrossRef]
3. Guo, W.; Sun, N. A 12b-ENOB 61μW noise-shaping SAR ADC with a passive integrator. In Proceedings of the ESSCIRC Conference 2016: 42nd European Solid-State Circuits Conference, Lausanne, Switzerland, 12–15 September 2016; pp. 405–408.
4. Liu, C.; Huang, M. A 0.46mW 5MHz-BW 79.7dB-SNDR noise-shaping SAR ADC with dynamic-amplifier-based FIR-IIR filter. In Proceedings of the 2017 IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, USA, 5–9 February 2017; pp. 466–467. [CrossRef]
5. Chen, Z.; Miyahara, M.; Matsuzawa, A. A 9.35-ENOB, 14.8 fJ/conv.-step fully-passive noise-shaping SAR ADC. In Proceedings of the 2015 Symposium on VLSI Circuits (VLSI Circuits), Kyoto, Japan, 17–19 June 2015; pp. C64–C65.
6. Zhang, Q.; Ning, N.; Li, J.; Yu, Q.; Wu, K.; Zhang, Z. A Second-Order Noise-Shaping SAR ADC Using Two Passive Integrators Separated by the Comparator. *IEEE Trans. Very Large Scale Integr. Syst.* **2020**, *29*, 227–231. [CrossRef]
7. Baird, R.; Fiez, T. Linearity enhancement of multibit ΔΣ A/D and D/A converters using data weighted averaging. *IEEE Trans. Circuits Syst. II Analog. Digit. Signal Process* **1995**, *42*, 753–762. [CrossRef]
8. Jie, L.; Tang, X.; Liu, J.; Shen, L.; Li, S.; Sun, N.; Flynn, M.P. An Overview of Noise-Shaping SAR ADC: From Fundamentals to the Frontier. *IEEE Open J. Solid State Circuits* **2021**, *1*, 149–161. [CrossRef]
9. Shu, Y.; Kuo, L.-T.; Lo, T.-Y. An oversampling SAR ADC with DAC mismatch error shaping achieving 105 dB SFDR and 101 dB SNDR Over 1 kHz BW in 55 nm CMOS. *IEEE J. Solid State Circuits* **2016**, *51*, 2928–2940. [CrossRef]
10. Liu, J.; Wang, X.; Gao, Z.; Zhan, M.; Tang, X.; Sun, N. A 40kHz-BW 90dB-SNDR noise-shaping SAR with 4× passive gain and 2nd-order mismatch error shaping. In Proceedings of the 2020 IEEE International Solid-State Circuits Conference-(ISSCC), San Francisco, CA, USA, 16–20 February 2020; pp. 158–160.
11. Sun, N. High-Order Mismatch-Shaping in Multibit DACs. *IEEE Trans. Circuits Syst. II Express Briefs* **2011**, *58*, 346–350. [CrossRef]
12. Liu, J.; Hsu, C.; Tang, X.; Li, S.; Wen, G.; Sun, N. Error-feedback mismatch error shaping for high-resolution data converters. *IEEE Trans. Circuits Syst. I Reg. Pap.* **2019**, *66*, 1342–1354. [CrossRef]
13. Obata, K.; Matsukawa, K.; Miki, T.; Tsukamoto, Y.; Sushihara, K. A 97.99 dB SNDR, 2 kHz BW, 37.1 μW noise-shaping SAR ADC with dynamic element matching and modulation dither effect. In Proceedings of the 2016 IEEE Symposium on VLSI Circuits (VLSI-Circuits), Honolulu, HI, USA, 15–17 June 2016; pp. 1–2.
14. Chan, K.L.; Rakuljic, N.; Galton, I. Segmented dynamic element matching for high-resolution digital-to-analog conversion. *IEEE Trans. Circuits Syst. I Reg. Pap.* **2008**, *55*, 3383–3392. [CrossRef]
15. Salib, A.; Flanagan, M.F.; Cardiff, B. Blind SAR ADC capacitor mismatch calibration. In Proceedings of the 2017 IEEE 60th International Midwest Symposium on Circuits and Systems (MWSCAS), Boston, MA, USA, 6–9 August 2017; pp. 587–590.
16. Guo, W.; Zhuang, H.; Sun, N. A 13b-ENOB 173dB-FoM 2ndorder NS SAR ADC with passive integrators. In Proceedings of the 2017 Symposium on VLSI Circuits, Kyoto, Japan, 5–8 June 2017; pp. C236–C237.
17. Zhuang, H.; Guo, W.; Liu, J.; Tang, H.; Zhu, Z.; Chen, L.; Sun, N. A Second-Order Noise-Shaping SAR ADC With Passive Integrator and Tri-Level Voting. *IEEE J. Solid State Circuits* **2019**, *54*, 1636–1647. [CrossRef]
18. Liu, J.; Wen, G.; Sun, N. Second-order DAC MES for SAR ADCs. *Electron. Lett.* **2017**, *53*, 1570–1572. [CrossRef]
19. Carusone, T.C.; Johns, D.A.; Martin, K.W. *Analog Integrated Circuit Design*; Wiley: Hoboken, NJ, USA, 2012.