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Analysis and Suppression of Rectifier Diode Voltage Oscillation Mechanism in IPOS High-Power PSFB Converters

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Abstract: Parasitic oscillations in the rectifier diode voltage of phase-shifted-full-bridge (PSFB) converters limit their application in high-voltage and high-power situations. The conventional analysis method for parasitic oscillation in rectifier diode voltage in PSFB converters treats the filter inductor as a constant current source and fails to consider the impact of changes in filter inductor current on the rectifier diode's parasitic oscillation. Consequently, this approach does not apply when analyzing the rectifier diode voltage's parasitic oscillations in high-power PSFB converters employing an input-parallel output-series (IPOS) configuration with interleaved drive. This research paper introduces an innovative equivalent circuit model for analyzing the parasitic oscillations of rectifier diode voltage in IPOS high-power PSFB converters. The model takes into account the mutual influence of rectifier diode voltage oscillations between submodules under interleaved control, considering the influence of changes in filter inductor current on rectifier diode parasitic oscillation. Based on the circuit model, we explain the mechanism of multiple oscillations of the rectifier diode voltage and the reason for the high peak of the first oscillation. Consequently, the interplay of rectifier diode voltage oscillations in IPOS high-power k-module PSFB converters under interleaved control is analyzed. To mitigate the adverse effects of rectifier diode voltage parasitic oscillation, a buffering strategy involving the connection of a resistor capacitor diode (RCD) circuit in parallel after the rectifier bridge is adopted, considering the structure of the IPOS high-power PSFB converter. The study provides a detailed analysis of the circuit's operation mechanism upon incorporating the RCD buffer circuit and establishes the relationship between buffer capacitance, resistance, and spike voltage. Furthermore, a design method for buffer capacitors and discharge resistors in buffer circuits is presented. Finally, a 100 kW prototype is tested to verify the rectifier diode voltage oscillation mechanism of the IPOS high-power PSFB converter and the rationality of the buffer capacitor and discharge resistor design method under the interleaved drive approach.

Keywords: input-parallel output-series (IPOS); phase-shifted full-bridge (PSFB); interleaved drive; parasitic oscillations; RCD buffer circuit

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1. Introduction

In light of the escalating depletion of fossil energy resources and the escalating concern regarding global warming, the production of clean energy from sources such as wind and solar power has gained considerable attention [1]. As an important link in the conversion of electrical energy, the reliability, efficiency, and power density of DC converters play a key role in the efficient use of clean energy [2]. Zero-voltage switching (ZVS) PSFB converters are the most commonly used topologies in the medium-to-high-power range [3–5]. The main attractive features compared to resonant converters [6–8] are the ZVS switching of the primary switching transistor, the constant switching frequency, and the simplicity of the control [9]. Nevertheless, the conventional PSFB ZVS pulse-width modulated (PWM)

converters have severe parasitic oscillations and high spike voltages on the output rectifier diode due to the filter inductor decoupling the rectifier stage from the capacitor stage, making the junction capacitor of the rectifier diode a passive buffer. Consequently, the rectifier diode will be subjected to high voltage and current stresses, which become particularly severe in medium and high voltage, high power applications [10].

The suppression of the rectifier diode spike voltage of the PSFB converter determines the success or failure of the entire converter design in high-voltage and high-power applications. The operating conditions of the switching transistors and rectifier diodes would be very harsh if only a single PSFB converter module was used. The DC/DC converter structure with multiple modules interleaved in parallel solves this problem well. By connecting the modules in series or parallel to the input terminal, voltage and current equalization between individual modules can be achieved, respectively. Moreover, the combination of serial and parallel connections to the output terminal allows for higher output voltages and higher output currents, respectively, and each connection method has its own characteristics, application areas, and advantages [11]. In addition, using redundant modules can improve the reliability of the modular conversion system [12]. The high boost ratio and high conversion efficiency of IPOS structures make them widely used in energy storage, renewable energy generation, and high-voltage pulse generators [13,14].

Many scholars have proposed many methods to suppress the problem of rectifier diode spike voltage in conventional PSFB converters. The literature [15] analyzed in detail the mechanism of rectifier diode spike voltage generation in a conventional phase-shifted full-bridge converter and proposed a basic method to suppress rectifier diode voltage oscillations. In the literature [16,17], the parasitic oscillation of the rectifier diode is well suppressed by adding a resonant inductor and clamp diode to the primary side and changing the driving mode of the switching transistor appropriately. However, by adding a clamp diode to the inverter bridge arm, only the additional inductance and rectifier diode junction capacitance oscillations can be suppressed. In contrast, the leakage inductance of the high-power, high-frequency transformer is difficult to reduce. The literature [18] regulates the effective energy of ZVS by introducing a triple-winding coupled inductor in the inverter bridge arm, thus reducing the need for an output filter inductor and the parasitic oscillation of the rectifier diode. However, the design of the triple-winding coupled inductor is complicated, and the loss of the triple-winding coupled inductor is high in high-power and high-voltage ratio applications. The analysis method of the rectifier diode voltage oscillation mechanism of the traditional PSFB converter is not applicable to the IPOS high-power PSFB converter under interleaved control, and the parasitic oscillations in the rectifier diode voltage of the IPOS high-power PSFB converter under interleaved control are more complex, making these solutions more difficult to implement in this converter.

This paper presents a novel approach to developing an equivalent circuit model for analyzing the parasitic oscillation of rectifier diode voltage in an IPOS high-power PSFB (phase-shifted full-bridge) converter with interleaved drive. The study takes into account the impact of changes in filter inductor current on the parasitic oscillation of the rectifier diode and aims to enhance the accuracy of the corresponding model. It is analyzed in detail to determine the mutual effect of rectifier diode voltage oscillation between submodules of an IPOS converter composed of two PSFB submodules under interleaved drive. The paper elucidates the mechanism behind the three oscillations of the rectifier diode voltage and provides an explanation for the high peak observed in the first oscillation. Furthermore, it proposes an oscillation mechanism for the rectifier diode voltage in the IPOS high-power k-module PSFB converter under interleaved control. To suppress the adverse effects of the parasitic oscillations of the rectifier diode voltage, the buffering strategy of shunt RCD after the rectifier bridge is chosen in conjunction with the structure of the IPOS high-power PSFB converter. Analyzing the relationship between buffer capacitor and discharge resistor with spike voltage and proposing the design method of buffer capacitor and discharge resistor. The correctness of the voltage oscillation mechanism of the rectifier diode of the

IPOS high-power PSFB converter and the rationality of the design method of the buffer capacitor and discharge resistor in the buffer circuit is verified through experiments.

The paper is organized according to the following structure: In Section 2, the equivalent circuit of the parasitic oscillation of rectifier diode voltage in the IPOS high-power PSFB converter is established. The mechanism of the parasitic oscillation of rectifier diode voltage under interleaved control is analyzed in detail. Additionally, it also presents the mechanism of n + 1 oscillations of the rectifier diode voltage in the IPOS high-power PSFB converter, which is based on n sub-modules. Section 3 describes the operation of the buffer capacitor after adding the RCD buffer circuit to a single submodule in the IPOS high-power PSFB converter and gives the design method of RC. In Section 4, a 100 kW hardware converter prototype is designed, manufactured, and tested to verify the correctness of the rectifier diode voltage oscillation mechanism and the rationality of the RC design method for the buffer circuit. Finally, conclusions are given in Section 5.

2. Mechanism of Rectifier Diode Voltage Oscillation

The conventional PSFB converter considers the junction capacitance of the rectifier diode to simulate the reverse recovery of the rectifier diode, and its main circuit is shown in Figure 1. S_1~S_4 are the four switching transistors of the primary inverter H-bridge. If the driving signals of S_1 and S_3 are ahead of S_2 and S_4, respectively, the bridge arms in which S_1 and S_3 are located are said to be ahead of the bridge arms, and the bridge arms in which S_2 and S_4 are located are said to be lagging bridge arms. D_{S1}~D_{S4} and C_1~C_4 are the switching transistor's internal anti-parallel diodes and the junction capacitance, respectively. v_{AB} is the output square wave AC voltage of the inverter bridge arm, and L_r is the resonant inductor of the primary side. The ZVS of the switching transistor is achieved by using the resonant inductor of the primary side (or transformer leakage) and the junction capacitance of the switching transistor to resonate [19–21]. T_r for high-frequency transformer primary and secondary turns ratio is 1:n, * is the eponymous end of the transformer, i_p for transformer primary current, and C_b is the isolation capacitor to prevent DC bias of the high-frequency transformer. D_1~D_4 are the secondary rectifier diodes; $C_{j1} \sim C_{j4}$ are the junction capacitors of the rectifier diodes; V_{rect} is the rectified H-bridge output voltage; L_f and C_f are the filter inductor and filter capacitor, respectively; i_{Lf} is the current flowing through the filter inductor; V_{in} and C_{in} are the input voltage and input filter capacitor, respectively; R_L and V_o are the load resistance and output voltage, respectively.

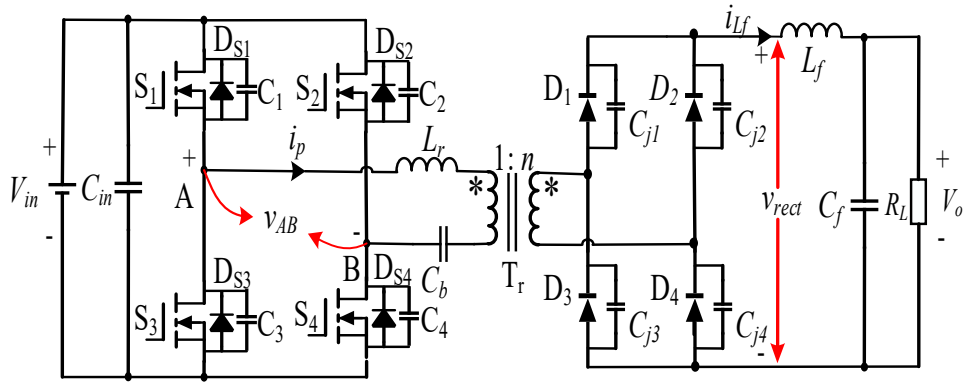


Figure 1. The main circuit of the PSFB converter.

When considering the junction capacitance of the rectifier diode, the resonance of the primary resonant inductor with the diode junction capacitance during the switching transistor hysteresis bridge arm commutation subjects the diode to a very high spike voltage. The resonant energy comes from the imbalance between the primary resonant inductor and

the filter inductor current. The maximum values of the transformer primary-side current and rectifier diode voltage, $i_{pmax}(t)$ and $v_{Cj23max}(t)$, are, respectively [15]:

$$i_{pmax}(t) = ni_{Lf}(t) + V_{in}\sqrt{\frac{C_{j23}}{L_r}} \tag{1}$$

$$v_{Cj23max}(t) = 2nV_{in} \tag{2}$$

C_{j23} is the parallel equivalent capacitance of the diagonal diode parasitic capacitance C_{j2} and C_{j3} of the rectifier bridge, and v_{cj23} is the voltage across the parallel equivalent capacitance. Combined with Equation (2), if the resonant inductor and filter inductor are respectively equivalent to a current source, the components of the primary side of the transformer are converted to the secondary side to further simplify the equivalent circuit, as shown in Figure 2. The essence of the resonant inductor and diode junction capacitance resonance generating diode spike voltage is the current imbalance between the primary equivalent current source of the transformer and the secondary equivalent current source of the transformer. That is, the current of the primary equivalent current source is greater than that of the secondary equivalent current source. This excess current charges the capacitance at the commutation point between the secondary and diode, leading to oscillation in the primary resonant inductor and rectifier diode junction capacitance.

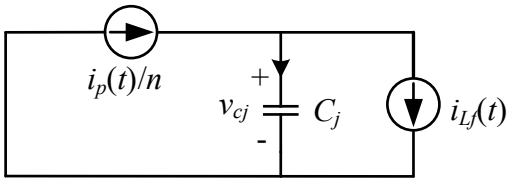


Figure 2. Simplifying equivalent circuits.

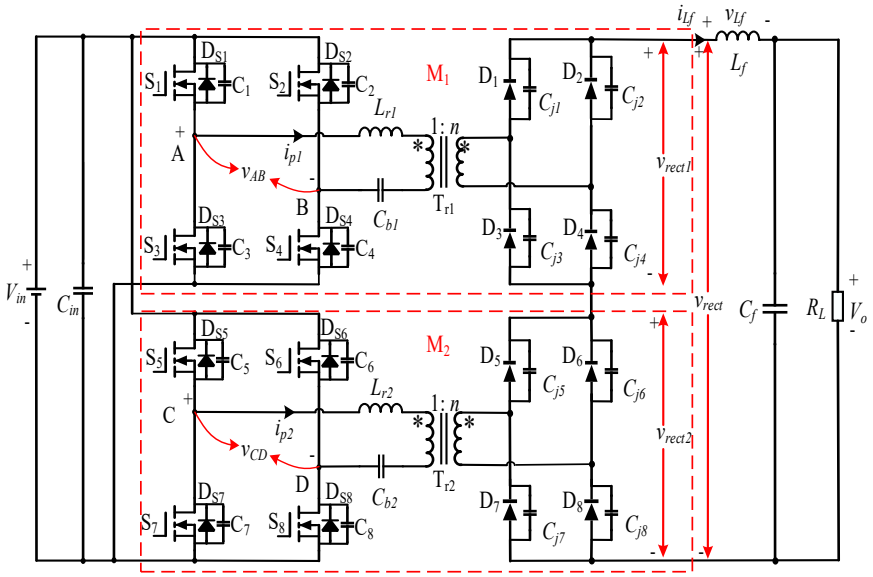
The IPOS high-power PSFB converter module is composed of multiple PSFB converter submodules connected in series after rectification at the output side in parallel with the input side [22]. Taking an IPOS high-power PSFB converter composed of two submodules as an example, the main circuit shown in Figure 3a takes into account the rectifier diode junction capacitance. L_{r1} and L_{r2}, C_{b1} and C_{b2}, i_{p1} and i_{p2}, V_{rect1} and V_{rect2}, and T_{r1} and T_{r2} are the resonant inductors (or transformer leakage), bulkhead capacitors, primary side currents, rectified output voltages, and transformers of submodules M_1 and M_2, respectively. V_{in}, C_{in}, V_{rect}, L_f, C_f, i_{Lf}, R_L, and V_o are the input voltage, input capacitance, rectified output voltage, filter inductor, filter capacitor, current flowing through the filter inductor, load equivalent resistance, and output voltage of the IPOS high-power PSFB converter module (hereinafter referred to as the module), respectively.

Defining the primary duty cycle D as the ratio of the overlap time of diagonal switching transistors to the switching period within one switching cycle. When neglecting all resonant modes and considering the PSFB converter as an isolated buck converter, its effective duty cycle D_{eff} on the secondary side is [23]:

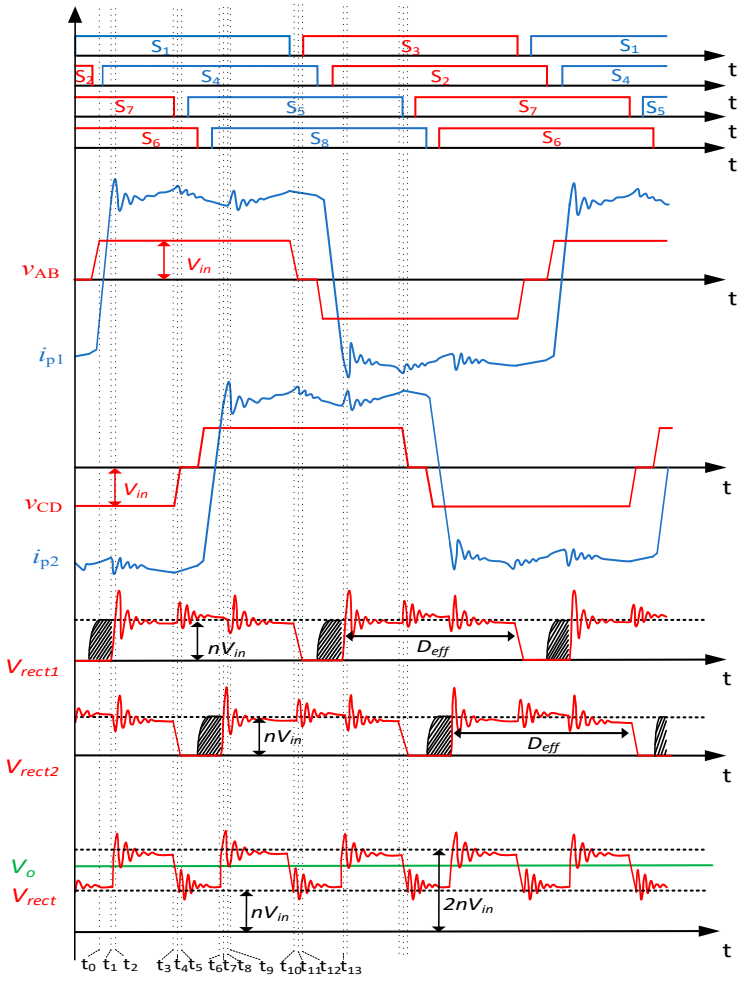
$$D_{eff} = \frac{V_o}{2nV_{in}} \tag{3}$$

Typically, to achieve greater power transfer and higher boost ratios, IPOS high-power PSFB converters are designed for stable operation with an effective duty cycle of $D_{eff} > 0.5$ on the secondary side. For reducing the input and output voltage and current ripple, interlaced driving is usually used between submodules. Figure 3b shows the main waveforms of the IPOS high-power PSFB converter for $D_{eff} > 0.5$ under interleaved drive. Since two rectifier H-bridges of this converter share a set of output LC filter networks, the interleaved driving mode makes the voltage oscillation process of the rectifier diode more complicated, and the parasitic oscillation of the rectifier diode of the IPOS high-power PSFB converter

will be more serious compared with the adverse effect brought by the parasitic oscillation of the rectifier diode of a traditional PSFB converter.



(**a**) Main circuit diagram



(**b**) Main waveform diagram

Figure 3. Main circuit and main waveform considering rectifier diode junction capacitance.

When the circuit is operating in a steady state, take submodule M_1 as an example to analyze the effect of submodule M_2 rectifier diode commutation on submodule M_1 rectifier diode voltage oscillation under interleaved control. The following assumptions are made for the convenience of the analysis [24,25]:

(1) The output voltage V_o is constant with a large filter capacitor, and $V_{rect1} < V_o$, $V_{rect2} < V_o$, $nV_{in} < V_o$, $2nV_{in} > V_o$, and $V_{rect1} + V_{rect2} > V_o$ when the circuit is operating in a steady state and both V_{rect1} and V_{rect2} are non-zero, as shown in Figure 3b;
(2) the resonant inductance of the primary side of submodules M_1 and M_2 is equal, and the junction capacitance of all rectifier diodes is equal, i.e., $L_{r1} = L_{r2} = L_r$, $C_{j1} = C_{j2} = \ldots = C_{j8}$;
(3) compared to the resonant inductance, the filter inductance is much larger, i.e., $L_f >> L_r$.

2.1. First Oscillation of Rectifier Diode Voltage

Before the moment t_1 in Figure 3b, the switching transistors S_6 and S_7 and rectifier diodes D_6 and D_7 of submodule M_2 are in conduction, and the rectifier output voltage is V_{rect2}. The switching transistors S_1 and S_4 of submodule M_1 are in the conduction state, and since their primary current is less than the converted value of the secondary current, the secondary rectifier diodes are all on to renew the current. The rectifier output voltage of submodule M_1 $V_{rect1} = 0$. All input voltage is added to the resonant inductor L_{r1}, resulting in a linearly increasing primary current. At this time, only submodule M_2 supplies power to the load; the module rectification output voltage $V_{rect} = V_{rect2}$. The current value i_{Lf} flows through the filter inductor as:

$$i_{Lf}(t) = i_{Lf}(t_0) + \frac{nV_{in} - V_o}{n^2 L_{r2} + L_f}(t - t_0) \tag{4}$$

In Equation (4), the filter inductor current decreases linearly before t_1. The primary side current of submodule M_2 is the same as the converted value for the secondary side current, which decreases linearly as well. At the moment t_1, the primary current of submodule M_1 increases to a converted value equal to the secondary current. The resonant inductor L_{r1} resonates with the junction capacitors C_{j2} and C_{j3} of rectifier diodes D_2 and D_3, charging the junction capacitors C_{j2} and C_{j3}. The rectified output voltage of submodule M_1 is equal to the voltage of junction capacitors C_{j2} and C_{j3}, and the primary side current i_{p1} of submodule M_1 before V_{rect1} rises to $V_o - V_{rect2}$, i.e., before the t_2 moment, is:

$$i_{p1}(t) = i_{p1}(t_1) + \frac{V_{in} - V_{rect1}/n}{L_{r1}}(t - t_1) \tag{5}$$

The filter inductor current i_{Lf} is:

$$i_{Lf}(t) = i_{Lf}(t_1) + \frac{V_{rect} - V_o}{L_f}(t - t_1) \tag{6}$$

In Equations (5) and (6), the primary side current of submodule M_1 is increasing and the filter inductor current is decreasing in the period [t_1–t_2]. Nevertheless, the primary current of the submodule M_1 is already equal to the converted value of the filter inductor current at the moment t_1. This causes an imbalance in the primary and secondary currents of submodule M_1, making the primary current greater than the converted value of the secondary current and generating the first oscillation of the rectifier diode D_2 and D_3 voltages. At this stage, the primary current comprises two components: one corresponds to the filter inductor current converted to the secondary side, and the other component represents the resonant current resulting from the resonant operation between the resonant inductor and the junction capacitor.

The components on the primary side of the transformer are equated to the secondary side to analyze the interaction of the rectified output voltage between the IPOS high-power

PSFB converter modules. Since the output filter capacitor is large, the output filter capacitor and load branch are replaced with a constant voltage source V_o for simplicity of analysis. The equivalent circuit for the [t_1–t_3] period is drawn in Figure 4.

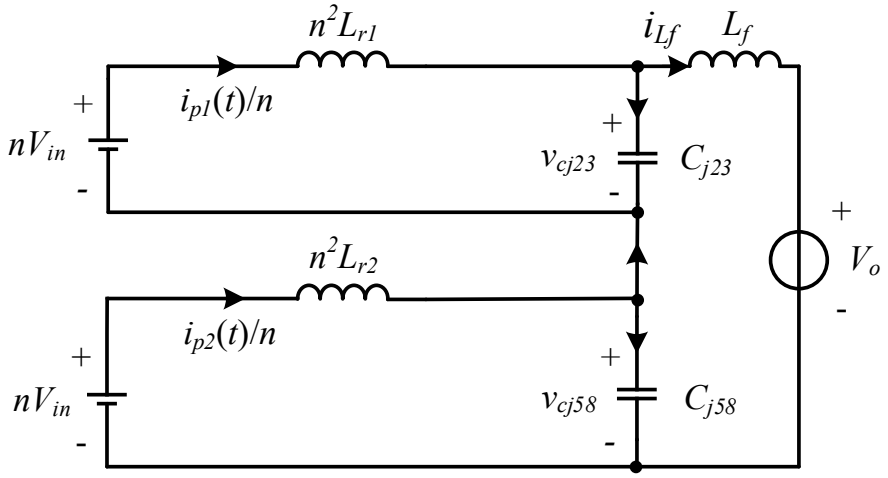


Figure 4. Equivalent circuit for the [t_1–t_3] period.

In Figure 4, nV_{in} is the equivalent value of the input supply voltage converted to the secondary side; i_{p1}/n, i_{p2}/n and n^2L_{r1} and n^2L_{r2} are the equivalent values of the primary side current and resonant inductance of submodules M_1 and M_2 converted to the secondary side. The capacitances C_{j23} and C_{j58} are the equivalent capacitances of rectifier diode junction capacitor C_{j2} in parallel with C_{j3} and the equivalent capacitances of C_{j5} and C_{j8} in parallel, respectively. The differential equation of Figure 4 is written and substituted into the initial conditions to solve the expressions of i_{p1} and v_{cj23} for the period [t_1–t_2] as:

$$i_{p1}(t) = ni_{Lf}(t-t_1) + nV_{in}\sqrt{\frac{C_{j23}}{n^2L_{r1}}}\sin\omega_1\frac{(t-t_1)}{\sqrt{C_{j23}n^2L_{r1}}} + \frac{V_o - nV_{in}}{n^2L_{r2}+L_f}(t-t_1) \tag{7}$$

$$v_{cj23}(t) = \frac{n^2L_{r2}+L_f}{n^2(L_{r2}+L_{r1})+L_f}nV_{in}\left[1-\cos\frac{(t-t_1)}{\sqrt{n^2L_{r1}C_{j23}}}\right] + \frac{n^2L_{r1}}{n^2(L_{r1}+L_{r2})+L_f}\left[V_o - nV_{in} + \frac{n^2L_{r1}(V_o-nV_{in})}{n^2(L_{r1}+L_{r2})+L_f}\cos\omega_2\frac{(t-t_1)}{\sqrt{n^2L_{r2}C_{j58}}}\right] \tag{8}$$

The first oscillation of the rectifier diode causes the rectified output voltage of submodule M_2 to transition from $V_{rect2} > nV_{in}$ to $V_{rect2} < nV_{in}$ after moment t_1. The primary side current i_{p2} of submodule M_2 transitions from a linear decrease before moment t_1 to a linear increase after moment t_1 in line with the filter inductor current i_{Lf}.

2.2. Second Oscillation of Rectifier Diode Voltage

Before the moment t_3 in Figure 3b, the switching transistors S_1 and S_4 and rectifier diodes D_1 and D_4 of submodule M_1 are in conduction, and the rectifier output voltage is V_{rect1}. The switching transistors S_6 and S_7 and rectifier diodes D_6 and D_7 of submodule M_2 are also in conduction, and the rectified output voltage is V_{rect2}. The rectified output voltages of submodules M_1 and M_2 are constant together to supply the load. The rectified output voltage of the module is $V_{rect} = V_{rect1} + V_{rect2}$, and the current value i_{Lf} flowing through the filter inductor is:

$$i_{Lf}(t) = i_{Lf}(t_3) + \frac{2nV_{in} - V_o}{2n^2(L_{r1}+L_{r2})+L_f}(t-t_3) \tag{9}$$

In Equation (9), the filter inductor current increases linearly before the t_3 moment, and the primary side currents of submodules M_1 and M_2 are equal to the converted value of the filter inductor current, which also increases linearly. At the moment t_3, the switching

transistor S_7 turns off, and the rectified output voltage of submodule M_2 starts to drop. When the rectified output voltage of submodule M_2 drops to $V_{rect2} < V_o - V_{rect1}$, i.e., at moment t_4, the filter inductor current i_{Lf} is:

$$i_{Lf}(t) = i_{Lf}(t_3) + \frac{V_{rect} - V_o}{L_f}(t - t_4) \tag{10}$$

In Equation (10), the filter inductor current starts to decrease linearly after moment t_4, while the primary side current i_{p1} of submodule M_1 keeps increasing linearly in line with that before moment t_3. This causes an imbalance in the primary and secondary currents of submodule M_1, making the primary current of submodule M_1 greater than the converted value of the secondary current. A second oscillation of the rectifier diode D_2 and D_3 voltages is generated. The second oscillation of the rectifier diode voltage causes the rectifier output voltage of submodule M_1 to transition from $V_{rect1} < nV_{in}$ to $V_{rect1} > nV_{in}$ after moment t_4, and the primary side current i_{p1} of submodule M_1 is:

$$i_{p1}(t) = i_{p1}(t_4) + (\frac{n(nV_{in} - V_o)}{n^2L_{r1} + L_f})(t - t_4) \tag{11}$$

This means that the second oscillation causes the average value of the rectified output voltage of submodule M_1 to increase, so that the primary current i_{p1} of submodule M_1 decreases linearly with the same filter inductor current i_{Lf}. Similar to the analysis in Section 2.1, its equivalent circuit in the period $[t_3–t_5]$ is shown in Figure 5.

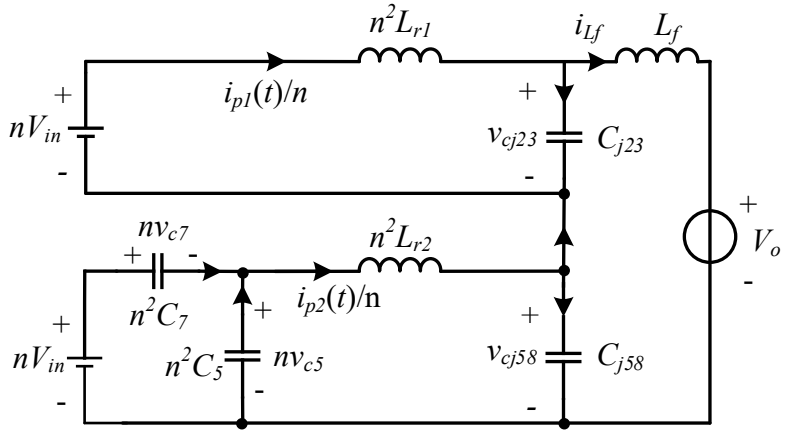


Figure 5. Equivalent circuit for the $[t_3–t_5]$ period.

When the switching transistor S_7 is turned off, it is considered that the rectifier output voltage V_{rect2} of submodule M_2 decreases linearly, and the expressions i_{p1} and v_{cj23} can be obtained as:

$$i_{p1} = ni_{Lf}(t - t_3) + \frac{n^2L_{r1}(2nV_{in} - V_o)}{\left[2n^2(L_{r1} + L_{r2}) + L_f\right]}\sqrt{\frac{C_{j23}}{n^2L_{r1}}}\sin\omega_1(t - t_3) \tag{12}$$

$$v_{cj23} = \frac{n^2L_{r2} + L_f}{n^2(L_{r1} + L_{r2}) + L_f}\left[nV_{in} + \frac{n^2L_{r1}(V_o - 2nV_{in})}{n^2(L_{r1} + L_{r2}) + L_f}\cos\frac{(t - t_3)}{\sqrt{n^2L_{r1}C_{j23}}}\right] + \frac{n^2L_{r1}}{n^2(L_{r1} + L_{r2}) + L_f}\left[V_o - \left(nV_{in} - \frac{i_{Lf}(t - t_3)}{C_{j58} + 2n^2C_5}\right)\right] \tag{13}$$

2.3. Third Oscillation of Rectifier Diode Voltage

Before the moment t_6 in Figure 3b, the switching transistors S_1 and S_4 and rectifier diodes D_1 and D_4 of submodule M_1 are in the conduction state, and the rectifier output voltage is V_{rect1}. The switching transistors S_5 and S_8 of submodule M_2 are in conduction, but since their primary current is less than the converted value of the secondary current, the

secondary rectifier diodes are all on to renew the current, and the rectifier output voltage of submodule M_2 is $V_{rect2} = 0$. The input voltage is all added to the resonant inductor L_{r2}, and the primary current increases linearly. At this time, only the submodule M_1 supplies power to the load; the module rectification output voltage $V_{rect} = V_{rect1}$, and the current value i_{Lf} flowing through the filter inductor is:

$$i_{Lf}(t) = i_{Lf}(t_6) + \frac{nV_{in} - V_o}{n^2 L_{r1} + L_f}(t - t_6) \tag{14}$$

In Equation (14), the filter inductor current decreases linearly before the moment t_6, and the primary side current of submodule M_1 is equal to the converted value of the filter inductor current, which also decreases linearly. At the moment t_6, the primary current of submodule M_2 increases to a value equal to the converted value of the secondary current, at which time the resonant inductor L_{r2} resonates with the junction capacitors C_{j6} and C_{j7} of rectifier diodes D_6 and D_7, charging the junction capacitors of the diodes. The diode voltage starts to rise, and the rectified output voltage of submodule M_2 is equal to the voltage of junction capacitors C_{j6} and C_{j7}, which also starts to rise. When V_{rect2} rises to $V_{rect2} > V_o - V_{rect1}$, i.e., at the moment t_7. The current i_{Lf} of the filter inductor is:

$$i_{Lf}(t) = i_{Lf}(t_7) + \frac{V_{rect} - V_o}{L_f}(t - t_7) \tag{15}$$

In Equation (15), the filter inductor current starts to increase after moment t_7, while the primary current i_{p1} of submodule M_1 keeps decreasing linearly in line with that before moment t_6, making the primary current of submodule M_1 smaller than the converted value of the secondary current and transformer T_{r1} lose carrying capacity. The rectifier diode junction capacitors C_{j2} and C_{j3} of submodule M_1 start to discharge, the rectifier output voltage V_{rect1} starts to decrease, and the transformer primary side voltage also starts to decrease. At the moment t_8, the transformer's primary voltage is less than the input voltage. At this time, the primary current i_{p1} of submodule M_1 is:

$$i_{p1}(t) = i_{p1}(t_8) + \frac{V_{in} - V_{rect1}/n}{L_r}(t - t_8) \tag{16}$$

In Equation (16), the primary current i_{p1} of submodule M_1 starts to increase after t_8 moments. Due to the small resonant inductance, the primary current rises rapidly. The primary current of submodule M_1 rises to a converted value equal to the secondary current at t_9 moments, and transformer T_{r1} recovers its carrying capacity. Since the junction capacitors C_{j2} and C_{j3} of the rectifier diode have been discharged during the [t_7–t_9] period, the primary and secondary windings of transformer T_{r1} lose contact, so there is a loss of duty cycle during the [t_7–t_9] period. The primary current of submodule M_1 is equal to the converted value of the secondary current at t_9, but the primary current of submodule M_1 still rises rapidly because the discharge of the junction capacitors C_{j2} and C_{j3} of the rectifier diode makes V_{rect1} less than nV_{in}. Thus, there is an imbalance of the primary and secondary currents of submodule M_1, which makes the primary current of submodule M_1 larger than the converted value of the secondary current, resulting in the third oscillation. The third oscillation of the rectifier diode causes the rectified output voltage of submodule M_1 to transition from $V_{rect1} > nV_{in}$ to $V_{rect1} < nV_{in}$ after moment t_9. The primary side current i_{p1} of submodule M_1 is:

$$i_{p1}(t) = i_{p1}(t_9) + \frac{n(2nV_{in} - V_o)}{2n^2(L_{r1} + L_{r2}) + L_f}(t - t_9) \tag{17}$$

The third oscillation causes the average value of the rectified output voltage of sub-module M_1 to decrease. The transformer primary voltage of sub-module M_1 is less than the input voltage V_{in}, which makes the primary current i_{p1} of sub-module M_1 rise linearly

and the filter inductor current i_{Lf} remain the same. Similar to the equivalent in Section 2.1, its equivalent circuit for the period [t_6–t_{10}] is shown in Figure 6.

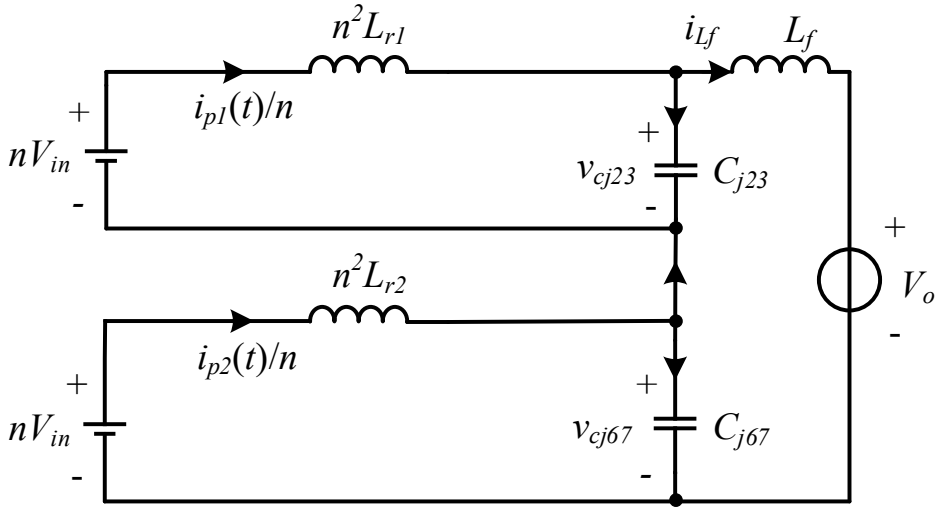


Figure 6. Equivalent circuit for the [t_6–t_{10}] period.

From Figures 4 and 6, it can be seen that the equivalent circuit structure of the third oscillation and the first oscillation of the rectifier diode D_2 or D_3 voltage are the same. This is because submodules M_1 and M_2 are symmetrical, and the first oscillation occurs in the rectifier bridge arm commutation of submodule M_1, while the third oscillation occurs in the rectifier bridge arm commutation of submodule M_2. Since the submodules M_1 and M_2 operate symmetrically, their equivalent circuits are the same. Similarly, in the period [t_6–t_{10}] from Figure 6, we can obtain i_{p1} and v_{cj23} as:

$$i_{p1} = ni_{Lf}(t - t_6) + \frac{n^2L_{r1}(nV_{in} - V_o)}{(n^2L_{r1} + L_f)}\sqrt{\frac{C_{j23}}{n^2L_{r1}}}\sin\omega_1\frac{(t - t_6)}{\sqrt{n^2L_{r1}C_{j23}}} \tag{18}$$

$$v_{cj23} = \frac{L_{r2} + L_f}{L_{r1} + L_{r2} + L_f}\left[nV_{in} + \frac{n^2L_{r1}(V_o - nV_{in})}{n^2L_{r1} + L_f}\cos\omega_1\frac{(t - t_6)}{\sqrt{n^2L_{r1}C_{j23}}}\right] + \frac{L_{r1}}{L_{r1} + L_{r2} + L_f}\left[V_o - nV_{in}(1 - \cos\omega_2\frac{(t - t_6)}{n^2L_{r2}C_{j67}})\right] \tag{19}$$

2.4. $k + 1$ *Oscillations of k PSFB Submodules*

To achieve higher power transfer and a higher step-up ratio, more PSFB converter submodules are required to be connected by IPOS. As shown in Figure 7 for a k-submodule IPOS high-power PSFB converter. For an IPOS converter consisting of k PSFB converter submodules with the interleaved drive between the submodules, the phase difference of the drive pulses between every two submodules should be $2\pi/k$. Since the frequency of the rectified output voltage of the PSFB converter is twice the switching frequency, the phase difference between adjacent modules in an IPOS converter composed of k PSFB converters should be π/k.

From the analysis in Sections 2.1–2.3, it is clear that for an IPOS converter consisting of two PSFB converter submodules, when the drive is interleaved between modules, the voltage of any rectifier diode in the module oscillates three times when the effective duty cycle of the secondary side $D_{eff} > 0.5$. The first oscillation is mainly caused by the rectifier diode commutation of submodule M_1 itself; the second oscillation is mainly caused by the rectifier diode renewal of submodule M_2; and the third oscillation is mainly caused by the rectifier diode commutation of submodule M_2. It follows that for an IPOS system consisting of k sub-modules, when interleaved driving is used between the sub-modules, the voltage of any rectifier diode in the module oscillates $k + 1$ times at $D_{eff} > 1/k$.

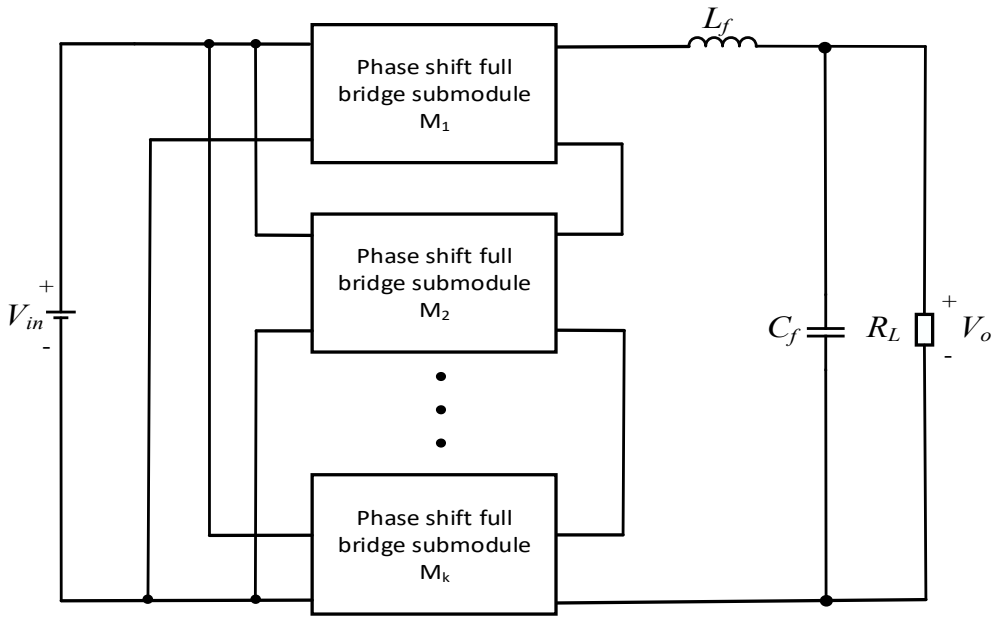


Figure 7. IPOS converter with k PSFB converter submodules.

3. Suppression Technique of Rectifier Diode Spike Voltage

The effective suppression of rectifier diode spike voltage plays a crucial role in the design of high-power, medium-voltage, and high-voltage applications utilizing the PSFB converter. For the IPOS high-power PSFB converter under interleaved drive, the voltage of the rectifier diode oscillates three times when it operates at $D_{eff} > 0.5$. If an active embedding strategy is used to suppress the rectifier diode spike voltage, the control circuit design will be very complicated. Considering the reliability of the system, the most efficient way to suppress the rectifier diode spike voltage in IPOS high-power PSFB converters is to connect an RCD buffer circuit in parallel behind the rectifier bridge.

3.1. Design of RCD Buffer Circuit

From Equations (7), (12), and (18), the three extreme values of the primary side current i_{p1} of submodule M_1, $i_{p\mathrm{I}}$, $i_{p\mathrm{II}}$ and $i_{p\mathrm{III}}$, respectively, are:

$$i_{p\mathrm{I}} = ni_{Lf}(t - t_1) + nV_{in}\sqrt{\frac{C_{j23}}{n^2 L_{r1}}} + \frac{V_o - nV_{in}}{n^2 L_{r2} + L_f}(t - t_1) \tag{20}$$

$$i_{p\mathrm{II}} = ni_{Lf}(t - t_3) + \frac{n^2 L_{r1}(2nV_{in} - V_o)}{\left[2n^2(L_{r1} + L_{r2}) + L_f\right]}\sqrt{\frac{C_{j23}}{n^2 L_{r1}}} \tag{21}$$

$$i_{p\mathrm{III}} = ni_{Lf}(t - t_6) + \frac{n^2 L_{r1}(V_o - nV_{in})}{n^2 L_{r1} + L_f}\sqrt{\frac{C_{j23}}{n^2 L_{r1}}} \tag{22}$$

They are composed of two parts: one for the filter inductor current $ni_{Lf}(t - t_a)$ $(a = 1, 2, 4)$ converted to the secondary, and the other for the resonant inductor and junction capacitor resonant operation. Since $L_r << L_f$, the resonant current of the resonant inductor at the first resonant operation with the rectifier diode junction capacitor is larger than the resonant current at the second and third resonant operations, which makes the resonant inductor resonate with the rectifier diode junction capacitor for the first time with the maximum resonant spike voltage, i.e., the first spike voltage of the rectifier diode is the largest.

The RCD buffer circuit connected in parallel behind the rectifier bridge can buffer the three oscillations of the rectifier diode voltage, which not only does not require additional control circuits but also has a good buffering effect and high reliability. The rectifier bridge is followed by a parallel RCD buffer circuit, which is shown in Figure 8.

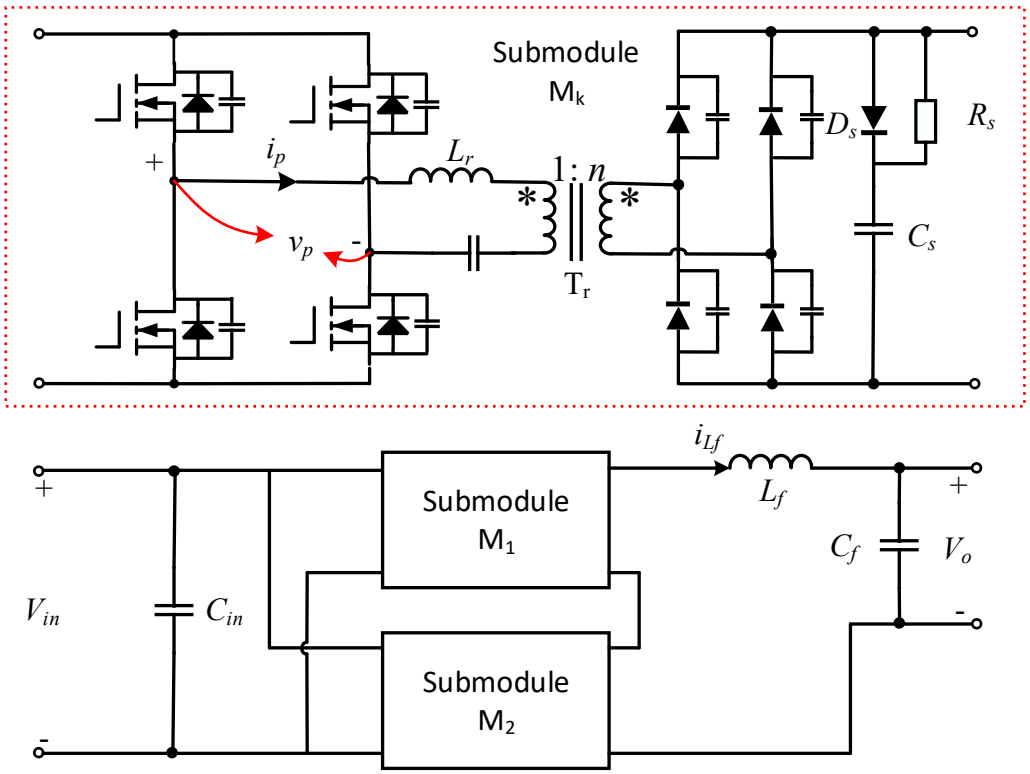


Figure 8. IPOS high-power PSFB converter with RCD buffer circuit.

Because the rectifier diode breakdown voltage depends on the maximum value of the diode transient voltage, the IPOS high-power PSFB converter has the largest spike voltage at the first oscillation. Therefore, the design of the RCD buffer circuit focuses on the suppression of the first spike voltage. The circuit structure utilizes the buffer capacitor C_s to absorb and store the energy from the primary resonant inductor, thereby reducing the spike voltage during diode turn-off. Therefore, the value of C_s in the RCD buffer circuit should be much larger than the value of the diode junction capacitance to achieve a better spike voltage suppression effect. The design of the buffer capacitor C_s and the discharge resistor R_s is crucial to achieving the best buffering effect. A sketch of the voltage waveform across the rectifier diode and C_s is shown in Figure 9.

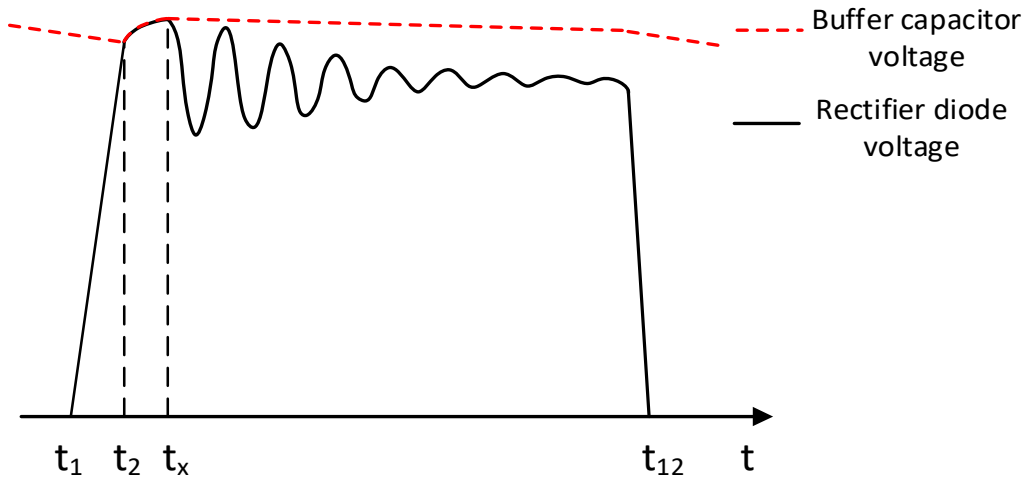


Figure 9. Schematic diagram of diode and buffer capacitor voltages.

The black curve and the red dashed line in Figure 9 are the voltage waveforms across the rectifier diode and C_s, respectively. The primary current of submodule M_1 increases to a value equal to the converted value of the secondary current at moment t_1. The resonant inductor L_{r1} resonates with the

junction capacitors C_{j2} and C_{j3} of rectifier diodes D_2 and D_3, charging the junction capacitors C_{j2} and C_{j3}, and the voltage across the diodes starts to rise. The moment when C_s participates in resonance is t_2, and the moment when C_s starts to discharge is t_x.

3.2. Working Process of RCD Buffer Circuit

With the RCD buffer circuit connected in parallel behind the rectifier bridge, C_s has two completely same charge/discharge cycles in one switching cycle, and the energy absorbed and released in one charge/discharge cycle is the same. The choice of C_s and R_s is mainly related to the energy absorbed or discharged during one charge/discharge. Based on the relationship between the charged energy of C_s and the discharged energy of C_s, an algebraic equation is established to obtain the relationship between the spike voltage, R_s, and C_s. Using this equation, the design of buffer capacitors and discharge resistors within the RCD buffer circuit can be realized to achieve effective suppression and prediction of diode spike voltage values.

The oscillation process of the diode voltage after adding the RCD buffer circuit can be divided into 3 stages.

(1) Stage 1: The C_{j23} voltage is smaller than the C_s voltage; only C_{j23} is involved in resonance, i.e., the [t_1–t_2] period in Figure 9.

(2) Stage 2: The C_{j23} voltage is slightly greater than the C_s voltage, diode D_s turns on, and then C_{j23} and C_s at the same time participate in resonance, that is, the [t_2–t_x] period in Figure 9.

(3) Stage 3: The energy of the resonant part of the resonant inductor L_{r1} has all been transferred to the capacitor. The capacitors C_{j23} and C_s start to discharge at this stage, and the capacitor voltage starts to drop. Since the discharge circuit of C_{j23} is different from that of C_s, and $C_{j23} << C_s$, entering this stage, the voltage across C_{j23} is less than the voltage across C_s, and the diode D_s turns off. The time starting point of this stage is the t_2 moment in Figure 9.

The rectifier diode spike voltage appears at the moment when all the energy involved in the resonant part of the inductor is transferred to the capacitor. The value of the inductor current is equal to the value at the moment of t_1, and the voltage at both ends of the capacitor involved in resonance begins to fall. Stage 2 is the charging process of buffer capacitor C_s, and the energy charged into C_s as:

$$\Delta E_{Cs\_in} = \frac{1}{2} C_s V_{Cs}^2(t_x) - \frac{1}{2} C_s V_{Csmin}^2 \tag{23}$$

The energy of the resonant inductor Lr's resonant part has been fully transferred to the capacitor at the moment t_x. In this stage, the rectifier diode junction capacitors C_{j23} and C_s start to discharge, and the capacitor voltage starts to drop. Since the discharge circuits of C_{j23} and C_s are different, and $C_{j23} << C_s$, after entering this stage, the voltage across C_{j23} is less than the voltage across C_s, and the diode D_s turns off.

Since the time from t_2 to t_x is much smaller than the switching period, the charging time of C_s is ignored when analyzing the discharge process. Because none of the components on the primary side of the transformer participate in the discharge process of C_s, only the circuit state on the secondary side of the transformer is analyzed when discussing the discharge process. The time scale of C_s discharge is much larger than the resonant period, and the effect of resonance is ignored when analyzing the discharge process. Based on the different states of the transformer, the discharge phase of C_s can be analyzed in two processes.

Discharge process 1: The voltage on the secondary side of the transformer is not 0, and the voltage at the output of the rectifier bridge is nV_{in}; Because the capacitance of C_s is large enough, the voltage change across C_s is small throughout the charging and discharging processes. C_s in the discharge state is equivalent to a voltage source, whose value can be approximated as $V_{Cs}(t_x) = V_{Csmin} + \Delta V_{cs}$, where ΔV_{cs} is the amount of change in voltage across C_s. For an IPOS converter consisting of two PSFB converter submodules, the output voltage corresponding to a single submodule is approximated as $V_o/2$. The equivalent circuit for discharge process 1 is shown in Figure 10.

In discharge process 1, the energy discharged by $C_s E_1$ is:

$$E_1 = \frac{V_o V_{Cs}(t_x) \cdot (V_{Cs}(t_x) - nV_{in})}{4nV_{in} R_s f_s} \tag{24}$$

Discharge process 2: The discharge process transformer's secondary voltage is 0, and the energy released by C_s is the energy consumed by R_s. The equivalent circuit of discharge process 2 is shown in Figure 11.

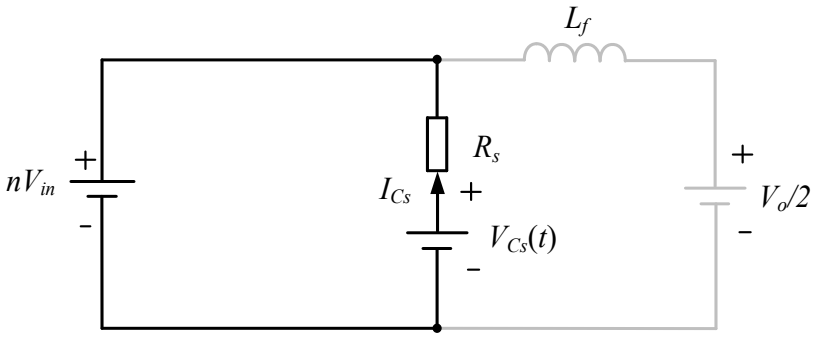


Figure 10. Equivalent circuit of discharge process 1.

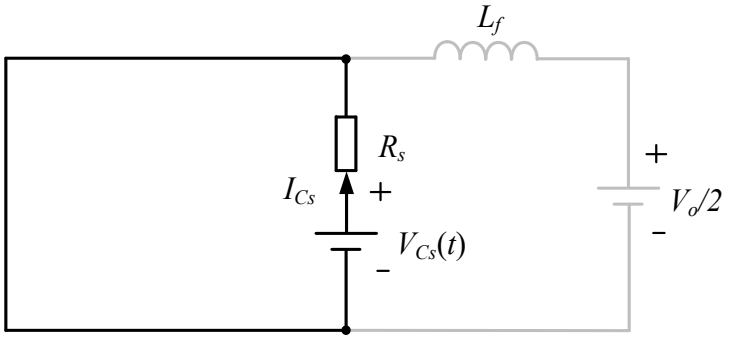


Figure 11. Equivalent circuit of discharge process 2.

In discharge process 2, the energy discharged by C_sE_2 is:

$$E_2 = \frac{V_{Cs}^2(t_x)}{2R_s f_s} \cdot (1 - \frac{V_o}{2nV_{in}}) \tag{25}$$

The energy discharged from the buffer capacitor C_s during one discharge is:

$$\Delta E_{Cs\_out} = E_1 + E_2 = \frac{V_{Cs}(t_x)}{2R_s f_s}(V_{Cs}(t_x) - \frac{V_0}{2}) \tag{26}$$

The energy absorbed and discharged by the buffer capacitor C_s is equal in half a switching cycle, and the relationship between the variation of the spike voltage $V_{Cs}(t)$ with C_s and R_s is obtained by $\Delta E_{Cs\_in} = \Delta E_{Cs\_out}$. The surface plot of the variation of $V_{Cs}(t)$ with R_s and C_s is shown in Figure 12 by substituting the data in Table 1.

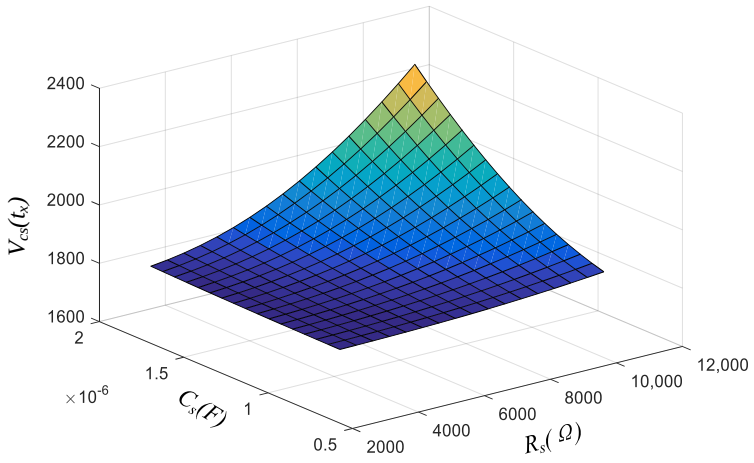


Figure 12. Surface plot of buffer capacitor spike voltage $V_{cs}(t_x)$ with R_s and C_s.

Table 1. Key parameters of the 100 kW prototype.

Parameter	Value
Input voltage V_{in}	240 V
Output voltage V_o	2000 V
Transformer ratio 1:n	1:6
Switching frequency f_s	15 kHz
Transformer leakage inductance L_r	2 µH
Buffer capacitance C_s	0.9 µF
Discharge resistance R_s	4.7 kΩ
Rectifier diode junction capacitance C_j	630 pF
Rated power P_n	100 kW

Under certain operating conditions, as can be seen from Figure 12. In the RCD buffer circuit, when the value of C_s is certain, the smaller R_s, the more energy the buffer capacitor releases through the discharge resistor. The buffer capacitor can participate in the resonance earlier, and the buffer effect is better. But the smaller R_s, the more energy is consumed on it, and the lower the efficiency. When R_s is certain, the smaller the C_s, the lower the voltage when the buffer capacitor is involved in the resonance. So, the C_s can also participate in the resonance earlier, and the buffering effect of the RCD buffer circuit will be better. However, choosing too small a C_s will not only lead to large voltage fluctuations in the buffer capacitor but also cause severe heating of the buffer capacitor and low system efficiency. Therefore, the design of the RCD buffer circuit should take into account the withstand voltage of the rectifier diode and choose a smaller buffer capacitor and resistor as much as the efficiency of the system allows. Thus, the suppression and prediction of diode spike voltage values can be achieved by $\Delta E_{Cs\_in} = \Delta E_{Cs\_out}$.

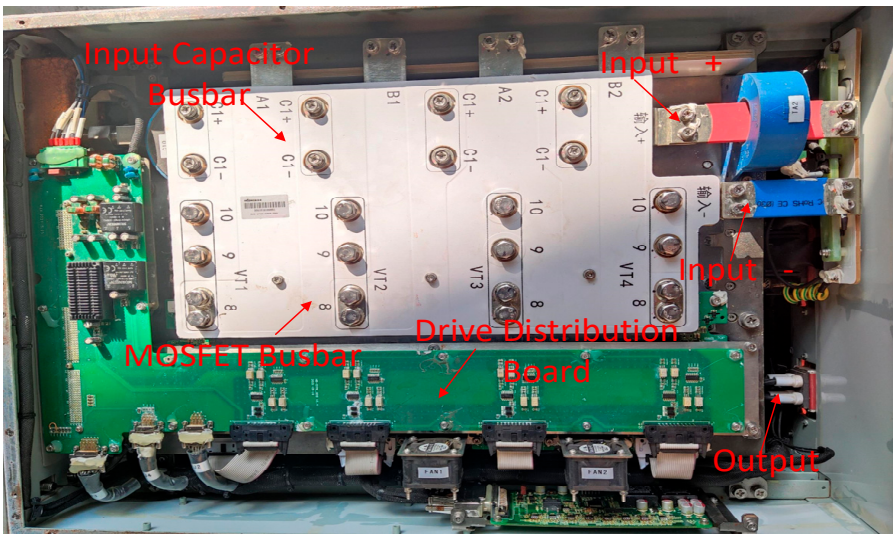
4. Experimental Verification

The correctness of the voltage oscillation mechanism of the rectifier diodes of the IPOS high-power PSFB converter and the accuracy of the prediction of the diode spike voltage values by C_s and R_s are verified on a 100 kW test prototype. Considering that commercially available fast recovery diodes typically have a maximum withstand voltage of 1700 V, two such diodes with a withstand voltage of 1700 V are connected in series for each rectifier diode in the test prototype. Table 1 presents the relevant parameters of the prototype.

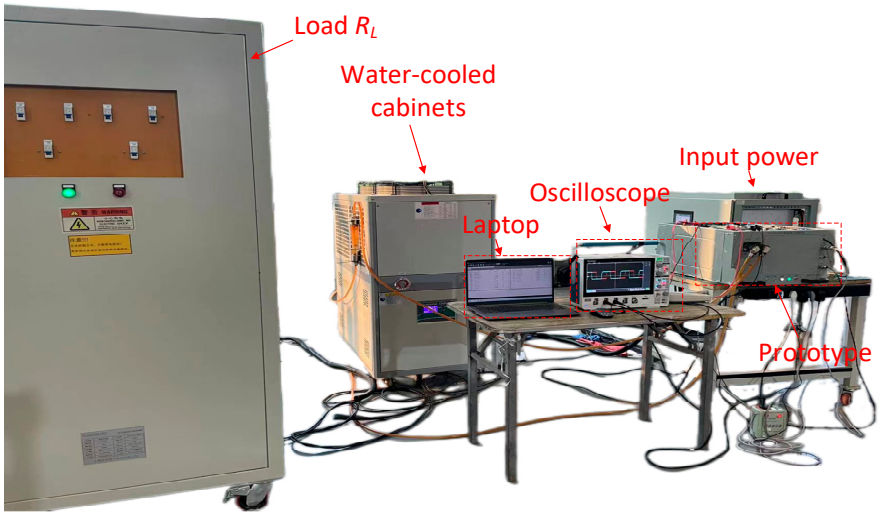
Points to note during the test and the specifications of the measuring equipment are provided in [Appendices A.1 and A.2]. Figure 13 shows the picture of the 100 kW prototype topology and test stand; Figure 14 shows the waveforms of driving pulses of switch transistors S_1 and S_5; Figure 15 shows the waveforms of module output voltage, output current, and rectifier output voltage; and Figures 16 and 17 show the waveforms of rectifier diode voltage and module rectifier output voltage.

Figure 14 provides the interleaved parallel drive waveforms of submodules M_1 and M_2 corresponding to switch transistors S_1 and S_5. The drive pulses of submodules M_1 and M_2 corresponding to switch transistors can be seen to be interleaved in phase by $\pi/2$. Figure 15 gives the module output voltage, module rectifier output voltage, and filter inductor current waveforms, and it can be seen that the inductor current ripple under the drive of interleaved pulses is four times the switching frequency when comparing Figures 14 and 15. Figures 16 and 17 show the voltage waveforms of rectifier diodes D_1, D_5, and D_6 and module rectifier output voltage V_{rect}. The change in amplitude of the diode voltage during the first and second oscillations is seen to increase and then decrease, while the change in amplitude during the third oscillation decreases and then increases. It is also clear from Figures 16 and 17 that the voltage amplitude of the first oscillation of the diode voltage is greater than the voltage amplitude of the second and third oscillations. which is consistent with the conclusions analyzed in Section 2.

To verify the rationality of the buffer capacitor and discharge resistor configuration method in Section 3.2, based on the fact that the rectifier diode voltage does not exceed 2000 V, three combinations of C_s and R_s were selected from Figure 12. The predicted values of the corresponding rectifier diode spike voltages were given as shown in Table 2.



(**a**) Prototype structure



(**b**) Test stand and measurements

Figure 13. One hundred kilowatt (100 kW) prototype topology and test stand.

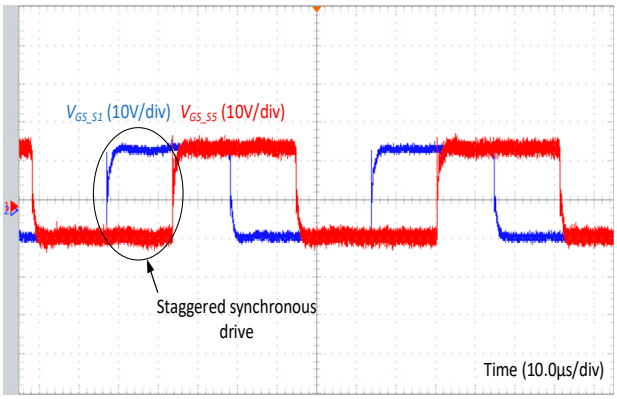


Figure 14. Waveforms of driving pulses of switch transistors S_1 and S_5.

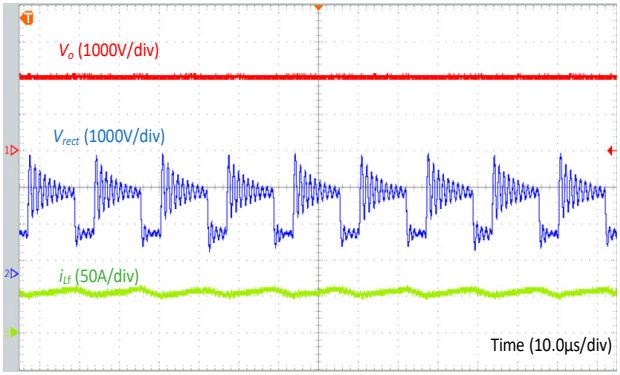


Figure 15. Waveforms of module output voltage V_o, filter inductor current i_{Lf} and rectified output voltage V_{rect}.

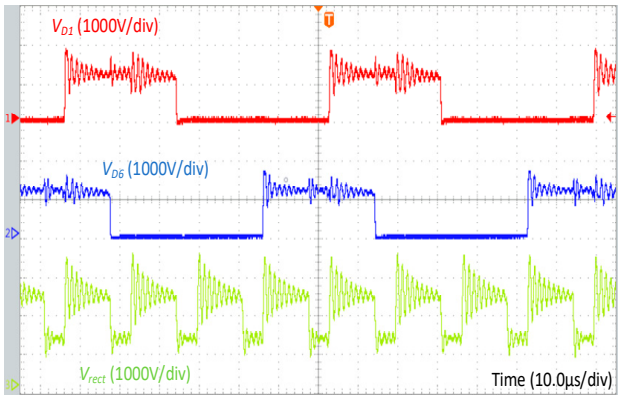


Figure 16. Waveforms of rectifier diode voltage V_{D1}, V_{D6} and module rectifier output V_{rect}.

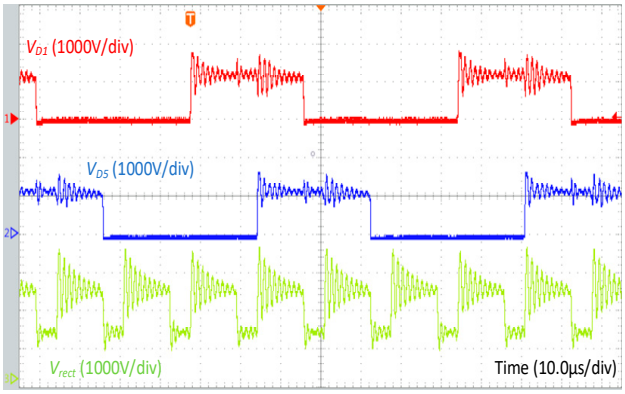


Figure 17. Waveforms of rectifier diode voltage V_{D1}, V_{D5} and module rectifier output V_{rect}.

Table 2. Prediction of rectifier diode spike voltage at different C_s and R_s.

	Absorption Capacitance C_s (µF)	**Discharge Resistance R_s (kΩ)**	**The Predicted Value of Spike Voltage (V)**
a	0.9	4.7	1782
b	1.2	6.2	1841
c	1.4	7.5	1937

According to the three sets of C_s and R_s combinations selected in Table 2. Three sets of rectifier diode voltage spike prediction tests were done under the same operating conditions, and the test pictures are shown in Figure 18.

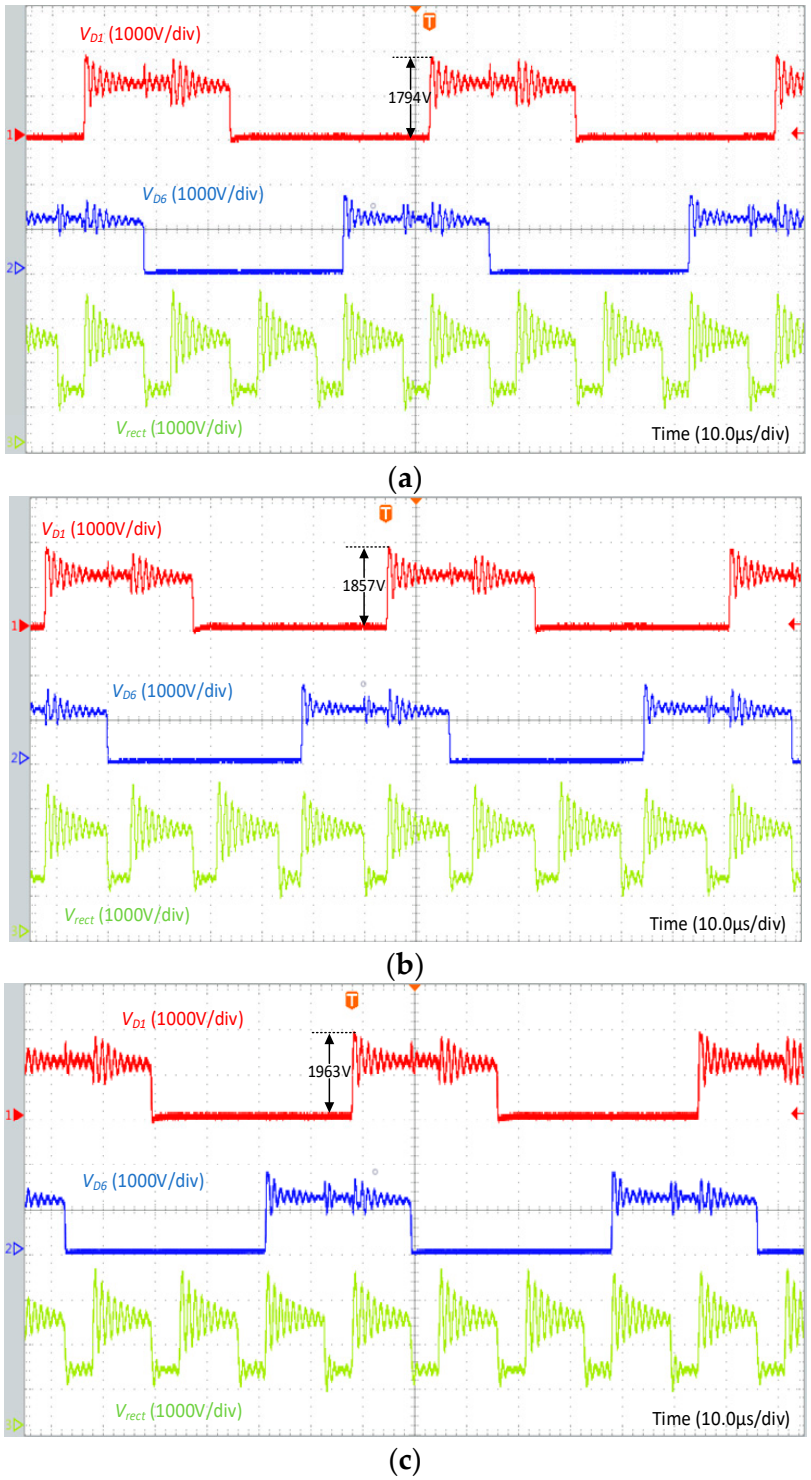


Figure 18. Measurement waveforms of rectifier diode spike voltage for different combinations of C_s and R_s.

As shown in Figure 18a–c, the spike voltage across the rectifier diode D_1 increases as C_s and R_s increase, which is consistent with the conclusion drawn in Figure 12. Table 3 gives the tested values of the diode spike voltages and the voltage error rates of the predicted and tested values for different combinations of R_s and C_s corresponding to the subplots (a), (b) and (c) in Figure 18. The maximum error between the measured and predicted values of rectifier diode spike voltage can be seen to be only 1.34%, which is within the acceptable range in engineering applications.

Table 3. Rectifier diode spike voltage test for different combinations of C_s and R_s.

	Absorption Capacitance C_s (μF)	Discharge Resistance R_s (kΩ)	The Predicted Value of Spike Voltage (V)	Spike Voltage Error Rate (%)
a	0.9	4.7	1794	0.67
b	1.2	6.2	1857	0.87
c	1.4	7.5	1963	1.34

5. Conclusions

This paper innovatively establishes the equivalent circuit model of the rectifier diode voltage parasitic oscillation of the IPOS high-power PSFB converter. It analyzes the mutual influence of rectifier diode voltage oscillations between submodules under interleaved control and investigates the mechanism behind multiple voltage oscillations. The following conclusions are drawn based on prototype testing:

(1) By establishing the equivalent circuit of the parasitic oscillation of the rectifier diode of the IPOS high-power PSFB converter, it improves the precision of the analytical model of the parasitic oscillation of the rectifier diode voltage of the PSFB converter and provides an analytical idea of the parasitic oscillation of the rectifier diode voltage in the complex case of PSFB converters.
(2) Revealing the mechanism of interplay and multiple oscillations of rectifier diode voltage in an IPOS high-power PSFB converter under interleaved control, and it agrees well with the experimental results.
(3) The design method of C_s and R_s is obtained by analyzing the relationship between the rectifier diode spike voltage with C_s and R_s. This method effectively predicts the spike voltage and avoids issues of insufficient margin or over margin in RCD buffer circuit design.

This paper investigates the mechanism of multiple oscillations of rectifier diode voltage and diode voltage spike suppression in an IPOS high-power PSFB converter under interleaved control and achieves certain results, but there are also some shortcomings and room for progress. The RCD buffer circuit reduces the efficiency of the system, so the next step is to find a better voltage spike suppression strategy.

Author Contributions: Conceptualization, F.S. and J.C.; methodology, F.S. and X.L.; formal analysis, J.C. and X.L.; investigation, X.L.; resources, J.C. and X.L.; data curation, X.L.; writing—original draft preparation, F.S.; writing—review and editing, J.C., X.L. and D.L.; funding acquisition, J.C. All authors have read and agreed to the published version of the manuscript.

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Data Availability Statement: The data presented in this study are available in Appendix A.3.

Conflicts of Interest: The funders had no role in the design of the study; in the collection, analyses.

Appendix A

Appendix A.1. Measurement Details

It is worth noting that when measuring the rectifier diode voltage, do not measure only the voltage of the transformer T_{r1} or T_{r2} secondary winding or rectifier bridge output voltage, because this does not reflect the voltage of a specific rectifier diode.

Appendix A.2. Specifications of the Measuring Device

Table A1. Measuring device model and specification.

Name	Producers	Model	Measurement Range	Bandwidth	Quantity
Laptop	Lian Xiang	Xiao Xin AIR 14ITL			One
Oscilloscope	Tektronix	MDO34 3-BW-200		200 MHz	One

Table A1. *Cont.*

Name	Producers	Model	Measurement Range	Bandwidth	Quantity
Voltage Probes	PINTECH	N1070A	0–7000 V	50 MHz	Three
Current Probes	Tektronix	TCPO150	Maximum current RMS 150 A Maximum peak pulse current 500 A	20 MHz	One

Appendix A.3. Buffer Capacitor Spike Voltage $V_{cs}(t_x)$ with R_s and C_s

Table A2. Buffer capacitor spike voltage $V_{cs}(t_x)$ with R_s and C_s.

$V_{cs}(t_x)$ C_s / R_s	7.70E-07	8.40E-07	9.10E-07	9.80E-07	1.05E-06	1.12E-06	1.19E-06	1.26E-06	1.33E-06
3000	1776.82	1777.34	1778.02	1778.90	1779.99	1781.33	1782.93	1784.82	1787.01
3500	1777.08	1777.75	1778.63	1779.77	1781.19	1782.91	1784.98	1787.42	1790.25
4000	1777.39	1778.23	1779.35	1780.79	1782.59	1784.78	1787.40	1790.48	1794.06
4500	1777.74	1778.79	1780.19	1781.99	1784.22	1786.94	1790.20	1794.03	1798.47
5000	1778.15	1779.44	1781.16	1783.36	1786.10	1789.43	1793.42	1798.10	1803.53
5500	1778.61	1780.18	1782.26	1784.92	1788.23	1792.26	1797.07	1802.71	1809.25
6000	1779.14	1781.01	1783.50	1786.68	1790.64	1795.45	1801.18	1807.91	1815.68
6500	1779.73	1781.95	1784.89	1788.66	1793.34	1799.02	1805.78	1813.70	1822.85
7000	1780.39	1782.99	1786.44	1790.86	1796.34	1802.98	1810.88	1820.12	1830.77
7500	1781.12	1784.15	1788.16	1793.29	1799.65	1807.36	1816.51	1827.19	1839.48
8000	1781.93	1785.42	1790.06	1795.97	1803.30	1812.16	1822.67	1834.92	1848.99
8500	1782.81	1786.82	1792.13	1798.90	1807.29	1817.41	1829.39	1843.34	1859.32
9000	1783.78	1788.35	1794.40	1802.10	1811.62	1823.11	1836.69	1852.45	1870.47
9500	1784.83	1790.01	1796.86	1805.57	1816.33	1829.28	1844.56	1862.27	1882.47
10,000	1785.97	1791.81	1799.52	1809.32	1821.41	1835.93	1853.03	1872.80	1895.32
10,500	1787.20	1793.75	1802.40	1813.37	1826.87	1843.07	1862.10	1884.07	1909.02
11,000	1788.53	1795.85	1805.49	1817.70	1832.72	1850.70	1871.79	1896.06	1923.58

Table A3. Buffer capacitor spike voltage $V_{cs}(t_x)$ with R_s and C_s.

$V_{cs}(t_x)$ C_s / R_s	1.40E-06	1.47E-06	1.54E-06	1.61E-06	1.68E-06	1.75E-06	1.82E-06	1.89E-06
3000	1789.54	1792.41	1795.66	1799.30	1803.35	1807.82	1812.74	1818.12
3500	1793.51	1797.22	1801.40	1806.08	1811.28	1817.02	1823.31	1830.18
4000	1798.18	1802.85	1808.12	1814.00	1820.53	1827.73	1835.61	1844.19
4500	1803.57	1809.36	1815.87	1823.13	1831.18	1840.03	1849.70	1860.22
5000	1809.74	1816.79	1824.71	1833.53	1843.27	1853.97	1865.65	1878.31
5500	1816.73	1825.19	1834.68	1845.23	1856.87	1869.62	1883.49	1898.51
6000	1824.56	1834.60	1845.82	1858.28	1871.99	1886.98	1903.26	1920.83
6500	1833.28	1845.04	1858.17	1872.71	1888.68	1906.09	1924.96	1945.28
7000	1842.89	1856.54	1871.74	1888.54	1906.94	1926.96	1948.60	1971.84
7500	1853.44	1869.12	1886.56	1905.78	1926.78	1949.58	1974.15	2000.49
8000	1864.94	1882.81	1902.64	1924.43	1948.20	1973.94	2001.61	2031.19
8500	1877.39	1897.60	1919.98	1944.51	1971.20	2000.01	2030.93	2063.90
9000	1890.82	1913.52	1938.58	1965.99	1995.74	2027.79	2062.08	2098.56
9500	1905.23	1930.55	1958.44	1988.88	2021.82	2057.22	2095.02	2135.14
10,000	1920.62	1948.70	1979.55	2013.14	2049.40	2088.28	2129.69	2173.56
10,500	1936.99	1967.96	2001.90	2038.76	2078.46	2120.92	2166.06	2213.77
11,000	1954.34	1988.32	2025.47	2065.71	2108.96	2155.11	2204.07	2255.71

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