electronics

MDPI

Article

Reconfiguration Using Bio-Inspired Conduction Mode of Field-Effect Transistors toward the Creation of Recyclable Devices

Roberto Baca-Arroyo

Department of Electronics, National Polytechnic Institute, School of Mechanical and Electrical Engineering, Mexico City 07738, Mexico; rbaca02006@yahoo.com.mx; Tel.: +52-01-5729-6000

Abstract: A bio-inspired conduction mode in silicon-based field-effect transistors was studied here using the frequency-dependent reconfiguration principle in a size-reduced circuit architecture. Analog circuits comprising neuromorphic and reconfigurable behavior were analyzed across their physical quantities using a set of equations governing circuit performance. Practical examples were built, analyzed, and discussed from a phenomenological viewpoint. Upon exploiting their reconfiguration properties when semiconductor devices and passive components are interconnected, novel operating principles might inspire optimized signal processing and manufacturing facilities to design circular device-based complex systems.

Keywords: field-effect transistor; reconfiguration; bio-inspired conduction mode; circular devices; sustainable cycle

Citation: Baca-Arroyo, R. Reconfiguration Using Bio-Inspired Conduction Mode of Field-Effect Transistors toward the Creation of Recyclable Devices. *Electronics* **2023**, *12*, 2270. https://doi.org/10.3390/electronics12102270

Academic Editor: Francesco Giuseppe Della Corte

Received: 4 March 2023
Revised: 24 April 2023
Accepted: 10 May 2023
Published: 17 May 2023

1. Introduction

To challenge the semiconductor industry's trend toward focusing on the shrinkage of CMOS transistors, where run-time faults occur during storing and processing into digital circuit architectures because many complex operations are computed [1], it is desirable to find the best way to divide large networks into smaller simple circuits, similar to biological circuits. For example, a good compromise between the shortcomings of digital processing and the benefits of analog neuromorphic architecture is needed to devise a reconfigurable circuit capable of simulating digital signal processing and neuron ionic activity in real time. It is well known that analog circuits can model biological activity even faster than it happens in real life, use fewer active and passive components to operate at a lower voltage, to model the synapses that are associated with artificial neurons, which are always in flux and constantly being reinforced or phased out to mimic the way human neurons behave [2–4].

Scientific evidence from modern events in the context of the COVID-19 pandemic has perturbed the lives of humans, leading us to question where our civilization is headed, allowing us to promote sustainable engineering in the electronics industry, where the interrelation of environmental, social, and economic dimensions must force further research on innovative modes of production and their impact on the environment and human health worldwide [5].

The growing demand for consumer electronics has led to unsustainable amounts of waste products and adverse impacts, which are not expected to change in the coming decades. However, at present, several publications have emphasized waste reduction and recycling policies [6,7]: (1) policymakers are actively encouraging the repair and life extension of electrical and electronic equipment; (2) responsible recycling when consumers return electronic products to the point of purchase; (3) pro-active approaches to delaying the consignment of waste products to landfills through resource-efficient manufacturing; (4) recycling to decrease demand for new metal production and to reduce carbon footprints;

and (5) using recyclable materials and understanding their breakdown mechanisms to avoid waste.

The scope that the circularity approach must address is still unclear; however, taking advantage of a bio-inspired conduction mode in field-effect transistors could be crucial to solving existing challenges in the electronics industry, where in recent years it has been confirmed that CMOS technology is flexible enough to integrate complex digital systems that can contain many millions of small elementary circuits constructed using a reduced number of transistors. However, the complexity of these systems could be lessened by seeking and applying unusual conduction modes, which might play an important role in preventing new waste products in the circuits' premature end-of-life stage if the repair/reuse and remanufacture of any application-specific industry-scale building blocks are incorporated. Hence, this work studies a bio-inspired conduction mode in field-effect transistors to suggest future directions for designing recyclable devices as part of a sustainable cycle. Possibilities for circuit architecture, including two circuit properties—neuron-like spike generation and reconfigurable signal processing—will be detailed in Section 2. Practical examples using two field-effect transistor types will be covered in Section 3. Finally, conclusions about this research are presented in Section 4.

2. Circuit Architecture

Due to the biological brain's ability to quickly process large quantities of simultaneous information in a small package, which is the result of the coordinated action of many highly interconnected brain areas, previous research has focused on modeling those individual parts of the human brain, which is composed of 100 billon nerve cells called neurons, whose biological activity consists of talking to each other by means of dendrites and axons, which transmit electrical impulses, fire biological neurons, and center integration and spike generation from one neuron to another [8].

Because bioprocessing in the nervous system occurs at the junctions between neurons (known as synapses), the learning of new information depends on how closely any two neurons are linked. The circuits depicted in Figure 1 contain one inductor series connected to the active device, which can follow the non-linear ionic activity of a neuron, such as a biological neuron. Meanwhile, Neuron 1, through the external stimulus of the region known as the soma, is equivalent to the inductor and can send a signal down the axon, which is equivalent to the junction capacity of each active device, creating a synapse with Neuron 2, where integration and spike generation at the output of each active device can be collected as electrical impulses, as shown in Figure 1 [9]. Here, the equivalent-circuit linear functions of two active devices [10,11], namely, a field-effect transistor (FET) and a metal oxide semiconductor field-effect transistor (MOSFET), will follow p–n-junction-like behavior at the gate–source junction, being roughly analogous to a physical circuit quantity arranged into state equations governing circuit performance, as explained below:

2.1. Circuit Based on FET

It is instructive to analyze the current paths into two basic operation modes to give a qualitative idea of the phenomenological response involved in operating the circuit architecture of Figure 1. The detailed description of each mode is given below:

Mode 1: At the beginning, the gate–source junction is forward biasing across the series inductor connected at V_{IN}, where electrons are injected from the n region into the p^+ regions, and holes are injected from the p^+ regions into the n region, which allows the inductor to store enough energy. The gate–source capacitance, C_{GS}, initially gets charged through the p^+–n junction, but channel formation is missing, as shown in Figure 2a.

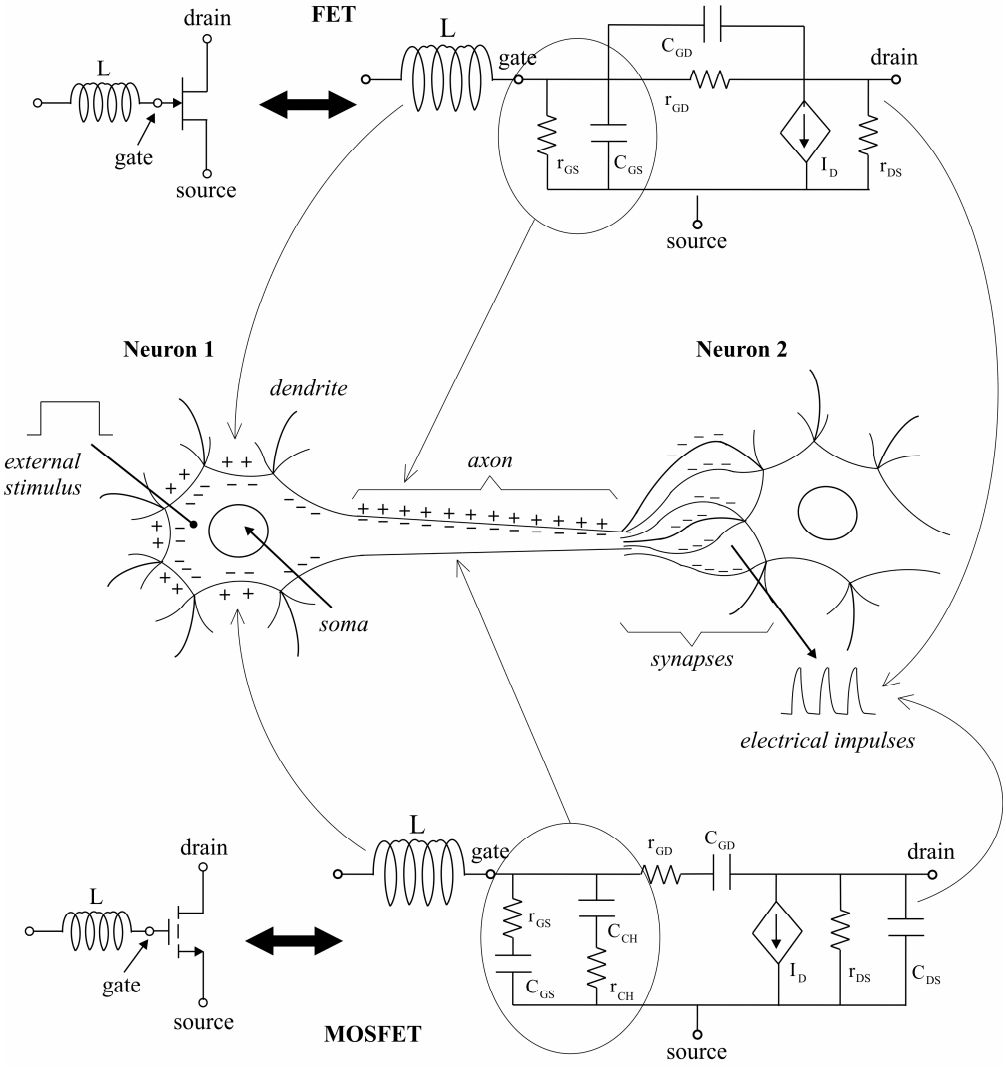

Figure 1. Schematic view for explaining the relationship between biological neurons and proposed circuits as synthetic neurons when the inductor is series connected with the equivalent physical circuit of the FET and MOSFET devices for spike generation.

The equation governing this operation mode is

$$V_{IN} = L\frac{dI_G}{dt} = L\frac{d^2Q_G}{dt^2}, \quad (1)$$

Mode 2: When the polarity of V_{IN} is inverted and the gate–source junction is reverse biasing, two conduction stages happen. (a) Due to the reverse energy stored in the inductor, C_{GS} becomes oppositely charged until it begins its discharge action across gate–source resistance, r_{GS}. Accordingly, transient channel resistance along the source–drain junction occurs, equivalent to an ON-state. (b) Due to the reduced charge-handling capacity in C_{GS} and the higher inductor voltage of V_L compared with V_{IN}, the C_{GS} becomes forward charged while it exchanges energy with the inductor, until it begins its discharge action across r_{GS}. Thus, conduction along the source–drain junction will be missing, which is equivalent to an OFF-state. As such, these conduction states together assemble an electrical impulse, which is dependent on the fluctuation of the electric field into the *n* region (channel length), as shown in Figure 2b. The equations governing this operation mode are

$$\frac{Q_G}{C_{GS}} + \Phi_B = L\frac{d^2Q_G}{dt^2}, \quad (2)$$

$$\frac{dQ_G}{dt} = \frac{Q_G}{r_{GS}C_{GS}}, \tag{3}$$

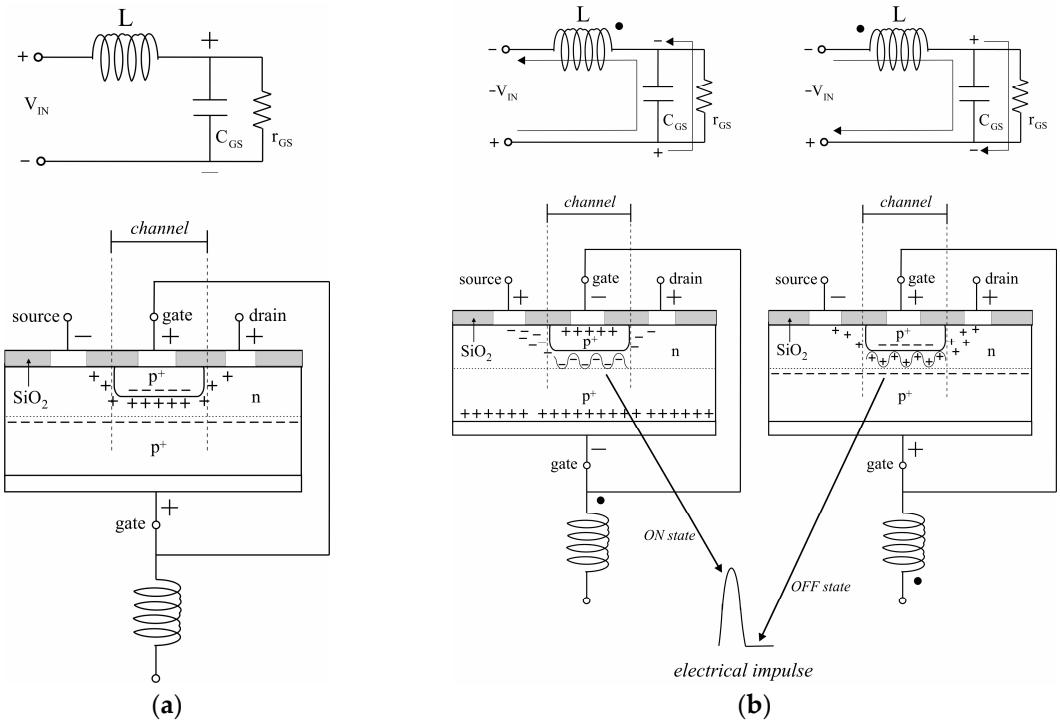

Figure 2. Phenomenological response of the suggested circuit in Figure 1 using a FET device: (**a**) at forward bias during Mode 1; (**b**) at reverse bias during Mode 2. The figure shows a schematic diagram of the physical structure of a FET.

2.2. Circuit Based on MOSFET

The phenomenological response predicted to serve as a mutual description between the physical structure and equivalent circuit through current paths is related to the two basic operating modes in the circuit architecture of Figure 1. Detailed descriptions of each mode are given below:

Mode 1: At the beginning, the gate–source junction is forward biasing across the series inductor connected at V_{IN}, where two transitory conduction stages occur. (a) Bulk charge distribution can be induced into the p region when channel capacitance, C_{CH}, is charged through channel resistance, r_{CH}, via electric field action along the source–drain junction. (b) Due to the reduced charge-handling capacity in C_{CH} and reverse energy stored in the inductor, a decrease in the charge toward the gate–source junction is observed when the gate–source capacitance, C_{GS}, is charged through gate–source resistance, r_{GS}. Hence, the resistance along the source–drain junction obeys the charge fluctuation at low-level injection, where two equivalent states, the so-called ON-state and OFF-state, are achieved. These states assemble an electrical impulse, as shown in Figure 3. The equations governing this operation mode are

$$L\frac{d^2Q_{G1}}{dt^2} + r_{CH}\frac{dQ_{G1}}{dt} + \frac{Q_{G1}}{C_{CH}} = V_{IN}, \tag{4}$$

$$\frac{Q_{G1}}{C_{GS}} + r_{GS}\frac{dQ_{G1}}{dt} = V_T, \tag{5}$$

Mode 2: Due to the reduced reverse energy stored in the series inductor and charge stored along the source–drain junction during Mode 1, three conduction stages can arise:

(a) Surface charge can be distributed at high-level injection to induce the n-channel, when C_{GS} is charged across r_{GS}. (b) The C_{CH} is weakly charged across channel resistance, r_{CH}, while the surface charge quickly begins to be deficient as a function of the reduced charge-handling capacity in C_{CH}, which is distributed toward the interface of the n^+–p junction. (c) The inductor exchanges residual energy with C_{CH} through r_{CH} and is empty when a blocking state in the n^+–p junction is attained. Accordingly, the charge distribution along the n-channel length obeys the charge fluctuation via a higher electric field condition, where two equivalent states, the so-called ON-state and OFF-state, assemble a different electrical impulse, as shown in Figure 4. The equations governing this operation mode are

$$L\frac{d^2Q_{G2}}{dt^2} + r_{GS}\frac{dQ_{G2}}{dt} + \frac{Q_{G2}}{C_{GS}} = -L\frac{d^2Q_{G1}}{dt^2}, \tag{6}$$

$$\frac{Q_{G2}}{C_{CH}} + r_{CH}\frac{dQ_{G2}}{dt} = \Phi_S, \tag{7}$$

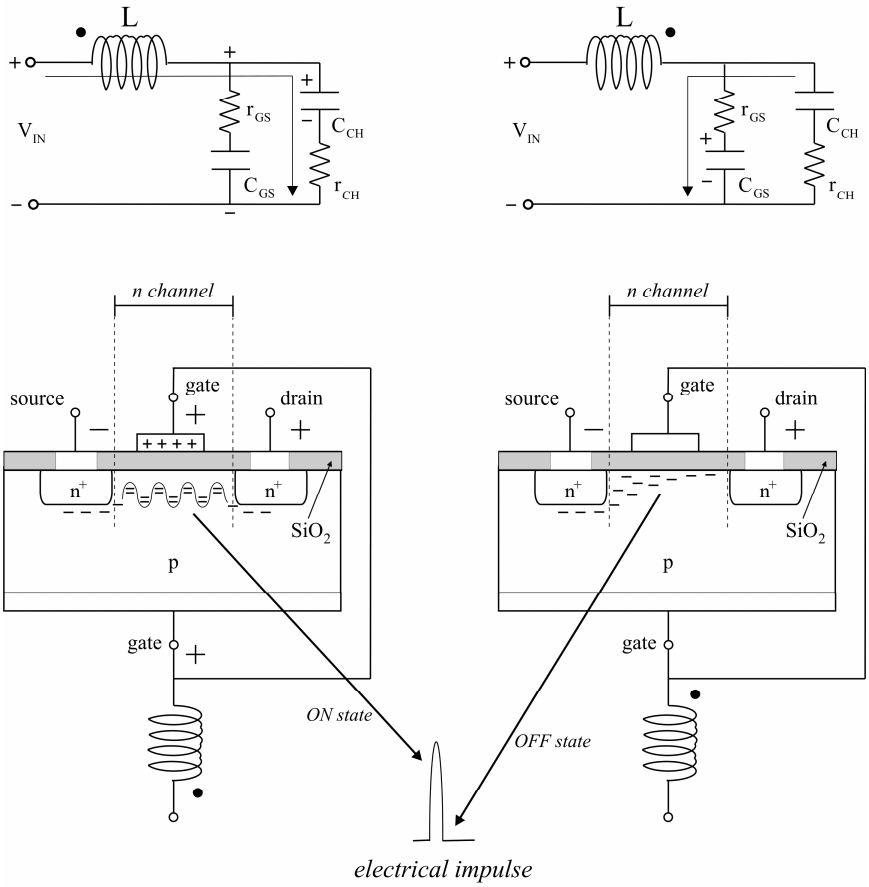

Figure 3. Phenomenological response of the suggested circuit in Figure 1 using a MOSFET device at positive voltage during Mode 1. The figure shows a schematic diagram of the physical structure of a MOSFET.

The empirical discussion on the p–n junction action in each FET or MOSFET device as a function of the physical parameters, as well as expected solutions for earlier equations governing each operating mode, are specified in Appendix A.

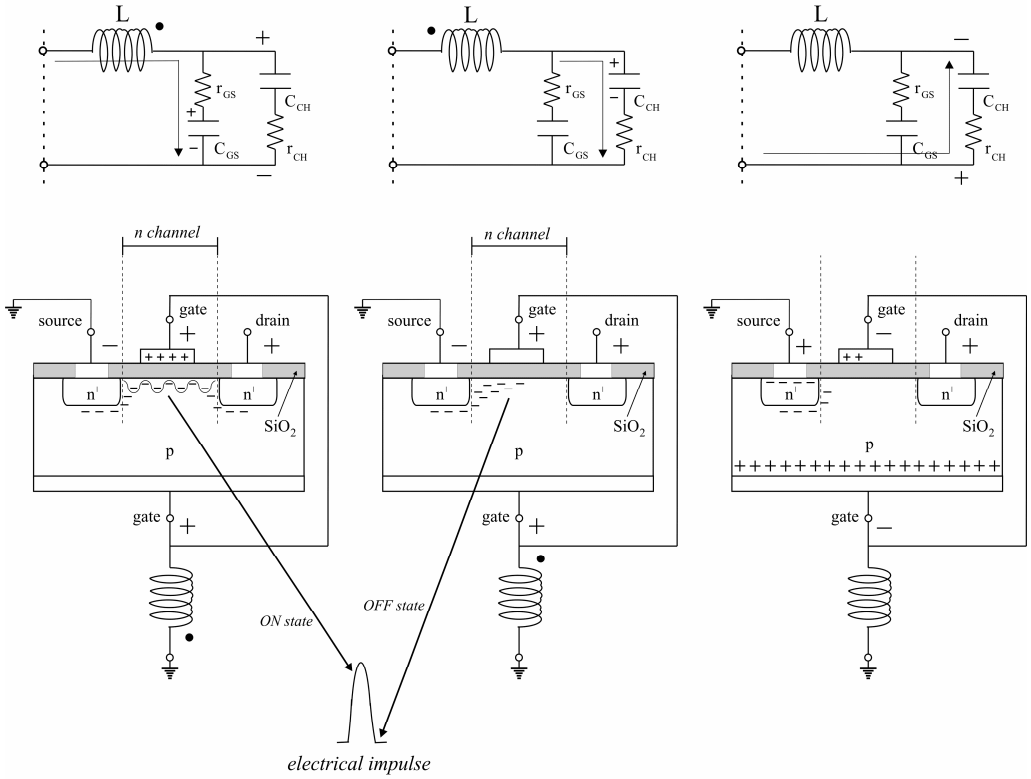

Figure 4. Phenomenological response of the suggested circuit in Figure 1, using a MOSFET device at zero voltage during Mode 2. The figure shows a schematic diagram of the physical structure of a MOSFET.

3. Circular Devices

Actions for the development of electrical and electronic equipment toward more energy-efficient and green manufacturing routes must follow, for example, a paradigm change in design for passive components (e.g., resistors, capacitors, and inductors) and nonlinear active devices (e.g., diodes, transistors, and memristors). Thus, bridges of collaboration among society, academia, and industry are needed to transform each stage into a circular scenario, as projected in Figure 5. Here, it is essential to describe four aspects in which a sustainable cycle might succeed:

- Domestic and industrial waste is an issue that requires urgent attention and adversely impacts economic, environmental, and health factors. Manufacturers of printed circuit boards (PCBs) and the silicon semiconductor industry have so far followed a traditional linear economy value chain, leading to high volumes of waste production and loss of value at the end of life. For example, to replace the traditional tracks on PCBs, conductive materials must possess stability and electrical functionality with existing materials, and to replace the existing semiconductor devices (SDs), their charge transport properties depend on reconfigurable charge carrier mobility and higher thermal stability. Therefore, cellulose, as one of the attractive substrate materials because of its flexibility, thermal stability, and simple synthesis technique, can be designed for easier dismantling opportunities, enabling electronics innovation [12,13], while next-generation SDs can be created with biodegradable materials, such as silicon nanomembranes (Si-NM), metal oxides, and conducting polymers [14,15];
- Novel business models can be created through the circulation of new knowledge, leading to innovative technical processes, products, and services focused on initiatives for repair/reuse and redesign into circular economy objectives, using fewer resources and closed-loop material flow, and decreasing negative environmental impacts by including remanufacturing, maintenance, recycling planning, and avoiding the use and generation of hazardous substances. New business models highlight a transition

to more sustainable practices regarding waste products that are currently eluding decision makers. Products can be maintained for as long as possible, but before they fail and have to be disposed of, they must be rigorously tested and potentially certified for performance, safety, and reliability for their transformation and reintroduction within a sustainable cycle [16,17];

- Education must highlight the impacts of recovery/recycling approaches on circular vision at every level, offering learning activities from pre-university science to university engineering and technology courses. There are many ways to engage education institutions by creating syllabi focused on recycling at a discrete-component level, where student's creativity could be considered, taking into account the traditional and uncommon properties of materials, as well as the atypical characteristics of the passive and active devices. Thus, the courses can be planned, for example, using well-known basic circuit theorems that were often conceived decades ago but now have additional mathematical models interrelated with the physics of semiconductors. Moreover, simulation software as design tools must allow the building of next-generation circuit architectures within several innovative functions combined with few components [18,19];
- Due to the specialized nature of the materials, those used in advanced integrated circuits (e.g., digital processors), such as gold, platinum, and palladium, are much less abundant and used sparsely, while copper, a more abundant and densely used material, is categorized as a source of cancerous diseases, and has the largest environmental footprint together with tin, lead, and mercury in terms of human toxicity impact [20]. Accordingly, the electronics industry must solve challenges, such as materials compatibility, thermal stability, unstressed current-handling capacity, and scalable circuit solutions. Thus, the recovery of waste materials (e.g., silicon, iron, copper, and aluminum) can be expected to upgrade the circularity stages by exploiting a material's unusual properties (e.g., reconfiguration, refurbishment, and reuse) to satisfy the need for an extended product lifecycle and long-term waste mitigation [21,22].

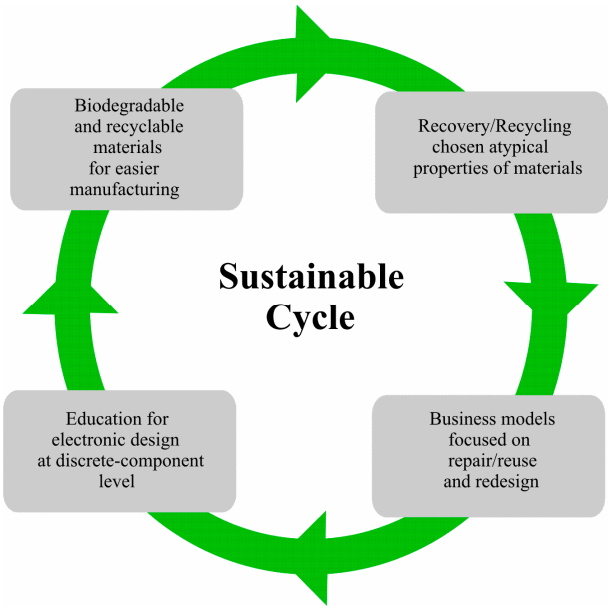

Figure 5. Projected stages for circularity-based paradigm change in a sustainable cycle.

There are practical examples of circular devices using the n-channel FET (type 2N5457; Fairchild Semiconductor) and the n-channel MOSFET (type 2N7000; ON Semiconductor), with an inductor L = 750 μH of 450 turns built using recycled magnetic wire AWG # 32 from out-of-date magnetic components, and bulk winding on a square base with a length of 10 mm and cross-sectional area of 0.25 cm^2 was experienced. For biasing purposes, resistors

R_1 = 2.2 kΩ and R_2 = 47 kΩ were of $\frac{1}{4}$ W at 5%, and to avoid switching noise due to the power supply current pulses flowing through parasitic inductors, typical Mn-Zn-Graphite batteries were connected in series at each circuit architecture.

To characterize the performance of each circuit architecture, we generated and extracted the voltage waveforms using a function generator (Matrix, MFG-8250A) and digital storage oscilloscope (Tektronix, TDS1012C), respectively. Based on the principles detailed in the foregoing section, the tested current–voltage characteristics from the manufacturer's datasheet for each silicon-based active device have been correlated in accordance with the physical semiconductor models [23,24]. Therefore, semiconductor parameters were computed, and the values are summarized in Tables 1 and 2 for 2N5457 and 2N7000, respectively. Next, physical behavior under the biasing conditions established for the practical examples is discussed:

Table 1. Physical parameters of the 2N5457 transistor.

Static	**Nomenclature**	**Value**
donor concentration	N_D	5×10^{15} cm^{-3}
acceptor concentration	N_A	2×10^{17} cm^{-3}
dielectric constant for Si	K_{Si}	11.7
channel transconductance	g_m	6.5×10^{-4} mhos
thickness of channel	d	2 µm
effective channel length	L	20 µm
channel width	Z	5000 µm
carrier mobility	μ_n	12.95 cm^{2}V^{-1}s^{-1}
built-in potential	Φ_B	0.7548 eV
Dynamic	**Nomenclature**	**Value**
input voltage	V_{IN}	2 V
gate–source resistance	r_{GS}	11.36 Ω
gate–source capacitance	C_{GS}	8.80 pF
cut-off frequency	f	1 MHz

Table 2. Physical parameters of the 2N7000 transistor.

Static	**Nomenclature**	**Value**
donor concentration	N_D	5×10^{17} cm^{-3}
acceptor concentration	N_A	2×10^{15} cm^{-3}
dielectric constant for Si	K_{Si}	11.7
dielectric constant for S_iO_2	K_{OX}	3.9
thickness of the S_iO_2	X_{OX}	100 nm
channel transconductance	g_m	2×10^{-3} mhos
effective channel length	L	20 µm
channel width	Z	2000 µm
carrier mobility	μ_n	400 cm^{2}V^{-1}s^{-1}
surface potential	Φ_S	1.5097 eV
Dynamic	**Nomenclature**	**Value**
input voltage	V_{IN}	5 V
turn-on voltage	V_T	0.4257 V
gate–source resistance	r_{GS}	0.1032 Ω
gate–source capacitance	C_{GS}	219.6 pF
channel resistance	r_{CH}	125 Ω
channel capacitance	C_{CH}	9.29 pF
cut-off frequency	f	40 MHz

3.1. Reconfigurable Conduction Mode in FET

Figure 6a shows how reconfigurable behavior can occur in the circuit architecture when operating at 200 kHz, which is caused by the negative square-wave pulse depending on the

amplitude of three voltages, V_{IN}. Their physical operating principle, whose experimental waveforms are displayed in Figure 6b–d, can be discussed as follows: At V_{IN} = 200 mV, the gate and source regions on the FET (see Figure 3) operate through the wide space-charge region, which is similar to the p^+–n junction, where an adequate electric field is produced after a certain number of charge carries (electrons and holes) have flowed. Thus, this behavior corresponds with a logic circuit. At V_{IN} = 1 V, the distribution of the charge carries within the p^+–n junction through the narrow space-charge region, where a reduced electric field allows their transient diffusion into the n-channel's length, whose behavior is equivalent to the neuron-like spikes that are generated in neuromorphic circuits. At V_{IN} = 2.5 V, the transient diffusion begins to be negligible near the p^+–n junction, which is just below the lowly doped n-region, meaning that decreasing neuron-like activity in a reduced space-charge region under a lower electric field is attained.

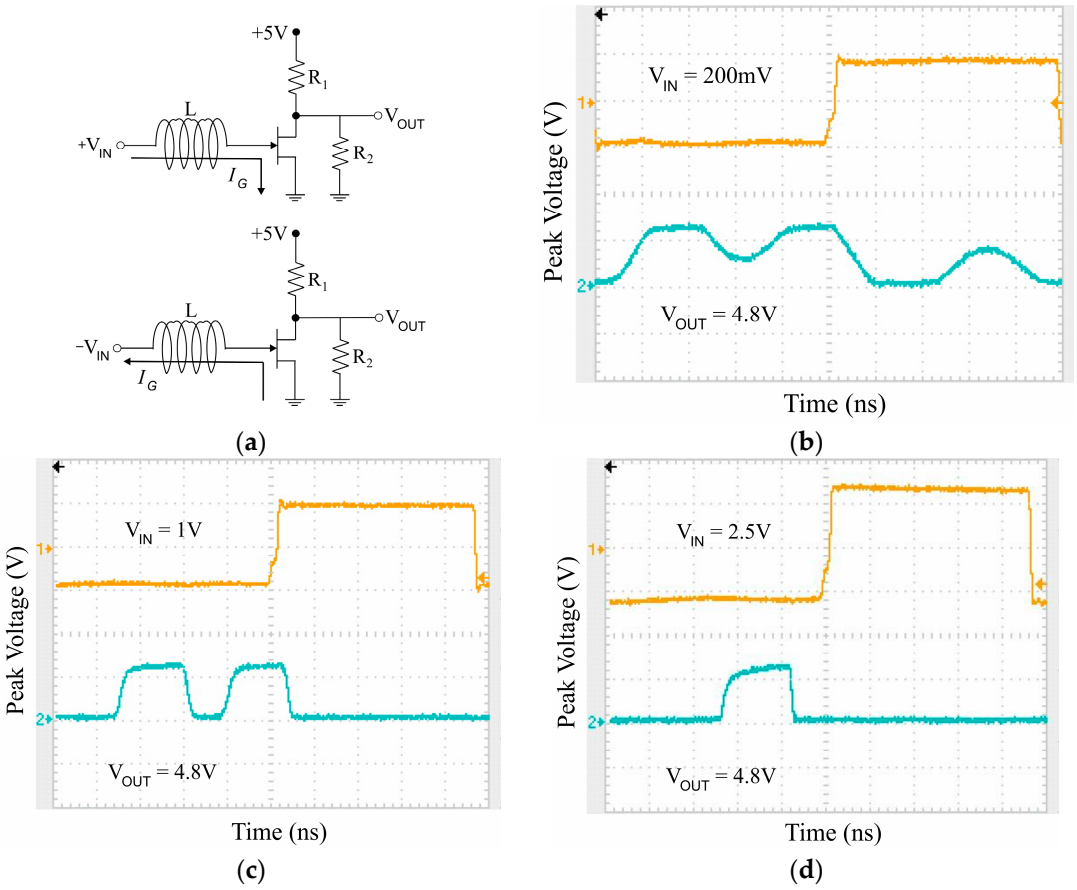

Figure 6. FET during reconfigurable conduction mode: (**a**) schematic circuit and biasing conditions; (**b**–**d**) input and output waveforms under 200 kHz and three input voltages.

3.2. Reconfigurable Conduction Mode in MOSFET

To confirm that a MOSFET can operate in an unusual conduction mode, the circuit architecture in Figure 7a was built. Figure 7b–d show the resulting output waveforms, V_{OUT}, when a square-wave pulse with V_{IN} = 5.6 V corresponding to a TTL level was applied. Because the distribution of the charge carried in the n-channel depends on the bias condition in the p–n^+ junction and the space-charge capacitance at the gate–source junction, the circuit must operate at a variable frequency, as follows:

At f = 160 kHz, charge accumulation in the gate–source junction and low-level injection force a transient diffusion of the carries along the n-channel, which means that neuron-like spikes are generated at the zero square-wave pulse. At f = 175 kHz, the saturation of the space-charge capacitance and high-level injection due to a constant electric field along the n-channel occurs at positive and zero square-wave pulses, resulting in a correspond-

ingly higher number of neuron-like spikes during the transient diffusion phenomena. At f = 250 kHz, the velocity of the charge carried along the n-channel is higher than the velocity for the exchange of energy between the inductor and space-charge capacitance arising in the lowly doped p-region [25]; therefore, charge accumulation through this p–n^+ junction allows a delayed conduction, which obeys the well-known logic circuit performance [26].

As a result, the synthesis of neuron-like spikes has already taken place during the square-wave pulse transfer across the inductor by the time the signal reaches each space-charge capacitance to exchange energy, such as the nonlinear LC circuit at the resonance condition [27,28], integrating over the drain–source junction until the spikes are generated, as shown in Figures 6 and 7, respectively.

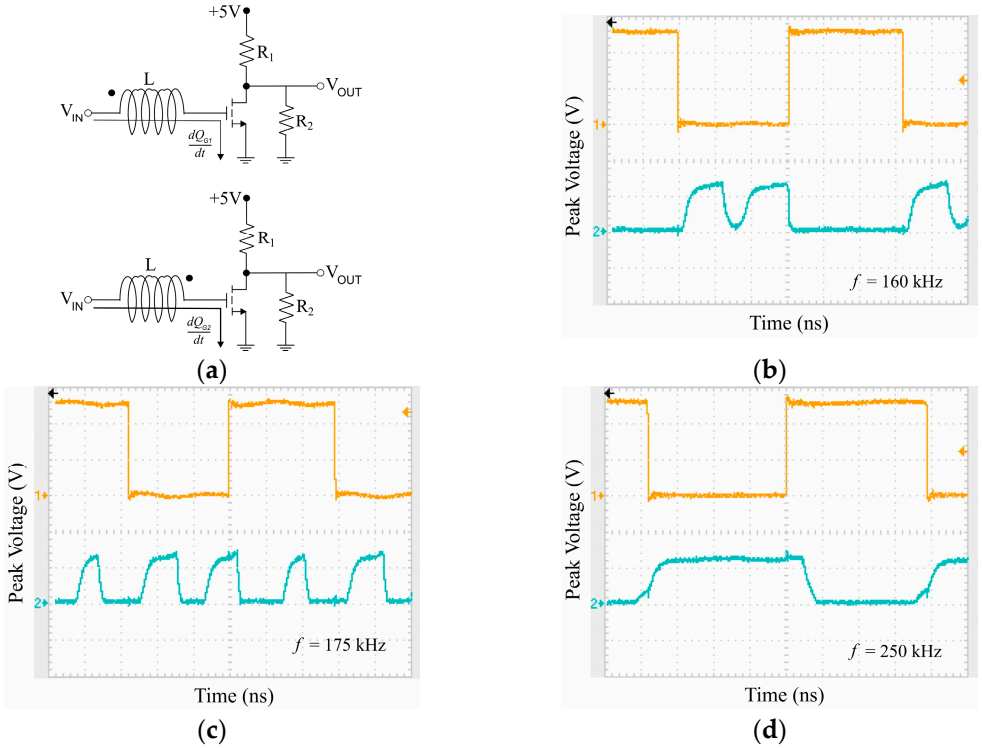

Figure 7. MOSFET during reconfigurable conduction mode: (**a**) schematic circuits at two current-injection levels; (**b**–**d**) output waveforms when a square-wave pulse at the input of three operating frequencies was applied.

The neuromorphic behavior of the underlying hardware is divided up between hardware that processes similar to how the body of a neuron functions and hardware that processes the way that axons work, and practical examples have focused on building biological activity using simple circuit architectures operating at higher voltage (>1 volts) in comparison to around 0.1 volts in human neurons, which means that electrical impulses can be generated and transmitted using flexible power consumption [29,30].

Likewise, with increasing amplitude or frequency in the input square-wave pulse, the transferred signal across the FET or MOSFET is always at the ready, responding upon receiving a stimulus, similar to how logic circuits in computer processors execute functions in discrete time steps.

3.3. Validation of the Reconfiguration Principle

The small-signal equivalent circuit models suggested in Figure 1 consider intrinsic elements mainly affected by the conduction of current drain and gate–source voltage, as well as those limited in response below the cut-off frequency, whereas extrinsic elements extracted from circuits continuously scaling down the gate length, which leads to increased operation frequency, have made FET devices a critical technology in the design of mono-

lithic microwave integrated circuits (MMICs), where parasitic resistances, capacitances, and inductances that are often bias-independent are included to model the coupling effects and substrate losses, and the distributed effect at the gate channel and distributed the resistances are mainly caused by the lightly doped extensions of the drain and source diffusions, and are frequency-dependent [31].

The noise sources that are generated by the basic mechanisms responsible for the anomalous current flows can be correlated with the transient conduction mode described in Appendix A to provide insight into how noise would affect the bio-inspired conduction mode in the practical examples provided by Figures 6 and 7 as a function of physical quantities. To discover the interaction of the charge carriers (electrons and holes) from the surface region with the surface states and the bulk in the semiconductor, the shot noise can be produced by transient changes in drift and diffusion flows in the case of an FET, determined by the density of impurities $N_{TT} \sim 10^{10}$ cm^{-3} and/or defect centers within the depletion n-region, whereas the occupation of interface states would be determined by effective surface-state density $N_{SS} \sim 10^{12}$ cm^{-2} in the case of a MOSFET near the dielectric region, which can result in fluctuations in the channel conduction, giving rise to a flicker noise [32,33].

Because the equivalent circuits in Figure 1 link the device's physical structure to its circuit behavior, it allows us to predict the valid performance of the circuits at the proposed operating conditions; therefore, based on the physical quantities in Table A1, as described in Appendix A, the dominant operation mode for the practical examples corresponds to the nonlinear transient conduction, which satisfies at N_D^*, $N_A^* \geq N_{TT}$ in the case of an FET and $N_A^* X_{OX}$, $N_D^* X_{OX} \geq N_{SS}$ in the case of a MOSFET, attaining a reconfigurable behavior at room temperature during the reduced flow of dynamic charge $Q_F(t)$ and $Q_R(0)$ at medium-frequency range (<1 MHz), where input parasitic resistances and capacitances might be negligible in comparison with the dynamic physical parameters of Tables 1 and 2, as well as the inductor L > > gate–source parasitic inductances.

4. Conclusions

This research focused on frequency-dependent reconfiguration based on a bio-inspired conduction mode, analyzing its considerable dynamic properties, such as an exchange of energy between the inductor and the space-charge capacitances of an FET or MOSFET device to enable nonlinear transient conduction restricted by noise sources. As a result of applying intuition, physical analysis, and basic experiments, circuit architectures optimized for signal processing and size for easier dismantling and an extended time of operation have been proposed and validated in this work to overcome the practical circuits in the design of monolithic high-frequency integrated circuits using emerging materials and semiconductor technologies to achieve scalable solutions within a circularity-based paradigm change to support novel and feasible waste management processes in the electronics industry over the next few years.

Funding: This research received no external funding, and the APC was funded by the author.

Data Availability Statement: All of the manuscript is legible for readers, and the data in this manuscript are given in Appendix A. Lastly, the intention of the author is to motivate other researchers to explore new research routes by using similar methods documented here.

Acknowledgments: The research was supported in part by the National Council of the Science and Technology (CONACyT), Mexico. The experiments were possible thanks to the facilities provided by the technical personnel of the Electronics Laboratory, National Polytechnic Institute.

Conflicts of Interest: The author declares no conflict of interest.

Appendix A

Due to the dependence on transient charge in the gate–source junction, an FET or MOSFET device can follow the relationship $I_F \propto e^{q\Phi(mkT)}$ at forward bias and $I_R \propto 0$ at re-

verse bias; therefore, when $e^{q\Phi(mkT)} \gg 1$, its conduction state can be closely approximated by a function of the form

$$\ln \frac{I_F}{I_R} = \frac{q\Phi}{mkT}, \tag{A1}$$

where I_F is the forward current; I_R is the reverse saturation current; Φ is the built-in potential at the junction; k is the Boltzmann constant 8.82×10^{-5} eVK^{-1}; T is the temperature; and $m = \ln N_D^* N_A^* \left(n_i^{-2}\right)$ is the factor determining ratio of the donor, N_D^*, acceptor, and N_A^* ionized impurities [24,25].

Since the current–voltage characteristic in field-effect transistors has roughly an exponential behavior, a dynamic charge function $Q(\Phi)$ can be used to estimate the reconfigurable condition state during charge displacement. Substituting $I = dQ(dt)^{-1}$ and $C = dQ(d\Phi)^{-1}$ into (A1) and rewriting terms, the exponential form of the expression defining charge can be given by

$$Q_F(t) = Q_R(0) e^{\frac{qQ(\Phi)}{mkT}}, \tag{A2}$$

where $Q_F(t)$ is the dynamic forward diffusion charge, and $Q_R(0)$ is the dynamic reverse saturation charge under transient conduction when energy stored in the inductor was exchanged with space-charge capacitances varying with the gate voltage at zero time. To find a useful solution for $Q(\Phi)$ and $Q_R(0)$, methods to solve second-order linear differential equations must be applied:

The FET operating mode assumes that $Q_G = Q(\Phi)$; thus, solution for (2) must be written as follows:

$$Q_G(t) = C_{GS}\Phi_B \sin \frac{t}{\sqrt{LC_{GS}}}, \tag{A3}$$

while taking into account that $Q_G = Q_R(0)$, the solution of (3) is determined as below:

$$Q_R(0) = C_{GS}\Phi_B e^{-\frac{t}{r_{GS}C_{GS}}}, \tag{A4}$$

The solution of (4) and (6), in accordance with the two MOSFET operating modes with $Q_{G1} = Q_{G2} = Q(\Phi)$, can be written, respectively, as follows:

$$Q_1(\Phi) = C_{CH}V_T e^{-\frac{r_{CH}}{2L}t} \sin \frac{t}{\sqrt{LC_{CH}}}, \tag{A5}$$

$$Q_2(\Phi) = C_{GS}\Phi_S e^{-\frac{r_{GS}}{2L}t} \sin \frac{t}{\sqrt{LC_{GS}}}, \tag{A6}$$

while when $Q_{G1} = Q_{G2} = Q_R(0)$ at the two operating modes, the solution of (5) and (7) can be assumed as below, respectively.

$$Q_{R1}(0) = C_{GS}V_T e^{-\frac{t}{r_{GS}C_{GS}}}, \tag{A7}$$

$$Q_{R2}(0) = C_{CH}\Phi_S e^{-\frac{t}{r_{CH}C_{CH}}}, \tag{A8}$$

Substituting (A3) and (A4) into (A2) with m = 19.23, and substituting (A5) and (A7) into (A2) computed at m = 10.76, as well as (A6) and (A8) into (A2) computed at m = 9.61, satisfies the solution for $Q_F(t)$ with FET, $Q_{F1}(t)$, and $Q_{F2}(t)$ with MOSFET when the operation depends on the amount of ionized impurities. N_D^* and N_A^* correlate with the average dynamic charge, which is summarized in Table A1, when practical examples were operating at room temperature. The physical quantities involved in expressions from (A3) to (A8) are defined in Tables 1 and 2, respectively.

Table A1. Estimated physical quantities under transient conduction mode.

Device	N_D^* (cm^{-3})	N_A^* (cm^{-3})	Q_F (A-sec)	Q_R (A-sec)
2N5457	3.43×10^{13}	1.37×10^{15}	$\sim 5 \times 10^{-11}$	$\sim 6 \times 10^{-12}$
2N7000	4.96×10^{13}	1.98×10^{11}	$\sim 2 \times 10^{-9}$	$\sim 1.5 \times 10^{-10}$
	2.75×10^{13}	1.11×10^{11}	$\sim 5 \times 10^{-10}$	$\sim 2 \times 10^{-11}$

References

1. Theis, T.N.; Wong, H.-S.P. The end of Moore's law: A new beginning for information technology. *Comput. Sci. Eng.* **2017**, *19*, 41–50. [CrossRef]
2. Sauro, H.M.; Kim, K.H. It's an analog world. *Nature* **2013**, *497*, 572–573. [CrossRef]
3. Rozenberg, M.J.; Schneegans, O.; Stoliar, P. An ultra-compact leaky-integrate-and-fire model for building spiking neural networks. *Sci. Rep.* **2019**, *9*, 11123. [CrossRef]
4. Burr, G.W.; Sebastian, A.; Ando, T.; Haensch, W. Ohm's law + Kirchhoff's current law = Better AI: Neural-network processing done in memory with analog circuits will save energy. *IEEE Spectr.* **2021**, *58*, 44–49. [CrossRef]
5. A New Circular Vision for Electronic, Time for a Global Reboot. 2019. Available online: https://www.unep.org/news-and.stories/press-release/un-report-time-seize-opportunity-tackle-challenge-e-waste (accessed on 5 January 2023).
6. Chakraborty, M.; Kettle, J.; Dahiya, R. Electronic waste reduction through devices and printed circuit boards designed for circularity. *IEEE J. Flex. Electron.* **2022**, *1*, 4–23. [CrossRef]
7. Abad-Segura, E.; Fuente, A.B.D.L.; González-Zamar, M.D.; Belmonte-Ureña, L.J. Effects of circular economy polices on the environment and sustainable growth: Worldwide research. *Sustainability* **2020**, *12*, 5792. [CrossRef]
8. Martin, A.R.; Brown, D.A.; Diamond, M.E.; Cattaneo, A.; De-Miguel, F.F. *From Neuron to Brain*, 6th ed.; Sinauer Associates is an imprint of Oxford University Press: New York, NY, USA, 2020; pp. 25–150.
9. Kandel, E.; Koester, J.D.; Mack, S.H.; Siegelbaum, S. *Principles of Neural Science*, 6th ed.; McGraw-Hill: New York, NY, USA, 2021; pp. 190–211, 241–254.
10. Fitchen, F.C. *Transistor Circuit Analysis and Design*, 2nd ed.; D.Van Nostrand Company Inc.: Princeton, NJ, USA, 1967; pp. 122–136.
11. Liu, S.; Nagel, L.W. Small-signal MOSFET models for analog circuit design. *IEEE J. Solid-State Circuits* **1982**, *SC-17*, 983–998. [CrossRef]
12. Steckl, A.J. Circuits on cellulose. *IEEE Spectr.* **2013**, *50*, 48–61. [CrossRef]
13. Alimenti, F.; Palazzi, V.; Mariotti, C.; Mezzanotte, P.; Correia, R.; Borges Carvalho, N.; Roseli, L. Smart hardware for smart objects. *IEEE Microw. Mag.* **2018**, *19*, 48–68. [CrossRef]
14. Bishop, M.D.; Hills, G.; Srimani, T.; Lau, C.; Murphy, D.; Fuller, S.; Humes, J.; Ratkovich, A.; Nelson, M.; Shulaker, M.M. Fabrication of the carbon nanotube field-effect transistors in commercial silicon manufacturing facilities. *Nat. Electron.* **2020**, *3*, 492–501. [CrossRef]
15. Hosseini, E.S.; Dervin, S.; Ganguly, P.; Dahiya, R. Biodegradable materials for sustainable health monitoring devices. *ACS Appl. Bio. Matter.* **2021**, *4*, 163–194. [CrossRef] [PubMed]
16. Bressanelli, G.; Saccani, N.; Pigosso, D.C.A.; Perona, M. Circular economy in the WEEE industry: A systematic literature review and a research agenda. *Sustain. Prod. Consum.* **2020**, *23*, 174–188. [CrossRef]
17. Fogarassy, C.; Finger, D. Theoretical and practical approaches of circular economy for business models and technological solutions. *Resources* **2020**, *9*, 76. [CrossRef]
18. Minati, L.; Frasca, M.; Oświęcimka, P.; Faes, L.; Drożdż, S. Atypical transistor-based chaotic oscillators: Design, realization, and diversity. *Chaos Interdiscip. J. Nonlinear Sci.* **2017**, *27*, 073113. [CrossRef] [PubMed]
19. Fei, W.; Trommer, J.; Lemme, M.C.; Mikolajick, T.; Heinzig, A. Emerging reconfigurable electronic devices based on two-dimensional materials: A review. *InfoMat* **2022**, *4*, e12355. [CrossRef]
20. Chen, A.; Dietrich, K.-N.; Huo, X.; Ho, S. Developmental neurotoxicants in e-waste: An emerging health concern. *Environ. Health Perspect.* **2011**, *119*, 431–438. [CrossRef]
21. Baca-Arroyo, R. Synthesis of an aluminum oxide-based functional device engineered by corrosion/oxidation process. *Crystals* **2020**, *10*, 734. [CrossRef]
22. Baca-Arroyo, R. Recycled silicon waste as a sustainable energy material. In *Sustainable Materials for Next-Generation Energy Devices*, 1st ed.; Yew Cheong, K., Chen, L.-C., Eds.; Elsevier: Amsterdam, The Netherlands, 2021; pp. 359–373.
23. Grove, A.S. *Physics and Technology of Semiconductor Devices*, 1st ed.; John Wiley & Sons: New York, NY, USA, 1967; pp. 243–259, 317–333.
24. Sze, M.S.; NG, K.K. *Physics of Semiconductor Devices*, 3rd ed.; John Wiley & Sons, Inc.: New York, NY, USA, 2007; pp. 79–101, 293–328, 374–388.
25. Baca Arroyo, R. Unusual Operation of the Junction Transistor Based on Dynamical Behavior of Impurities. *Adv. Cond. Mater. Phys.* **2018**, *2018*, 4237686. [CrossRef]
26. Sedra, A.S.; Smith, K.C. *Microelectronics Circuits*, 5th ed.; Oxford University Press Inc.: New York, NY, USA, 2004; pp. 1042–1090.
27. Khalil, H.K. *Nonlinear Systems*, 1st ed.; Macmillan Publishing: New York, NY, USA, 1992; pp. 12–55.

28. Kennedy, M.P. Chaos in the Colpitts Oscillator. *IEEE Trans. Circuits Syst.* **1994**, *41*, 771–774. [CrossRef]
29. Furber, S. To build a brain. *IEEE Spectr.* **2012**, *49*, 45–49. [CrossRef]
30. Rosselló, J.L.; Canals, V.; Morro, A.; Oliver, A. Hardware implementation of stochastic spiking neural networks. *Int. J. Neural Syst.* **2012**, *22*, 1250014. [CrossRef] [PubMed]
31. Resca, D.; Raffo, A.; Santarelli, A.; Vannini, G.; Filicori, F. Scalable equivalent circuit FET model for MMIC design identified through FW-EM analyses. *IEEE Trans. Microw. Theory Tech.* **2009**, *57*, 245–253. [CrossRef]
32. Leach, W.M. Fundamentals of Low-Noise Analog Circuit Design. *Proc. IEEE* **1994**, *82*, 1515–1538. [CrossRef]
33. Das, M.B. FET Noise Sources and their Effects on Amplifier Performance at Low Frequencies. *IEEE Trans. Electron. Devices* **1972**, *19*, 339–348. [CrossRef]