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A Memristor-Based High-Resolution A/D Converter

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Abstract: Based on the voltage threshold adaptive memristor (VTEAM) model, this paper proposes a circuit design of a memristor-based A/D converter, which can achieve high-resolution conversion by simple configuration. For this A/D converter, there are the input voltage stage and the reference voltage stage in one conversion. According to the memristance change in the two stages, the input analog voltage is converted as the corresponding digital value. In the input voltage stage, the memristance increases from the initial memristance. Meanwhile, the counter rises its value from zero to the maximum. Next, the memristance returns to the initial memristance in the reference voltage stage. At the same time, the counting value starts to increase from zero again. Then, the input analog voltage is mapped to the eventual counting value of the reference voltage stage. The simulations of the memristor-based A/D converter demonstrate that it has good conversion performance. The proposed memristor-based A/D converter not only has more brilliant performance than the CMOS A/D converter, but also has the advantages over existing memristor-based A/D converters of anti-interference ability and high resolution.

Keywords: memristor-based A/D converter; memristor-based circuit design; VTEAM model; anti-interference performance

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1. Introduction

Analog-to-digital (A/D) converters are widely used in the modern electronic circuit, which is an important component in the information processing system. If an analog signal needs to be converted more precisely, the A/D converter should have high-resolution conversion ability [1,2].

In 1971, L. O. Chua proposed the memristor in theory [3]. HP labs manufactured the first physical memristor in 2008 [4]. The memristor can be manufactured to a nano-size, and it has non-volatility [5,6]. When the voltage is applied to the memristor, the memristance can be changed [7,8]. Furthermore, the memristor has the advantages on operating at high switching frequency, realizing large-scale parallel computing, etc. [9,10]. Owing to these merits, the memristor has been widely applied to the neuromorphic system [11,12], logic circuit [13–15], D/A and A/D converters [16,17], etc. [18,19].

The majority of physical memristors are voltage-controlled memristors [20,21]. When the voltage on the memristor is greater than the positive threshold voltage or is smaller than the negative voltage, the memristance will increase or decrease. Otherwise, the memristance stays unchanged. The voltage threshold adaptive memristor (VTEAM) model is a voltage-controlled memristor model that can match the behaviors of different memristors by changing the parameters [22–25].

Up to now, there are a few studies on the circuit design of memristor-based A/D converters. The Hopfield neural network is capable of converting analog signals to digital forms by configuring the network parameters to special values [26]. Because the memristor has changeable memristance, the memristor-based Hopfield neural networks are designed to accomplish A/D conversion [27,28]. In [29], the proposed memristor-based neural network is trained at first. Then, the trained network is applied to realize A/D conversion.

Based on the threshold feature of the memristor, combining the unilateral conductivity of diode, a memristor-based A/D converter is proposed in [30]. The threshold voltage of the memristor is used as the minimum distinguishable voltage of the A/D converter. Due to the non-volatility of the memristor, the memristor-based A/D converter can achieve the A/D conversion and the result storage synchronously.

Based on the excellent properties of memristor, a memristor-based D/A converter is proposed in [16]. Further, the memristor-based D/A converter is applied as the component to construct a successive approximation register A/D converter.

However, there are some deficiencies in the existing memristor-based A/D converters. For memristor-based Hopfield neural networks in [27,28], the A/D conversion is realized only if the memristors are arranged to accurate special values. This is difficult to implement in the manufacture. The memristor-based neural network in [29] must be trained before the A/D conversion. The training process is difficult to implement. Once the resolutions of the memristor-based A/D converters in [27–29] require change, the memristor-based neural networks must be configured or trained again. Because the resolution of the memristor-based A/D converter in [30] is decided by the threshold voltage of the memristors, the resolution cannot be arranged. Moreover, the conversion result of the memristor-based A/D converter will become inaccurate when the threshold voltage of the memristors changes along with the operation. The memristor-based A/D converters in [27–30] are susceptible to noises.

Based on the VTEAM model, this paper proposes the circuit design of memristor-based A/D converter, which has good conversion performance. Compared with the memristor-based circuits in [27–30], the proposed memristor-based A/D converter can easily realize high-resolution conversion by setting the bits of the counter. Meanwhile, the proposed memristor-based A/D converter has good anti-interference performance. Compared with A/D converters in [27–29], the memristor in the proposed memristor-based circuit can be arranged to random memristance in the manufacture, simplifying the fabrication process. Compared with the COMS dual-slope A/D converter, the proposed memristor-based A/D converter has a simpler circuit structure and timing.

The rest of the paper is organized as follows. Section 2 presents the circuit design and the conversion process of the memristor-based A/D converter. Section 3 shows the circuit simulations to prove the performance of the memristor-based A/D converter. The anti-interference of the memristor-based A/D converter is presented in Section 4. Section 5 presents the comparisons between the A/D converters. Conclusions are drawn in Section 6.

2. The Memristor-Based A/D Converter

2.1. Circuit Implementation of the Memristor-Based A/D Converter

The most physical memristors are voltage-controlled memristors. The VTEAM model is a general voltage-controlled memristor model [22]. The VTEAM model is given by

$$\frac{dw(t)}{dt} = \begin{cases} k_{off}\left(\dfrac{v(t)}{v_{off}} - 1\right)^{a_{off}}, & \text{if } 0 < v_{off} < v \quad (1a) \\ 0, & \text{if } v_{on} < v < v_{off} \quad (1b) \\ k_{on}\left(\dfrac{v(t)}{v_{on}} - 1\right)^{a_{on}}, & \text{if } v < v_{on} < 0 \quad (1c) \end{cases}$$

$$R_m(t) = R_{on} + \frac{R_{off} - R_{on}}{w_{off} - w_{on}}(w(t) - w_{on}) \quad (2)$$

where $R_m(t)$ represents memristance, and R_{on} and R_{off} denote the minimum and maximum memristance, respectively. w_{on} and w_{off} are the bounds of the internal state variable, and v_{on} and v_{off} represent the negative threshold voltage and the positive threshold voltage, respectively. k_{on}, k_{off}, a_{on}, and a_{off} are constant parameters.

The schematic diagram of the proposed memristor-based A/D converter is shown in Figure 1, in which V_i is the analog input voltage and $-V_{ref}$ is the negative permanent reference voltage. The resistors R_1, R_2, RN_1, RN_2, and operational amplifier $A1$ constitute a subtracting circuit, obtaining the difference between V_i and $\frac{-V_{ref}}{2}$. The output voltage of $A1$ can be represented as

$$V_{A1} = (1 + \frac{RN_1}{R_1})(\frac{\frac{RN_2}{R_2}}{1 + \frac{RN_2}{R_2}}) \times (V_i) - \frac{RN_1}{R_1} \times (-V_{ref}) \quad (3)$$

When the resistance of RN_1 is one half of R_1's resistance, and the resistance of RN_2 is twice that of R_2's resistance, Equation (3) can be simplified as

$$V_{A1} = V_i + \frac{1}{2}V_{ref} \quad (4)$$

Either the output of $A1$ or the reference voltage is linked to the memristor R_m through the selector switch S_1. Because the output of $A1$ should be larger than the positive threshold voltage v_{off} to increase the memristance, the input voltage to be converted must be greater than $\frac{-V_{ref}}{2} + v_{off}$.

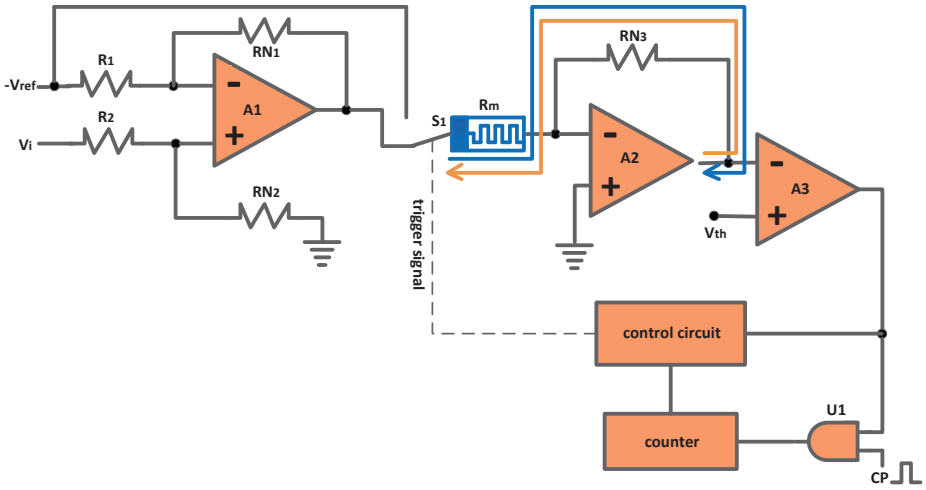

Figure 1. The schematic diagram of the memristor-based A/D converter.

Memristor R_m, resistor RN_3, and operational amplifier $A2$ constitute an inverting amplifying circuit. Due to *virtual ground*, the voltage at inverting terminal of $A2$ is 0 V. When the output of $A1$ is linked to the memristor, the current flows to the inverting terminal of $A2$, making the memristance rise. The corresponding current path is presented as the blue line in Figure 1.

Alternatively, when $-V_{ref}$ is connected to the memristor, the current flows from the output terminal of $A2$, through RN_3 and R_m, to $-V_{ref}$. Therefore, the memristance reduces. The orange line in Figure 1 shows the corresponding current path.

The output of $A2$ connects to the inverting terminal of the comparator $A3$. The comparator $A3$ generates the corresponding digital logic signal to enable or disable the AND gate U_1. If the output of $A3$ is *logic* 1, the AND gate U_1 is enabled. Then, the digital clock source CP serves as the counting clock of the counter. The output of the counter returns to the control circuit to generate the trigger signal, controlling the selector switch S_1.

Compared with the CMOS dual-slope A/D converter, the proposed memristor-based A/D converter in this paper has a more compact control circuit structure, and has the simpler control timing [31,32]. Compared with the memristor-based A/D converter in [17], the proposed A/D converter in this paper adopts the VTEAM model to construct the circuit.

The VTEAM model can match a number of voltage-controlled physical memristors, so the proposed A/D converter has the more flexible application potential.

2.2. Inference of Conversion Result

For the proposed memristor-based A/D converter, one conversion contains two stages: input voltage stage (IVS) and reference voltage stage (RVS). In IVS, the count value is reset to zero firstly. The analog input voltage V_i adds $\frac{V_{ref}}{2}$ to obtain the output of $A1$, V_{A1}. Then, the selector switch S_1 connects V_{A1} to the memristor to raise the memristance. Because V_{A1} is a positive voltage, the output of $A2$ is a negative voltage

$$V_{A2}(t) = -\frac{RN_3 V_{A1}}{R_m(t)} \tag{5}$$

where $R_m(t)$ denotes the memristance of R_m. The threshold voltage of the comparator V_{th} is positive, which is larger than $V_{A2}(t)$. Thus, AND gate U_1 is enabled.

According to the digital clock source CP, the counting value increases from zero to the maximum M_c in IVS. The duration of IVS can be represented as

$$T_c = M_c \cdot T_s \tag{6}$$

where T_s is the cycle of CP. Once the counting value attains the maximum M_c, IVS finishes. Then, the memristor-based A/D converter enters RVS.

During RVS, the reference voltage $-V_{ref}$ is connected to the memristor. The voltage across the memristor is negative. Thus, the memristance decreases. Due to the connection of the negative voltage $-V_{ref}$, the output of $A2$ hops to a positive voltage at the start of RVS

$$V_{A2}(t) = \frac{V_{ref} RN_3}{R_m(t)} \tag{7}$$

In the beginning, the threshold voltage of the comparator V_{th} is still larger than the output voltage of $A2$, $V_{A2}(t)$. Hence, the AND gate U_1 remains enabled. Accordingly, the counter begins counting from zero again. The memristance reduces and $V_{A2}(t)$ increases in RVS. When $V_{A2}(t)$ rises to be equal to V_{th}, the comparator outputs a low level afterwards. Then, the AND gate U_1 is disabled. The counting stops, and the conversion comes to the end. The duration of RVS is given by

$$T_d = M_d \cdot T_s \tag{8}$$

where M_d is the eventual counting value of RVS. At the end of the conversion, $V_{A2}(t)$ is equal to V_{th}. In accordance with (7), the memristance at the end of the conversion R_{mf} can be deduced as

$$R_{mf} = \frac{V_{ref} RN_3}{V_{th}} \tag{9}$$

In the proposed memristor-based A/D converter, the reference voltage, the threshold voltage of the comparator V_{th}, and the resistance of RN_3 are fixed parameters. Accordingly, R_{mf} is a definite constant. At the end of every conversion, the memristance returns to R_{mf}. At the same time, R_{mf} is the initial memristance of the next conversion. Due to the non-volatility of memristor, the eventual memristance R_{mf} remains, even if the power turns off.

In one conversion, the memristance rises from the initial memristance R_{mf} to a value marked as R_{md} in IVS, and then it reduces from R_{md} to R_{mf} in RVS. The increment and decrement of the memristance are the same in the two stages.

V_{A1} is linked to the memristor in IVS to increase the memristance with T_c. The increment of the memristance in T_c is the total influence of V_{A1}. If V_{A1} is a varying voltage

in IVS, the effect of V_{A1} can be equivalent to that of V_{A1}'s average voltage. Therefore, the conversion obtains the average voltage of V_{A1} in IVS, V_{rg1}.

If the analog input signal V_i has mixed the sine noise, white Gaussian noise, or other zero-mean noises, the influence of the noise signals is weakened greatly by the average function in IVS. As a consequence, the proposed memristor-based A/D converter has good anti-interference performance to zero-mean noises. Nevertheless, the conversion results of the memristor-based A/D converters in [27–30] are susceptible to noises.

The reference voltage $-V_{ref}$ is connected to the memristor in RVS. The v_{on}, v_{off}, k_{on}, k_{off}, a_{on}, and a_{off} are constant parameters in the VTEAM model. Furthermore, V_{rg1} and $-V_{ref}$ are fixed voltages. Under the influence of V_{rg1} and $-V_{ref}$, the VTEAM model is simplified as

$$\frac{dw(t)}{dt} = \begin{cases} b_1, & \text{if } 0 < v_{off} < v \quad (10a) \\ 0, & \text{if } v_{on} < v < v_{off} \quad (10b) \\ b_2, & \text{if } v < v_{on} < 0 \quad (10c) \end{cases}$$

Accordingly, (10) can be solved as

$$w(t) = \begin{cases} b_1 t + w_s, & \text{if } 0 < v_{off} < v \quad (11a) \\ w_s, & \text{if } v_{on} < v < v_{off} \quad (11b) \\ b_2 t + w_s, & \text{if } v < v_{on} < 0 \quad (11c) \end{cases}$$

where w_s represents the initial state variable. Thus, the memristance change can be represented as

$$R_m(t) = \begin{cases} R_s + \dfrac{R_{off} - R_{on}}{w_{off} - w_{on}}(b_1 t - w_{on}), & \text{if } 0 < v_{off} < v \quad (12a) \\ R_s, & \text{if } v_{on} < v < v_{off} \quad (12b) \\ R_s + \dfrac{R_{off} - R_{on}}{w_{off} - w_{on}}(b_2 t - w_{on}), & \text{if } v < v_{on} < 0 \quad (12c) \end{cases}$$

where R_s represents the initial memristance.

In IVS, affected by V_{A1}, the memristance increases from R_{mf} to R_{md} during T_c

$$R_{md} = R_{mf} + \frac{R_{off} - R_{on}}{w_{off} - w_{on}}(b_1 T_c - w_{on}) \quad (13)$$

In RVS, under the influence of the reference voltage $-V_{ref}$, the memristance reduces from R_{md} to R_{mf} during T_d

$$R_{mf} = R_{md} + \frac{R_{off} - R_{on}}{w_{off} - w_{on}}(b_2 T_d - w_{on}) \quad (14)$$

The relation between T_c and T_d can be inferred by associating (13) and (14)

$$-b_1 T_c = b_2 T_d \quad (15)$$

Combining the presentation in (1), Equation (15) can be rewritten as

$$k_{off}\left(\frac{V_{rg1}}{v_{off}} - 1\right)^{a_{off}} T_c = -b_2 T_d \quad (16)$$

Then, V_{rg1} can be obtained by solving (16)

$$V_{rg1} = \left(\sqrt[a_{off}]{-\frac{b_2 T_d}{k_{off} T_c}} + 1\right) v_{off} \quad (17)$$

V_{rg1} is the average voltage of V_{A1} in IVS. The average voltage of V_i in IVS is marked as V_{rg}. Thus, V_{rg} can be represented as

$$V_{rg} = \left(\sqrt[a_{off}]{-\frac{b_2 T_d}{k_{off} T_c}} + 1 \right) v_{off} - \frac{1}{2} V_{ref} \tag{18}$$

As we can see in (18), the conversion result is the average voltage of the analog input voltage. Hence, the proposed memristor-based A/D converter is suitable to convert the input signal that changes relatively slowly. Then, the conversion result can reflect to the analog input voltage effectively.

As shown in (18), T_c, v_{off}, k_{off}, a_{off}, b_2 and $-V_{ref}$ are constant parameters. Hence, the conversion result is determined by the counting value T_d. In order to ensure the correctness of the conversion result, T_d must be less than the maximum counting value. In accordance with (16), when T_d is less than the maximum counting value, the parameters of the memristor-based A/D converter must satisfy

$$-k_{off} \left(\frac{V_{rg1}}{v_{off}} - 1 \right)^{a_{off}} < k_{on} \left(\frac{-V_{ref}}{v_{on}} - 1 \right)^{a_{on}} \tag{19}$$

Based on the presentation in (19), the analog input voltage range can be calculated when the parameters of memristor and the reference voltage are selected.

According to the previous analysis, the conversion result is decided by the eventual counting value T_d. If the counter is arranged to different bits, the resolution of the proposed memristor-based A/D converter is adjusted accordingly. For instance, the 16-bit counter indicates that the resolution is 16 bits while the 12-bit counter corresponds to 12-bit resolution. Therefore, the proposed memristor-based A/D converter can achieve high-resolution conversion easily.

However, the memristor-based A/D converter in [30] is unchangeable. Additionally, the conversion result in [30] becomes unreliable when the threshold voltage of the memristors changes along with the usage. The memristor-based A/D converters in [27–29] are difficult to realize high-resolution conversion, because the tremendous parameter configurations or computations are required to make the memristor-based neural networks converge to correct digital states. The memristor-based A/D converters in [27–30] are vulnerable to noises.

3. Simulations of the Memristor-Based A/D Converter

The simulations of the proposed memristor-based A/D converter with different parameters are implemented on SIMULINK to demonstrate the conversion performance. The simulations are fulfilled with four different parameters, which are shown in Table 1. Although the parameters of the memrsitor are arranged to different values, the conversion results of the input voltage 1V are the same. These simulations demonstrate that the conversion results of the proposed memristor-based A/D converter are not affected by the different parameter settings of the memristor.

In the simulations, the initial memristance is 45 kΩ. The counter is 16 bits, which indicates that the resolution of the A/D converter is 16 bits. The frequency of the digital clock source is set as 2 MHz. The input voltage to be converted is 1 V, while the reference voltage is −6 V.

In the fourth simulation, the parameter settings of a_{on} and a_{off} are 3 and 2. The threshold voltage of the comparator V_{th} is 3.5 V. The resistance of R_{N3} is 26 kΩ. Hence, based on the relation presented in (9), the initial memristance R_{mf} is 44.571 kΩ.

Table 1. The parameter settings of the memristor.

-	First Simulation	Second Simulation	Third Simulation	Fourth Simulation
$R_{on}(\Omega)$	1000	1000	1000	1000
$R_{off}(\Omega)$	100,000	100,000	100,000	100,000
w_{off}(m)	3×10^{-9}	3×10^{-9}	3×10^{-9}	3×10^{-9}
w_{on}(m)	0	0	0	0
k_{off}(m/s)	5×10^{-9}	2×10^{-9}	6×10^{-10}	2×10^{-9}
k_{on}(m/s)	-5×10^{-9}	-2×10^{-9}	-6×10^{-10}	-3.4×10^{-10}
v_{off}(V)	0.8	1	1	1
v_{on}(V)	−0.8	−1	−1	−1
a_{off}	1	2	3	2
a_{on}	1	2	3	3
a_{init}(m)	1.38×10^{-9}	1.38×10^{-9}	1.38×10^{-9}	1.38×10^{-9}
conversion result (1 V)	0.999 V	0.999 V	0.999 V	0.999 V

The memristance variation and the output voltage change in the fourth simulation are shown in Figure 2. The fourth simulation includes three conversions. *Conversion X* is invalid, while *conversions* 1 and 2 are effective. Because the arranged initial memristance 45 kΩ is not equal to the effective initial memristance 44.571 kΩ, the memristor-based A/D converter requires the transitional *conversion X* to enter the effective conversions.

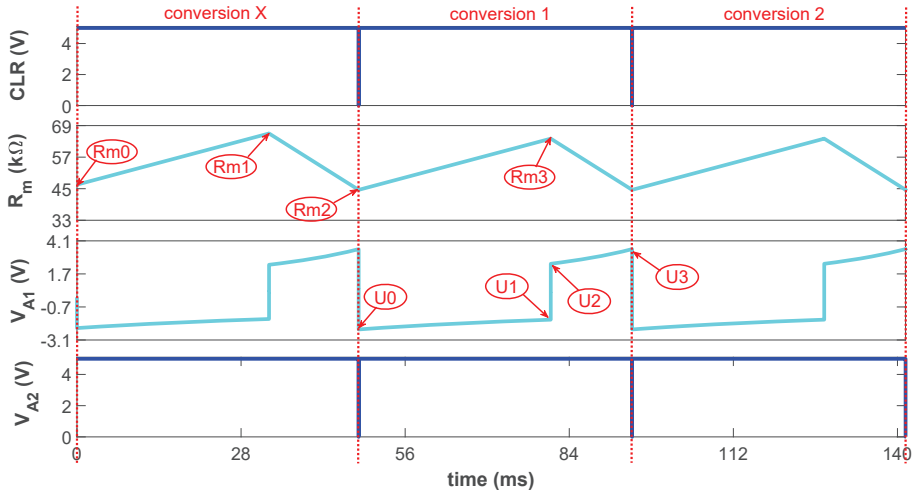

Figure 2. The memristance variation and the output voltage change in the fourth simulation.

In *conversion X*, the input voltage is applied to the memristor-based A/D converter in IVS. Accordingly, the memristance begins to increase from the arranged initial memristance 45 kΩ, which is marked as R_{m0} in Figure 2. The counting value rises from 0 to the maximum. Thus, the IVS lasts 32.768 ms, and the memristance increases from R_{m0} to R_{m1}.

In RVS of *conversion X*, the reference voltage −6 V is connected to the memristor-based A/D converter. The counting value increases from 0 again and the memristance decreases from R_{m1}. When the memristance reduces to the effective initial memristance 44.571 kΩ, which is marked as R_{m2} in Figure 2, the *conversion X* goes to the end. Relying on the invalid transition *conversion X*, the proposed memristor-based A/D converter adjusts to the effective transformation. Then, the memristor-based A/D converter begins to convert the analog input signal validly. Because the memristor is nonvolatile, the valid memristance R_{m2} remains, even though the power supply turns off.

At the beginning of *conversion* 1, the *CLR* signal resets the counter to zero. In the IVS of *conversion* 1, the memristance increases from R_{m2} to R_{m3}. At the same time, V_{A2} rises from U_0 to U_1. Next, it enters the RVS of *conversion* 1. The reference voltage is linked into the memristor-based A/D converter immediately. Therefore, V_{A2} hops to U_2. The

memristance decreases from R_{m3} to R_{m2}, and V_{A2} increases to U_3 in RVS. The memristance variation and the output voltage change in *conversion* 2 are same as those in *conversion* 1. The conversion results of *conversions* 1 and 2 are 0.999 V.

Based on the previous analysis, we can see that the proposed memristor-based A/D converter can adjust to the effective conversion depending on the transitional transformation when the memristance is not manufactured to the accurate 44.571 kΩ. Further, if the memristor is fabricated to the arbitrary memristance in the manufacture, the memristor-based A/D converter also can automatically proceed to the available conversion by the invalid transformations. In the condition that the memristance is manufactured to approach the minimum, the IVS becomes the dominant factor in the ineffective transformations to continuously increase the memristance. After several invalid conversions, the memristance increases to the effective initial memristance 44.571 kΩ. On the other hand, when the memristance is fabricated to near the maximum, the RVS dominantly affects the ineffective conversions, making the memristance reduce to 44.571 kΩ.

However, for the memristor-based Hopfield neural networks in [27,28], only when all the memristors are manufactured to the accurate memristance can the correct conversion be realized. Thus, the manufacture process is complicated.

Further, the analog input voltage is arranged to different values in the input voltage range. Then, a great number of simulations are implemented with the different analog input voltages to prove the conversion performance of the memristor-based A/D converter. Applying the final counting values of the conversions as the x axis, the corresponding conversion results that are computed by (18) are utilized as the y axis to obtain the fitting conversion curve of the simulations, which is presented as red in Figure 3. Moreover, the ideal conversion curve marked as blue is also presented in Figure 3. As we can see, the conversion curve of the simulations almost superposes the ideal conversion curve. Consequently, the conversion results of the simulations demonstrate that the memristor-based A/D converter has good transformation performance.

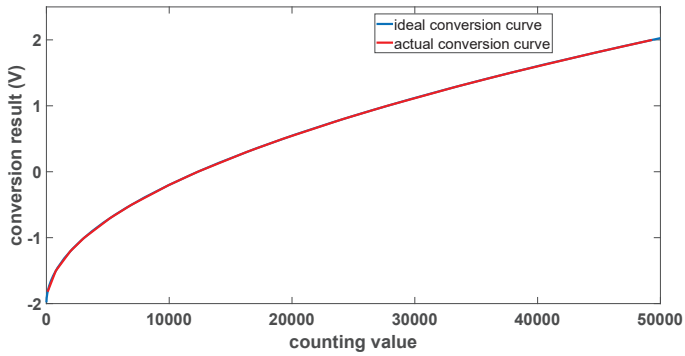

Figure 3. The conversion curve of the memristor-based A/D converter.

4. Anti-Interference Performance of the Memristor-Based A/D Converter

The conversion result of the memristor-based A/D converter is the average voltage of the input signal. If the zero-mean noise is superposed on the actual analog input signal to be the input signal, the influence of the noise is weakened effectively. Thus, the memristor-based A/D converter has the ability to prevent the interference of the zero-mean noise.

The memristor-based A/D converter is simulated on SIMULINK to prove the anti-interference performance. In the simulation, the sine noise whose amplitude is 1 V is superposed to the 0 V actual analog voltage, acting as the input voltage. The frequency of the sine noise is 300 Hz. The counter is arranged as 16 bits, and the frequency of the counting clock source is 2 MHz. Hence, the IVS lasts 32.768 ms. Ten cycles of the sine noise last 33.33 ms, which approaches the duration of the IVS. Then, the mean of the sine noise in IVS is close to zero, and the influence of the sine noise is notably weakened. The memristance change and the output variation under the input voltage with sine noise are presented in Figure 4.

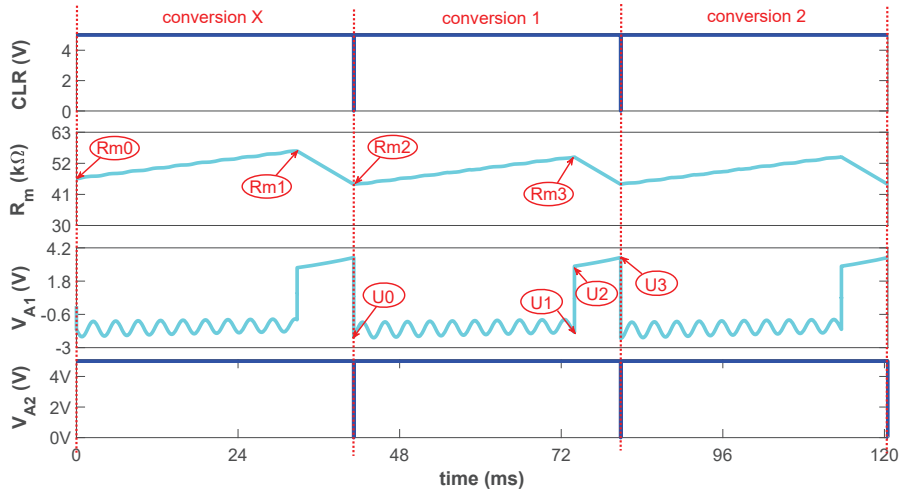

Figure 4. The memristance variation and the output voltage change under the input voltage with sine noise.

There are three conversions in Figure 4. The memristor-based A/D converter begins to convert the input signal effectively depending on the invalid transformation *conversion X*. *Conversion* 1 is effective, and the initial memristance of IVS is Rm_2. The memristance at the end of IVS is Rm_3. Affected by the input signal with sine noise, the increase in the memristance has little fluctuations. Because the input signal is sine voltage, combining with the variation of the memristance, the output voltage of amplifier A1 presents an analog sine change in IVS. According to (19), the conversion result is calculated as 0.109 V.

Then, the sine noises whose amplitudes change within 0.2–1.2 V are added to the actual 0 V analog voltage to implement the simulations. The interval of the sine noises' amplitude is 0.2 V. The corresponding conversion results are given in Table 2. As we can see in the table, the corresponding conversion results indicate that the influences of the sine noises are shortened notably.

Table 2. The conversion results of the 0 V analog voltage with the sine noises.

the Amplitude and Frequency of Sine Noise	Actual Analog Voltage	the Amplitude of Input Voltage	Conversion Result
0.2 v (300 Hz)	0 v	0.2 v	0.003 v
0.4 v (300 Hz)	0 v	0.4 v	0.018 v
0.6 v (300 Hz)	0 v	0.6 v	0.039 v
0.8 v (300 Hz)	0 v	0.8 v	0.067 v
1.0 v (300 Hz)	0 v	1 v	0.109 v
1.2 v (300 Hz)	0 v	1.2 v	0.165 v

Further, the actual analog voltage is arranged as 1 V. The different sine noises are superposed to the 1 V analog voltage to implement the more simulations. The frequency of these sine noises is 3000 Hz and the amplitudes of these sine noises also change within 0.2–1.2 V. The corresponding conversion results are shown in Table 3, which demonstrate that the effects of these sine noises are weakened validly.

As shown in the previous simulations, as long as the duration of IVS is arranged to approach the cycles of the sine noises, even though the sine noises have different amplitudes and frequencies, the influences of the sine noises have been shortened notably. This proves that the proposed memristor-based A/D converter has good anti-interference ability to prevent the zero-mean noises. However, the memristor-based A/D converters in [27–30] are susceptible to noises.

Table 3. The conversion results of the 1 V analog voltage with the sine noises.

the Amplitude and Frequency of Sine Noise	Actual Analog Voltage	the Amplitude of Input Voltage	Conversion Result
0.2 v (3000 Hz)	1 v	1.2 v	1.004 v
0.4 v (3000 Hz)	1 v	1.4 v	1.014 v
0.6 v (3000 Hz)	1 v	1.6 v	1.036 v
0.8 v (3000 Hz)	1 v	1.8 v	1.057 v
1.0 v (3000 Hz)	1 v	2 v	1.086 v
1.2 v (3000 Hz)	1 v	2.2 v	1.123 v

5. Discussion

Compared with the existing memristor-based A/D converters and the CMOS dual-slope A/D converter, the proposed memristor-based A/D converter has the advantages of different aspects. The corresponding comparisons are shown in Table 4.

Table 4. The comparisons of the A/D converters.

-	Circuit Structure	Timing	High Resolution	Memristor Manufacture	Anti-Interference Ability	Voltage-Controlled Memristor
[27,28]	-	-	no	complex	no	yes
[29]	-	-	no	simple	no	yes
[30]	-	-	no	complex	no	yes
[31,32]	complex	complex	yes	-	yes	-
[16]	-	-	yes	simple	no	yes
[17]	simple	simple	yes	simple	yes	no
this paper	simple	simple	yes	simple	yes	yes

For the CMOS dual-slope A/D converter [31,32], it must discharge the capacitor at the beginning of every conversion. Then, it needs the corresponding control circuit to manage the discharging timing. However, the proposed memristor-based A/D converter does not require this discharging operation. Therefore, the proposed circuit has the simper circuit structure and timing.

The memristor-based A/D converters in [27,28] must manufacture the memristors to accurate values while the memristor in the proposed circuit can be manufactured to a random value. Hence, the manufacture of the memristor in this paper is simple. For the memristor-based A/D converters in [27–29], they are difficult to realize high resolution because there will be a large number of parameters to be configured or trained. When the input signal mixes in noises, the noises can make the memristor-based neural networks in [27–29] converge to incorrect digital values.

The resolution of memristor-based A/D converters in [30] is unchangeable. Meanwhile, the threshold voltage of the memristors must be manufactured to be strictly equal. Thus, the manufacture of the memristors is complex. If noises are mixed into the input signal, the memristors can be changed to a false state, generating the wrong conversion result. Compared with the memristor-based A/D converters in [27–30], the proposed circuit in this paper has good anti-interference ability to prevent zero-mean noises. The memristor-based circuit design in [30] utilizes the HP memristor model to fulfill the conversion. However, this paper adopts the VTEAM model, which is a voltage-controlled memristor model. A majority of physical memristors are voltage-controlled memristors. Hence, the proposed memristor-based A/D converter in this paper has the more extensive application potential.

The CMOS successive approximation register (SAR) A/D converter and the CMOS dual-slope A/D converter are two high-resolution A/D converters. Meanwhile, the SAR A/D converter can convert the analog signals relatively fast. However, the SAR A/D converter does not have anti-interference ability. Hence, the SAR A/D converter and the CMOS dual-slope A/D converter are applied to different occasions [31,32]. Accordingly,

the memristor-based SAR A/D converter in [16] and the proposed memristor-based A/D converter in this paper also have different application occasions.

6. Conclusions

The A/D converter plays an important role in the modern circuit. This paper proposes a novel memristor-based high-resolution A/D converter in which one conversion contains IVS and RVS. Then, the memristance variation and the output voltage change are analyzed to illustrate the A/D conversion process. At the same time, the relation between the input voltage and the digital counting value is inferred according to the circuit parameter changes. The memristor-based A/D converter is simulated on SIMULINK to prove the performance. Under different parameter settings, a great number of simulations are implemented to obtain the conversion curve of the memristor-based A/D converter. Further, the memristor-based A/D converter is analyzed and simulated to prove its anti-interference ability for zero-mean noise. The comparisons between the proposed memristor-based A/D converter and the existing A/D conversion circuits are also presented to demonstrate the advantages of the proposed circuit. Implementing the proposed memristor-based A/D converter with real memristors will be studied in the future.

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