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Voltage Multiplier with High Input/Output Voltage Gain from Center-Tap Rectifier-Voltage Tripler and Quadrupler

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Abstract: This paper proposes new rectifiers in the center-tap transformer to provide higher input/output (I/O) voltage gain with an equal transformer turns-ratio in the LLC resonant converter: a voltage tripler rectifier and a voltage quadrupler rectifier, which have simple structures with one capacitor and two diodes, and three and four times higher I/O voltage gain than a center-tap rectifier, respectively. Each rectifier is compared in terms of the transformer turns-ratio and the magnetizing offset current, and the voltage and current stresses in the capacitors and diodes. The validity of these proposed rectifiers in the half-bridge (HB) LLC resonant converter is confirmed by the experimental results from a 100 V/200 W output prototype.

Keywords: LLC resonant converter; quadrupler rectifier; tripler rectifier; doubler rectifier; high step-up gain

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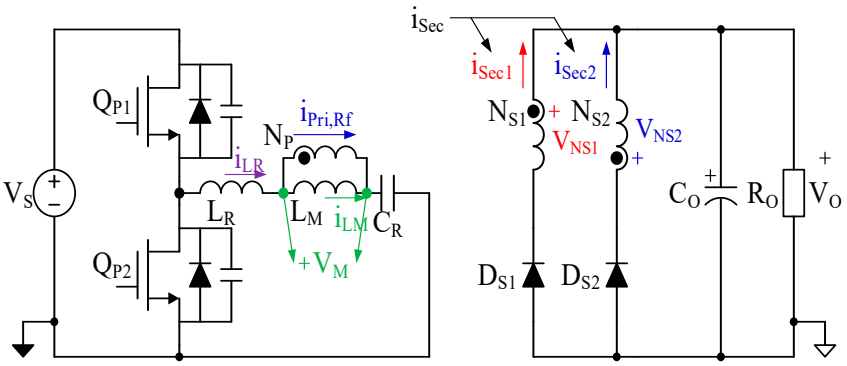
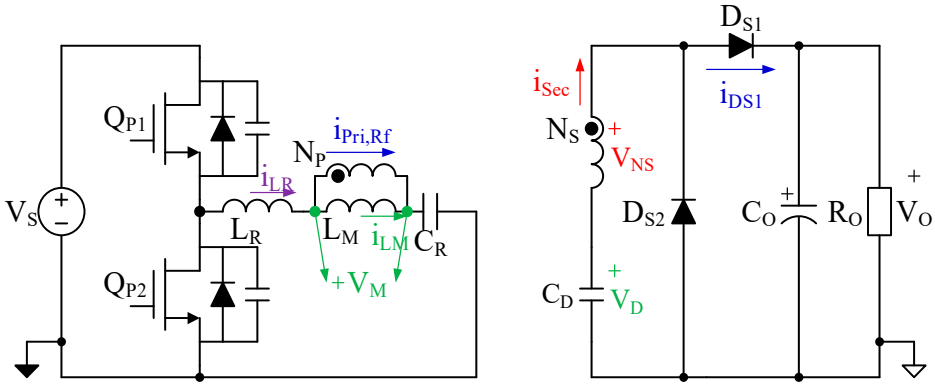
1. Introduction

The center-tap rectifier (CTR) without an output inductor is widely used in many switching converters in low output-voltage and high output-current applications, since it has a simple structure, low voltage stresses, and small conduction losses resulting from two diodes in the secondary side. The asymmetric/symmetric half-bridge (HB) and full-bridge (FB) converters with pulse-width modulation (PWM) control and resonant converters with pulse-frequency modulation (PFM) control normally adopt the CTR for the DC/DC power conversion. The CTR has many advantages, such as a simple structure, low component count, and flexibility in designing an asymmetric turns-ratio between the secondary turns. However, it has a limitation in making high input/output (I/O) voltage gain, due to a disadvantageous transformer turns-ratio. For example, if an HB LLC resonant converter, as shown in Figure 1a, operates in a resonant region, the voltage (V_M) on the magnetizing inductor (L_M) of the center-tap transformer is half of the input voltage ($V_S/2$), and is transferred to the output (V_O) through the transformer turns-ratio (n), i.e., $V_O = V_S/(2n)$, i.e., $n = N_P/N_S$.

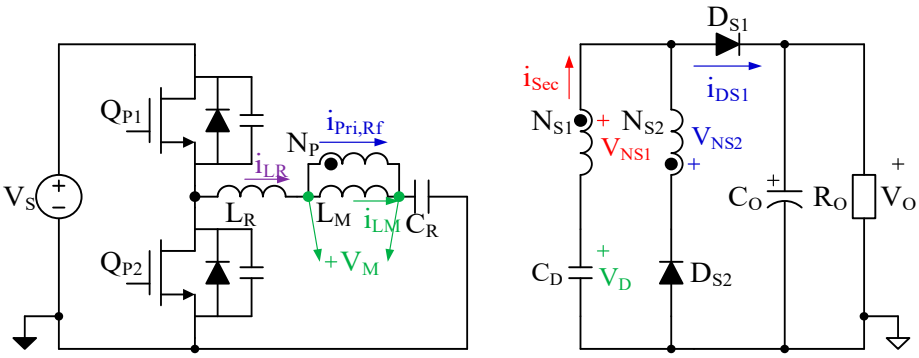
To relieve this drawback, the voltage doubler rectifier (VDR) in Figure 1b is frequently used in many applications requiring a higher transformer turns-ratio (n). For example, if an HB LLC resonant converter with the VDR operates in a resonant region, the voltage (V_M) on the magnetizing inductor (L_M) of the transformer with the VDR is half of the input voltage ($V_S/2$), and is transferred to the voltage (V_D) on a doubler capacitor (C_D) through the transformer turns-ratio (n), i.e., $V_D = V_S/(2n)$. Since the output voltage (V_O) is the sum of V_D and the voltage (V_{NS}) across the secondary turn (N_S), i.e., $V_{NS} = V_S/(2n)$ and $V_O = V_D + V_{NS}$, V_O is V_S/n, which means that n can be doubled, compared with the center-tap transformer in Figure 1a.



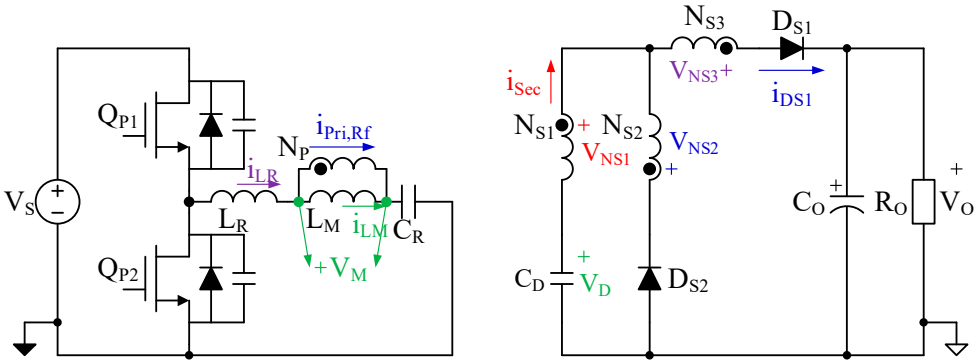
(**a**) Conventional center-tap rectifier.



(**b**) Conventional voltage doubler rectifier.



(**c**) Proposed voltage tripler rectifier.



(**d**) Proposed voltage quadrupler rectifier.

Figure 1. Circuit diagram of conventional and proposed rectifiers.

In addition, there are several approaches to obtain a higher I/O voltage gain [1–8]. Table 1 shows comparisons with "prior arts." In column [1] of Table 1, the HB LLC resonant converter can achieve a higher I/O voltage gain by increasing the transformer secondary turns. However, it utilizes one additional diode and switch, and additional transformer secondary windings, which cause circuit complexity. Moreover, in the mode of increasing I/O voltage gain, the offset current in the transformer occurs due to the primary unbalanced current, which results from only one powering operation in the secondary side. The offset current in the transformer causes the size of the transformer to be increased. In column [2] of Table 1, the HB LLC converter with a boost pulse-width modulation (PWM) control method is proposed. In the mode of increasing I/O voltage gain, the added switch is turned on or off with PWM control. While the added switch is turned on, the energy stored in the resonant capacitor (C_r) is stored in the resonant inductor (L_r) by the resonance between L_r and C_r. Meanwhile, if the added switch is turned off, the energy stored in L_r is transferred to the output through the transformer; thus, a higher I/O voltage gain can be obtained. However, one additional switch is needed, and the additional switch cannot be clamped due to the leakage inductor of the transformer, which has high voltage stress. Moreover, as in column [1] in Table 1, the offset current in the transformer occurs due to the primary unbalanced current, which results from only one powering operation in the secondary side. This increases the transformer size. In column [3] of Table 1, the HB LLC converter with the asymmetric PWM control method is proposed. This paper does not consider additional devices in order to obtain higher I/O voltage gain. However, in a situation of obtaining higher I/O voltage gain, asymmetric PWM control is used. Since it causes "only one powering operation during small duty-cycle" in one switching period, the primary current becomes unbalanced; thus, the offset current in the transformer occurs. The offset current in the transformer causes the size of the transformer to be increased, similar to [1,2].

Table 1. Comparisons with prior arts.

	[1]	[2]	[3]	[4]	[5]
Semiconductor Devices	Switch: 3EA Diode: 3EA Inductor: 1EA Capacitor: 1EA Total: 8EA	Switch: 3EA Diode: 4EA Inductor: 1EA Capacitor: 1EA Total: 9EA	Switch: 2EA Diode: 2EA Inductor: 1EA Capacitor: 1EA Total: 6EA	Switch: 3EA Diode: 3EA Inductor: 1EA Capacitor: 1EA Total: 8EA	Switch: 3EA Diode: 4EA Inductor: 2EA Capacitor: 2EA Total: 11EA
Transformer Offset-Current	Exist	Exist	Exist	None	None
Additional Control	On/Off Control	PWM Control	PWM Control	On/Off Control	On/Off/PWM Controls
	[6]	[7]	[8]	Proposed Rectifiers	
				Tripler	Quadrupler
Semiconductor Devices	Switch: 4EA Diode: 2EA Inductor: 1EA Capacitor: 1EA Total: 8EA	Switch: 3EA Diode: 2EA Inductor: 1EA Capacitor: 2EA Total: 8EA	Switch: 4EA Diode: 2EA Inductor: 1EA Capacitor: 2EA Total: 9EA	Switch: 2EA Diode: 2EA Inductor: 1EA Capacitor: 2EA Total: 7EA	Switch: 2EA Diode: 2EA Inductor: 1EA Capacitor: 2EA Total: 8EA
Transformer Offset-Current	None	None	None	Exist (Small)	None
Additional Control	Phase Control	On/Off Control	PWM Control	None	None

In column [4] of Table 1, a boost converter, which is utilized as a power factor correction (PFC) stage, is used to obtain higher I/O voltage gain. For higher I/O voltage gain, the boost inductor (L_B) in the PFC stage is replaced with a coupled inductor with secondary winding in the secondary side of the DC/DC stage, and one diode (D_A) and switch (Q_A)

are added in the secondary side of the DC/DC stage. In a situation of obtaining higher I/O voltage gain, the HB flyback converter with a single-ended rectifier is operated with a coupled inductor in the PFC stage and one diode and switch in the secondary side, finishing the operation of main HB LLC converter. This does not have offset current in the transformer, but too many components would be additionally required. In column [5] of Table 1, the HB LLC converter is proposed with additional "one primary switch (Q_A)" and "one resonant tank", including one transformer and a resonant inductor and a capacitor. If higher I/O voltage gain is required, an additional primary switch (Q_A) is always turned on, and Q_{P1} and Q_{P2} are alternatively switched. In this case, since the input voltage (V_S) is applied to each transformer in two "parallel-connected" resonant tanks, high I/O voltage gain can be obtained. Meanwhile, if Q_{P1} and Q_{P2} are together turned on or off, alternatively with Q_A, two transformers in two resonant tanks are connected in series. Since half ($V_S/2$) of the input voltage is applied to each transformer, low I/O voltage gain is achieved. This does not have offset current in the transformer, but too many components would be additionally required. In column [6] of Table 1, the HB LLC converter is proposed by "replacing two diodes with two switches" and "applying phase-shifted control" in the secondary full-bridge rectifier. If higher I/O voltage gain is needed, the phase-shifted control between the primary switches (Q_1 and Q_2) and the secondary switches (SR_1 and SR_2) is applied. Since the energy stored in a resonant inductor (L_r) is further increased, as the free-wheeling period in the secondary side is larger, higher I/O voltage gain can be achieved. However, this cannot be applied in a center-tapped rectifier, but only in a full-bridge rectifier. Moreover, this requires two additional secondary switches. In column [7] in Table 1, the HB LLC converter is proposed by "adding one switch (Q_A) and one resonant capacitor (C_{RA})". If higher I/O voltage gain is required, the additional switch is turned on; thus, the resonant capacitance is increased. Since Q factor is reduced, higher I/O voltage gain can be achieved. However, this requires additional on/off control and additional devices, which cause the complexity of the system. In column [8] of Table 1, the HB LLC converter is proposed by "replacing two diodes with two switches (Q_{SR1} and Q_{SR2})" and "adding one blocking capacitor (C_B)" in the secondary full-bridge rectifier. In the "normal full-bridge control" in the secondary side, an additional blocking capacitor (C_B) has only a function of current-balancing during the resonant region operation. Meanwhile, if higher I/O voltage gain is needed, low-side switches in the secondary full-bridge legs are both turned on. During this period, an additional blocking capacitor (C_B) stores $V_S/(2 \times n)$, where Vs and n, respectively, indicate the input voltage and the transformer turns-ratio. Then, the $V_S/(2 \times n)$ stored in the C_B is transferred to the output, with the transformer voltage reflected in the secondary side, i.e., $V_S/(2 \times n)$. Thus, the proposed converter in column [8] of Table 1 can obtain higher I/O voltage gain. However, this requires complex secondary gate control and two switches, which cannot be applied in a center-tapped rectifier but only in a full-bridge rectifier.

In this paper, new rectifiers to obtain higher voltage gain are proposed; a voltage tripler rectifier and a voltage quadrupler rectifier, which require one more capacitor in the secondary side compared with the CTR, or no elements compared with the VDR. Moreover, compared with columns [1,2,4–8] in Table 1, the proposed rectifiers can achieve high I/O voltage gain with "smaller number of elements." In addition, although the proposed voltage tripler has a "transformer offset current," it has a very small transformer offset current compared with columns [1–3] in Table 1, due to the "large transformer turns-ratio" resulting from higher I/O voltage gain. Meanwhile, the proposed voltage quadrupler has no transformer offset current. As a result, the proposed rectifiers can have a small volume, due to the low component count and the small-sized transformer, compared with prior arts. They have a simple structure with one capacitor and two diodes, and three and four times higher voltage gain with the same transformer turns-ratio.

The validity of these proposed rectifiers in the half-bridge (HB) LLC resonant converter is verified by the experimental results from a 100 W/200 V output prototype.

2. Comparison and Analysis

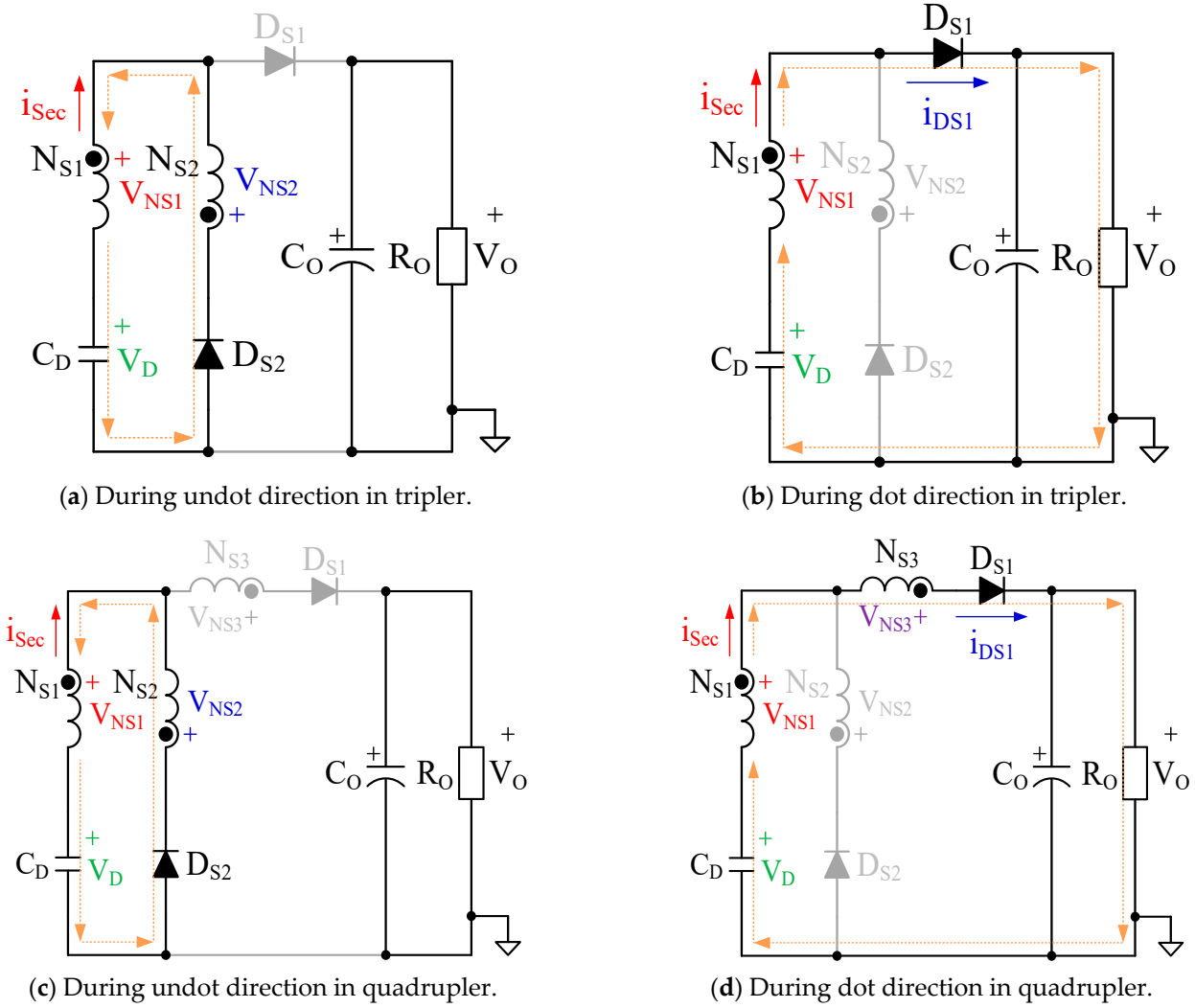
Figure 1 shows the circuit diagram of the conventional and proposed rectifiers. Figure 1a,b show the CTR and VDR, respectively. The CTR in Figure 1a has two secondary turns (N_{S1} and N_{S2}), and two diodes are series-connected to each turn.

Meanwhile, the VDR in Figure 1b has a secondary turn (N_S), and the doubler capacitor (C_D) is series-connected to that. If the secondary current (i_{Sec}) reflected from the primary flows in the secondary undot direction, the secondary diode (D_{S2}) is conducted. During this interval, assuming resonant operation, since half of the input voltage ($V_S/2$) is applied to L_M in the primary undot direction, $V_S/(2n)$ is applied to N_S in the undot direction, and the voltage (V_D) on C_D is $V_S/(2n)$. Since V_O is V_S/n in the VDR in resonant operation, as explained in Section 1, V_D is $V_O/2$, i.e., $V_D = V_S/(2n) = V_O/2$. On the other hand, if the secondary current (i_{Sec}) reflected from the primary flows in the secondary dot direction, the secondary diode (D_{S1}) is conducted, and the i_{sec} flows through N_S, D_{S1}, and C_D. During this interval, assuming resonant operation, since half of the input voltage ($V_S/2$) is applied to L_M in the primary dot direction, $V_S/(2n)$ is applied to N_S in the dot direction. Since the output voltage (V_O) is the sum of V_D and the voltage (V_{NS}) across the secondary turn (N_S), i.e., $V_{NS} = V_S/(2n)$ and $V_O = V_D + V_{NS}$, V_O is V_S/n. Thus, two times higher input/output (I/O) voltage gain can be achieved with an equal turns-ratio, compared with the CTR in Figure 1a.

On the other hand, Figures 1c and 1d show the proposed voltage tripler and quadrupler, respectively, and Figure 2 shows their operational modes. To achieve higher I/O voltage gain, the proposed rectifier has new secondary windings from the VDR.

The voltage tripler has a new N_{S2}, which is series-connected with D_{S2}. If the secondary current (i_{Sec}) reflected from the primary flows in the secondary undot direction, the secondary diode (D_{S2}) is conducted, and the secondary current flows through N_{S1}, C_D, D_{S2}, and N_{S2}, as shown in Figure 2a. During this interval, assuming resonant operation, since half of the input voltage ($V_S/2$) is applied to L_M in the primary undot direction, $V_S/(2n)$ is applied, respectively, to N_{S1} and N_{S2} in the undot direction, and the voltage (V_D) on C_D is V_S/n. On the other hand, if the secondary current (i_{Sec}) reflected from the primary flows in the secondary dot direction, the secondary diode (D_{S1}) is conducted, the i_{sec} flows through N_{S1}, D_{S1}, and C_D., and D_{S2} is blocked, as shown in Figure 2b. During this interval, assuming resonant operation, since half of the input voltage ($V_S/2$) is applied to L_M in the primary dot direction, $V_S/(2n)$ is applied to N_{S1} in the dot direction. Since the output voltage (V_O) is the sum of V_D and the voltage (V_{NS1}) across the secondary turn (N_{S1}), i.e., $V_{NS1} = V_S/(2n)$ and $V_O = V_D + V_{NS1}$, V_O is $3V_S/(2n)$. That is, since V_D is V_S/n, V_D is equal to $2V_O/3$.

The voltage quadrupler is operated similarly to the voltage tripler. It has new windings N_{S2} and N_{S3}, which are series-connected with D_{S2} and D_{S1}, respectively. If the secondary current (i_{Sec}) reflected from the primary flows in the secondary undot direction, the secondary diode (D_{S2}) is conducted, and the secondary current flows through N_{S1}, C_D, D_{S2}, and N_{S2}, as shown in Figure 2c. During this interval, assuming resonant operation, since half of the input voltage ($V_S/2$) is applied to L_M in the primary undot direction, $V_S/(2n)$ is respectively applied to N_{S1} and N_{S2} in the undot direction, and the voltage (V_D) on C_D is V_S/n. On the other hand, if the secondary current (i_{Sec}) reflected from the primary flows in the secondary dot direction, the secondary diode (D_{S1}) is conducted, the i_{sec} flows through N_{S1}, N_{S3}, D_{S1}, and C_D., and D_{S2} is blocked, as shown in Figure 2d. During this interval, assuming resonant operation, since half of the input voltage ($V_S/2$) is applied to L_M in the primary dot direction, $V_S/(2n)$ is respectively applied to N_{S1} and N_{S3} in the dot direction. Since the output voltage (V_O) is the sum of V_D and voltages (V_{NS1} and V_{NS3}) across the secondary turns (N_{S1} and N_{S3}), i.e., $V_{NS1} = V_{NS3} = V_S/(2n)$ and $V_O = V_D + V_{NS1} + V_{NS3}$, V_O is $2V_S/n$. That is, since V_D is V_S/n, V_D is equal to $V_O/2$.



(**a**) During undot direction in tripler.

(**b**) During dot direction in tripler.

(**c**) During undot direction in quadrupler.

(**d**) During dot direction in quadrupler.

Figure 2. Operational modes of proposed rectifiers.

Consequently, in the proposed voltage tripler and quadrupler, three and four times higher input/output (I/O) voltage gain can be achieved with an equal turns-ratio, compared with the CTR shown in Figure 1a.

Tables 2 and 3 show the comparison of rectifiers in terms of the transformer turns-ratio, the voltage and RMS current of C_D, and the voltage and current stresses of D_{S1} and D_{S2}. It is assumed that the HB LLC resonant converter operates in a resonant region, the diodes (D_{S1} and D_{S2}) have the same conduction time, N_P is the transformer primary turns, and the rectifiers have equal output voltage (V_O) and output current (I_O).

Table 2. Comparison of conventional and proposed rectifiers in turns-ratio (n) and secondary capacitor (C_D).

Types of Rectifier	Turns-Ratio	Capacitor (C_D)		
		Voltage Stress	Current	
			Peak	RMS
×1-Rectifier (Center-tap)	n:1:1	-	-	-
×2-Rectifier (Voltage doubler)	n:(1/2)	$V_O/2$	πI_O	$\pi I_O\sqrt{2}/2$
×3-Rectifier (Voltage tripler)	n:(1/3):(1/3)	$2V_O/3$	πI_O	$\pi I_O\sqrt{2}/2$
×4-Rectifier (Voltage quadrupler)	n:(1/4):(1/4)	$V_O/2$	πI_O	$\pi I_O\sqrt{2}/2$

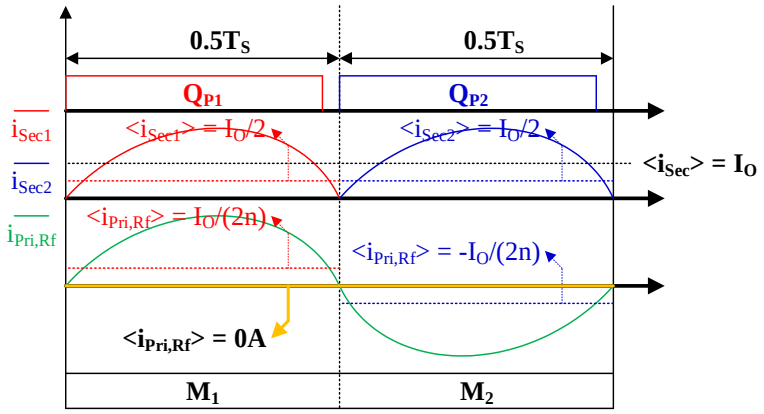
Table 3. Comparison of conventional and proposed rectifiers in secondary diodes (D_{S1} and D_{S2}).

Types of Rectifier	Turns-Ratio	Diodes (D_{S1} and D_{S2})			
		Voltage Stress		Current	
		D_{S1}	D_{S2}	Peak	Average
×1-Rectifier (Center-tap)	n:1:1	$2V_O$		$\pi I_O/2$	$I_O/2$
×2-Rectifier (Voltage doubler)	n:(1/2)	V_O		πI_O	I_O
×3-Rectifier (Voltage tripler)	n:(1/3):(1/3)	$2V_O/3$	$4V_O/3$	πI_O	I_O
×4-Rectifier (Voltage quadrupler)	n:(1/4):(1/4)	V_O		πI_O	I_O

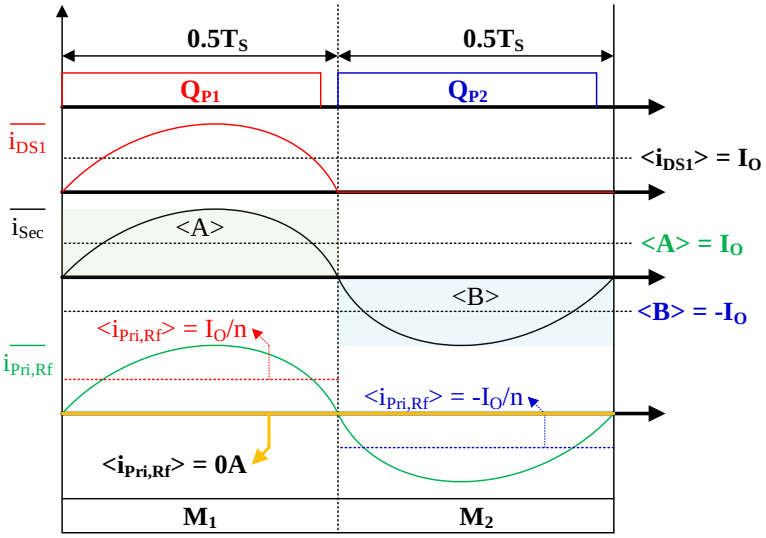
2.1. Transformer Turns-Ratio and Magnetizing Offset Current

Since the I/O voltage gains of the conventional CTR and VDR and the proposed tripler and quadrupler rectifiers are, respectively, $V_S/(2n)$, V_S/n, $3V_S/(2n)$, and $2V_S/n$, the turns-ratios ($n = N_P/N_{Sk}$, k = 1, 2, 3) of the VDR and the tripler and quadrupler rectifiers are 2, 3, and 4, respectively, under n = 1 in the CTR. Thus, a larger turns-ratio ($n = N_P/N_S$) is required to obtain the same output voltage in the proposed tripler and quadrupler, compared with the CTR and the VDR.

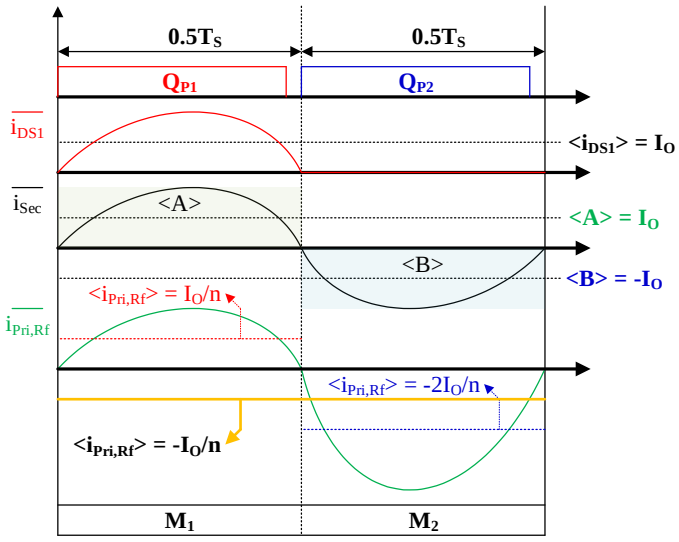
Meanwhile, in the HB LLC resonant converter with the CTR, the secondary resonant current is flowing alternately in the secondary dot or undot direction during half of a switching period ($T_S/2$), and their average should be the output current (I_O). Thus, each average of the i_{Sec} flowing in the secondary dot or undot direction should be half of the output current ($I_O/2$). If the i_{sec} is reflected in the primary side of the transformer, each average of the reflected primary current ($i_{Pri,Rf}$) is $I_O/(2n)$ or $-I_O/(2n)$ during $T_S/2$, as shown in Figure 3a. Due to the current-second balance on the primary resonant capacitor, the transformer magnetizing offset current is zero in the CTR. In Figure 3, M_1 and M_2, respectively, indicate operational modes 1 and 2.



(**a**) Conventional CTR.

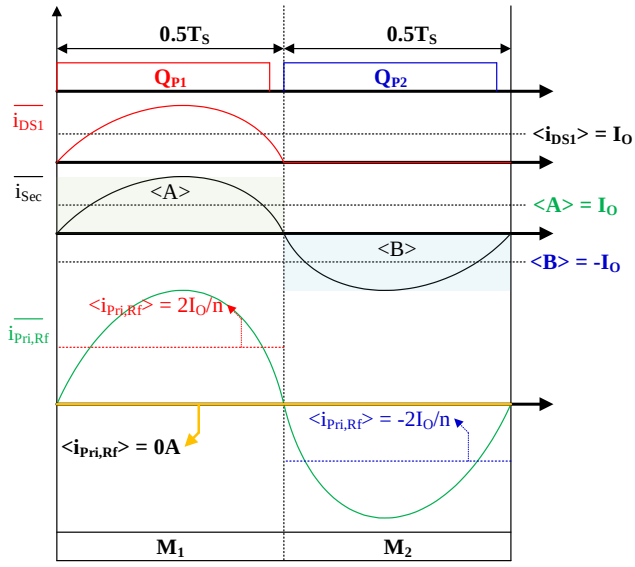


(**b**) Conventional VDR.



(**c**) Proposed tripler.

Figure 3. *Cont.*



(**d**) Proposed quadrupler.

Figure 3. Simplified primary and secondary currents in resonant operation.

Second, in the VDR, the secondary resonant current, which only flows in the secondary dot direction, is transferred to the output through C_D during $T_S/2$, and its average should be the output current (I_O). Meanwhile, the secondary resonant current, flowing in the secondary undot direction, does not pass through the output, but through C_D and D_{S2}. Due to the current-second balance on C_D, its average should be $-I_O$ during the undot-direction operation. If the i_{sec} is reflected in the primary side of the transformer, each average of the reflected primary current ($i_{Pri,Rf}$) is I_O/n or $-I_O/n$ during $T_S/2$, as shown in Figure 3b. Due to the current-second balance on the primary resonant capacitor, the transformer magnetizing offset current is also zero in the VDR.

Third, in the proposed tripler rectifier, the secondary resonant current ($i_{Sec} = i_{DS1}$), which only flows in the secondary dot direction of N_{S1}, is transferred to the output through C_D and D_{S1} during $T_S/2$, as shown in Figure 2b, and its average should be the output current (I_O), as shown in Figure 3c. Meanwhile, the secondary resonant current, flowing in the secondary undot direction of N_{S1} and N_{S2}, does not pass through the output, but through C_D and D_{S2}, as shown in Figure 2a. Due to the current-second balance on C_D, its average should be $-I_O$ during the undot-direction operation. If the i_{sec} is reflected in the primary side of the transformer, the average of the reflected primary current ($i_{Pri,Rf}$) in the dot direction is I_O/n, and the average of $i_{Pri,Rf}$ in the undot direction is $-2I_O/n$, as shown in Figure 3c. Due to the current-second balance on the primary resonant capacitor, the transformer magnetizing offset current is I_O/n in the proposed tripler rectifier.

Fourth, in the proposed quadrupler rectifier, the secondary resonant current ($i_{Sec} = i_{DS1}$), which only flows in the secondary dot direction of N_{S1} and N_{S3}, is transferred to the output through C_D and D_{S1} during $T_S/2$, as shown in Figure 2d, and its average should be the output current (I_O), as shown in Figure 3d. Meanwhile, the secondary resonant current, flowing in the secondary undot direction of N_{S1} and N_{S2}, does not pass through the output, but through C_D and D_{S2}, as shown in Figure 2c. Due to the current-second balance on C_D, its average should be $-I_O$ during the undot-direction operation. If the i_{sec} is reflected in the primary side of the transformer, each average of the reflected primary current ($i_{Pri,Rf}$) is $2I_O/n$ or $-2I_O/n$ during $T_S/2$, as shown in Figure 3d. Due to the current-second balance on the primary resonant capacitor, the transformer magnetizing offset current is also zero in the proposed quadrupler rectifier.

2.2. Voltage and Current Stress on C_D

As explained in Section 2, in the VDR, and in the proposed tripler and quadrupler rectifiers, each voltage (V_D) on the secondary capacitor (C_D) is $V_O/2$, $2V_O/3$, and $V_O/2$, respectively.

Meanwhile, in the VDR and the proposed tripler and quadrupler rectifiers, as explained in Section 2.1, if the secondary resonant current only flows in the secondary dot direction, the secondary resonant current is transferred to the output during $T_S/2$. Assuming resonant operation, its average should be the output current (I_O), and the peak ($i_{Sec,Pk}$) of the secondary resonant current can be obtained as πI_O from Equation (1), in the VDR and in the proposed tripler and quadrupler rectifiers. Since the secondary resonant current (i_{Sec}) flows through C_D, the current stress on C_D is πI_O.

$$I_O = \frac{1}{2\pi}\int_0^{\pi} i_{Sec,pk}\sin(wt)d(wt) \quad (1)$$

Moreover, due to the current-second balance on C_D, the secondary resonant current (i_{Sec}) can be expressed as $\pi I_O \times \sin(wt)$ during a period; thus, the rms current on C_D is $\pi I_O/(2)^{0.5}$, in the VDR and in the proposed tripler and quadrupler rectifiers.

2.3. Voltage and Current Stress on D_{S1} and D_{S2}

The voltage stress on a diode is determined when a diode is blocked.

In the CTR, if the secondary current (i_{Sec}) reflected from the primary flows in the secondary dot direction, D_{S1} is conducted and D_{S2} is blocked. Thus, the voltage across N_{S1} is the output voltage (V_O), and the voltage stress on D_{S2} is $2V_O$ by the secondary turns-ratio of the transformer, assuming $N_{S1} = N_{S2}$. In the opposite situation, the voltage stress on D_{S1} is $2V_O$. Moreover, the secondary resonant current is twice transferred to the output during a period. Assuming resonant operation, its average should be the output current (I_O), and the peak ($i_{Sec,Pk}$) of the secondary resonant current can be obtained as $\pi I_O/2$ from Equation (2).

$$I_O = \frac{1}{\pi}\int_0^{\pi} i_{Sec,pk}\sin(wt)d(wt) \quad (2)$$

Since the secondary resonant current (i_{Sec}) flows through D_{S1} or D_{S2}, the current stress on D_{S1} and D_{S2} is $\pi I_O/2$.

In the VDR, if the secondary current (i_{Sec}) reflected from the primary flows in the secondary dot direction, D_{S1} is conducted and D_{S2} is blocked. Thus, the voltage stress on D_{S2} is V_O. On the other hand, if the secondary current (i_{Sec}) reflected from the primary flows in the secondary undot direction, D_{S2} is conducted and D_{S1} is blocked. Thus, the voltage stress on D_{S1} is V_O.

In the proposed tripler rectifier, if the secondary current (i_{Sec}) reflected from the primary flows in the secondary dot direction, D_{S1} is conducted and D_{S2} is blocked. Since V_D is $2V_O/3$, the voltage (V_{NS1}) across N_{S1} is $V_O/3$. Assuming $N_{S1} = N_{S2}$, the voltage (V_{NS2}) across N_{S2} is $V_O/3$ in the dot direction; thus, the voltage stress on D_{S2} is $4V_O/3$. Meanwhile, if the secondary current (i_{Sec}) reflected from the primary flows in the secondary undot direction, D_{S2} is conducted and D_{S1} is blocked. Due to $V_D = 2V_O/3$, and assuming $N_{S1} = N_{S2}$, the voltage (V_{NS2}) across N_{S2} is $V_O/3$ in the undot direction by the secondary turns-ratio of the transformer; thus, the voltage stress on D_{S1} is $2V_O/3$.

In the proposed quadrupler rectifier, if the secondary current (i_{Sec}) reflected from the primary flows in the secondary dot direction, D_{S1} is conducted and D_{S2} is blocked. Since V_D is $V_O/2$, the voltages (V_{NS1}, V_{NS2}, and V_{NS3}) across N_{S1}, N_{S2}, and N_{S3} are $V_O/4$ in the dot direction by the secondary turns-ratio of the transformer, assuming $N_{S1} = N_{S2} = N_{S3}$. As a result, the voltages (V_{NS2} and V_{NS3}) across N_{S2} and N_{S3} are cancelled, and the voltage stress on D_{S2} is V_O. Meanwhile, if the secondary current (i_{Sec}) reflected from the primary flows in the secondary undot direction, D_{S2} is conducted and D_{S1} is blocked. Due to $V_D = V_O/2$, and assuming $N_{S1} = N_{S2} = N_{S3}$, the voltages (V_{NS1}, V_{NS2}, and V_{NS3}) across N_{S1}, N_{S2}, and N_{S3} are $V_O/4$ in the undot direction by the secondary turns-ratio of the transformer. As

a result, the voltages (V_{NS2} and V_{NS3}) across N_{S2} and N_{S3} are cancelled, and the voltage stress on D_{S1} is V_O.

On the other hand, in the VDR and in the proposed tripler and quadrupler rectifiers, due to once powering in a switching period, as explained in Section 2.2, the average currents on D_{S1} and D_{S2} are I_O, and they are increased two times compared with that ($I_O/2$) in the CTR. Moreover, since the secondary resonant current (i_{Sec}) flows through D_{S1} or D_{S2}, the current stresses on D_{S1} or D_{S2} are πI_O, which is equal to the current stress on C_D. Consequently, the multipliers have lower voltage stress and higher current stress than the CTR.

3. Design Guideline of Proposed Rectifiers

3.1. Design of Transformer Turns-Ratio

The I/O voltage gain ($M = V_O/V_S$) of the proposed voltage tripler is $3/(2n)$ at resonant frequency, as mentioned in Section 2, Comparison and Analysis. Since "the input voltage (V_S) and output voltage (V_O) are, respectively, 400 V and 100 V" and "the highest efficiency is indicated at resonant frequency," n is 6.

Meanwhile, the I/O voltage gain ($M = V_O/V_S$) of the proposed voltage quadrupler is $2/n$ at resonant frequency, as mentioned in Section 2, Comparison and Analysis. Since "the input voltage (V_S) and output voltage (V_O) are, respectively, 400 V and 100 V" and "the highest efficiency is indicated at resonant frequency," n is 8.

3.2. Design of Resonant Tanks (L_R, C_R, and L_M)

The voltage gain ($M = V_O/V_S$) of the HB LLC converter can be expressed as follows [7]:

$$M = \frac{V_O}{V_S} = \frac{1}{n' \sqrt{\left\{1 + \frac{1}{k}\left[1 - \left(\frac{f_R}{f_S}\right)^2\right]\right\}^2 + \left[\frac{\pi^2 Q}{8(\alpha n)^2}\left(\frac{f_S}{f_R} - \frac{f_R}{f_S}\right)\right]^2}} \quad (3)$$

where $k = L_M/L_R$, $Q = (L_R/C_R)^{0.5}/R_O$, $f_R = 1/[2\pi(L_R C_R)^{0.5}]$, $n = N_P/N_S$, and f_S is the switching frequency.

Here, n′ indicates, respectively, $3/(2n)$ and $2/n$ in the proposed tripler and quadrupler rectifiers. Moreover, α indicates, respectively, 1/3 and 1/4 in the proposed tripler and quadrupler rectifiers. Assuming V_S = 400 V and V_O = 100 V, n should be 6 and 8 at resonant frequency in the proposed tripler and quadrupler rectifiers. In addition, since n′ and $\alpha \times n$ are equal to 1/4 and 2 in both rectifiers, both voltage gains are the same.

Figure 4 shows equal voltage gain ($M = V_O/V_S$) in the proposed tripler and quadrupler rectifiers at full load condition, where I/O voltage gain is the lowest. Since Vs is 400 V and V_O is 100 V, the voltage gain (M) is 0.25. From Figure 4, it is noted that M is 0.25 at resonant frequency (f_R = 80 kHz). By considering "double gain margin" and frequency variation range, L_M and L_R are designed at 500 µH and 62 µH, i.e., $k = L_M/L_R \approx 8$. To operate at resonant frequency (f_R = 80 kHz) for high efficiency, C_R is designed at 62nF, i.e., $f_R = 1/[2\pi(L_R C_R)^{0.5}] \approx 80$ kHz.

3.3. Design of Main Transformer

The core area (A_C) is included in $L_M \cdot i_{LM,Max} = N_P \cdot B_{Max} \cdot A_C$, where $i_{LM,Max}$ is the maximum magnetizing inductor current, N_P is the primary turns of the transformer, and B_{Max} is the maximum flux density.

In the tripler rectifier, since the voltages (V_D and V_{NS1}) on C_D and secondary turns (N_{S1}) are $2V_O/3$ and $V_O/3$ during 0.5 T_S of undot direction operation in Figure 2a, the voltage (V_M) on the magnetizing inductor (L_M) is $nV_O/3$; thus, the ripple (Δi_{LM}) of the magnetizing inductor current is $nV_O/(6 \cdot L_M \cdot F_S)$. Meanwhile, the tripler rectifier has a transformer magnetizing offset current ($i_{LM,Offset}$), i.e., $i_{LM,Offset} = I_O/n$; thus, $i_{LM,Max}$ is the sum of $i_{LM,Offset}$ and $\Delta i_{LM}/2$, i.e., $i_{LM,Max} = i_{LM,Offset}$ ($=I_O/n$) + $\Delta i_{LM}/2$[$=nV_O/(12 \cdot L_M \cdot F_S)$]. Generally, the transformer turns-ratio (n) of the HB LLC resonant converter with the CTR is

2, but with the proposed tripler rectifier, it is is 6. As a result, the proposed tripler rectifier has a much smaller transformer magnetizing offset current, compared with [1–3].

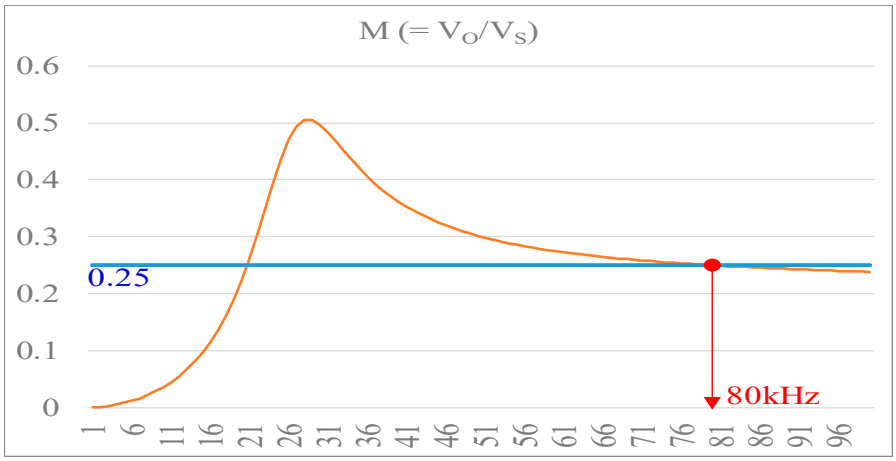


Figure 4. Voltage gain (M) of the proposed tripler and quadrupler rectifiers.

In the quadrupler rectifier, since the voltages (V_D and V_{NS1}) on C_D and secondary turns (N_{S1}) are $V_O/2$ and $V_O/4$ during 0.5 T_S of the undot direction operation, as shown in Figure 2c, the voltage (V_M) on the magnetizing inductor (L_M) is $nV_O/4$; thus, $i_{LM,Max}$ is $nV_O/(16 \cdot L_M \cdot F_S)$.

On the other hand, the window area (A_W) indicates the area to wind the primary and secondary windings. A_W can be expressed as $(N_P \cdot i_{LR,RMS} + N_{S1} \cdot i_{NS1,RMS} + N_{S2} \cdot i_{NS2,RMS})/(K_U \cdot J)$ in the tripler rectifier and $(N_P \cdot i_{LR,RMS} + N_{S1} \cdot i_{NS1,RMS} + N_{S2} \cdot i_{NS2,RMS} + N_{S3} \cdot i_{NS3,RMS})/(K_U \cdot J)$ in the quadrupler rectifier, where, respectively, $i_{LR,RMS}$ and $i_{NSn,RMS}$ mean the RMS current on the primary turns (N_P) and the secondary turns (N_{Sn}) in the transformer, and K_U and J mean the utilization factor of the window area and the current density of the primary and secondary wires in the transformer.

The turns-ratio (n) of the proposed tripler and quadrupler rectifiers were determined to be 6 and 8 by applying I/O voltage gain at resonant frequency. Moreover, L_M was determined to be 500µH by considering "double gain margin" and frequency variation range. Assuming N_P and A_C are 48 and 170 mm^2 because of V_O = 100 V and F_S = 80 kHz, the maximum flux density (B_{Max}) is 0.097 T and 0.077 T, respectively, in the tripler and quadrupler rectifiers, which are within the saturation flux (B_{Sat}), i.e., B_{Sat} = 0.3 T. Due to $i_{LM,Offset}$ in the tripler rectifier, B_{Max} in the tripler rectifier is higher. For high efficiency in high switching frequency, the variation (ΔB) of the flux density, related to the core loss, is generally designed below 0.15 T. ΔB are equal to 0.153 T, because Δi_{LM} in both rectifiers are equal to 2.5 A. By considering ΔB and core volume (V_e), related to the core loss, the primary turns and core of the transformer are chosen at 48 turns and PQ3220 with "A_C = 170 mm^2 and PL-13 material."

Meanwhile, in the tripler and quadrupler rectifiers, the peak ($i_{LR,PK}$) of the primary current (i_{LR}) is πI_{in}, using a relationship that the average of the input current with i_{LR} and 0 A in half a cycle is equal to the input current (I_{in}); thus, the RMS ($i_{LR,RMS}$) of i_{LR} is $\pi I_{in}\sqrt{2}/2$, i.e., $i_{LR,RMS}$ = 1.11 A. In the tripler and quadrupler rectifiers, the current (i_{NS1}) on N_{S1} is equal to that on C_D from Figure 2, and its RMS current ($i_{NS1,RMS}$) is $\pi I_O\sqrt{2}/2$ from Table 2, i.e., $i_{NS1,RMS}$ = 4.44 A. Moreover, in both rectifiers, the currents (i_{NS2} and i_{NS3}) on N_{S2} and N_{S3} are the same as the half-cycle shape of the current on C_D from Figure 2. As a result, their RMS currents ($i_{NS2,RMS}$ and $i_{NS3,RMS}$) are all $\pi I_O/2$, i.e., $i_{NS2,RMS} = i_{NS3,RMS}$ = 3.14 A. If K_U is 0.25 and J is 6 A/mm^2, A_W in the tripler and quadrupler rectifiers are, respectively, 76 mm^2 and 78.4 mm^2, which are suitable for PQ3220 with A_W = 80.8 mm^2.

Consequently, PQ3220 with PL-13 material, A_C = 170 mm^2, and A_W = 80.8 mm^2 was selected for the transformer in both rectifiers, by considering reasonable A_C and A_W as following Table 4.

Table 4. Design parameters for transformer and resonant inductor (L_R).

Components	Proposed Voltage Tripler	Proposed Voltage Quadrupler
Ripple of magnetizing inductor current (Δi_{LM})	$nV_O/(6 \cdot L_M \cdot F_S)$	$nV_O/(8 \cdot L_M \cdot F_S)$
Magnetizing offset current ($i_{LM,Offset}$)	I_O/n	-
Maximum magnetizing inductor current ($i_{LM,Max}$)	$I_O/n + nV_O/(12 \cdot L_M \cdot F_S)$	$nV_O/(16 \cdot L_M \cdot F_S)$
Core Area (A_C)	$[L_M \cdot I_O/n + nV_O/(12 \cdot F_S)]/(N_P \cdot B_{Max})$	$nV_O/(16 \cdot F_S \cdot N_P \cdot B_{Max})$
RMS current ($i_{LR,RMS}$) on primary turns (N_P)	$\pi I_{in}\sqrt{2}/2$	
RMS current ($i_{NS1,RMS}$) on secondary turns (N_{S1})	$\pi I_O\sqrt{2}/2$	
RMS current ($i_{NS2\sim3,RMS}$) on secondary turns (N_{S1}, N_{S2})	$\pi I_O/2$	
Window Area (A_W)	$(N_P \cdot i_{LR,RMS} + N_{S1} \cdot i_{NS1,RMS} + N_{S2} \cdot i_{NS2,RMS})/(K_U \cdot J)$	$(N_P \cdot i_{LR,RMS} + N_{S1} \cdot i_{NS1,RMS} + N_{S2} \cdot i_{NS2,RMS} + N_{S3} \cdot i_{NS3,RMS})/(K_U \cdot J)$
Transformer	Proposed Voltage Tripler	Proposed Voltage Quadrupler
L_M	500μH	
n (N_P:N_{S1}:N_{S2}:N_{S3})	6 (48:8:8)	8 (48:6:6:6)
A_C (PQ3220)/B_{Max}/ΔB	170 mm^2/0.097 T/0.153 T	170 mm^2/0.077 T/0.153 T
A_W	76 mm^2	78.4 mm^2

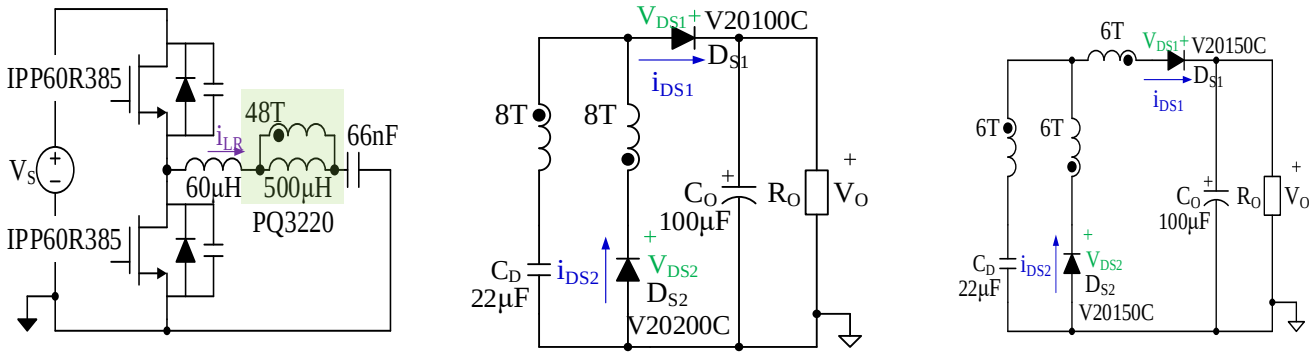
4. Experimental Results

To verify the operation and analysis of the proposed rectifiers, the prototype was implemented using the half-bridge (HB) LLC resonant converter with the proposed voltage tripler and quadrupler rectifiers. Table 5 and Figure 5 show the experimental specifications, components, and circuits with used parameters of each component. The specifications are 400 V input and 100 V/200 W output. The transformer turns-ratios are 48:8:8, and 48:6:6:6 for the voltage tripler and quadrupler, respectively. From Table 2, it is noted that the number of the secondary turns between the voltage tripler and quadrupler is three-fourths different, under the same primary turns.

Figures 6 and 7 show the experimental waveforms based on the realized H/W of the primary current (i_{LR}), and the voltages (V_{DS1} and V_{DS2}) and currents (i_{DS1} and i_{DS2}) of the secondary diodes in the voltage tripler and quadrupler, respectively.

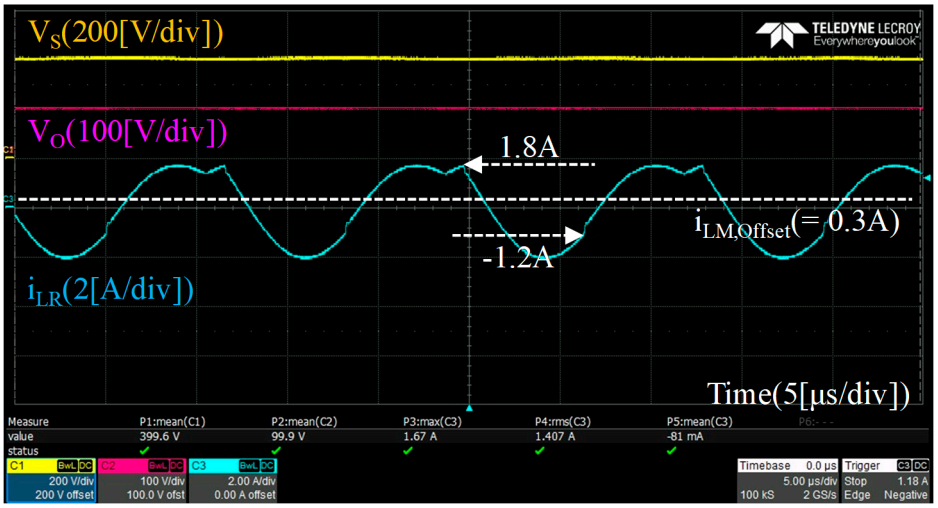
Table 5. Specifications and components used in experimental prototype.

Specifications	**Proposed Voltage Tripler**	**Proposed Voltage Quadrupler**
Input Voltage (V_S)	400 [V_{DC}]	
Output Voltage (V_O)	100 [V_{DC}]	
Output Power (P_O)	200 [W] (Rated Load Resistance (R_O) = 50 [Ω])	
Switching Frequency (F_S)	80 [kHz]	
Components	**Proposed Voltage Tripler**	**Proposed Voltage Quadrupler**
Primary switches (Q_{P1} and Q_{P2})	IPP60R385CP (650 [V]/9 [A]/385 [mΩ])	
Transformer	PQ3220(PL-13) • L_M: 500 [μH], L_{lkg}: 32 [μH] • Turns-ratio: 48:8:8 (n = 6) • Primary Winding: 0.5[mm] • Secondary Winding: 1 [mm](N_{S1}), 0.8 [mm](N_{S2})	PQ3220(PL-13) • L_M: 500 [μH], L_{lkg}: 38 [μH] • Turns-ratio: 48:6:6:6 (n = 8) • Primary Winding: 0.5[mm] • Secondary Winding: 1 [mm](N_{S1}), 0.8 [mm] (N_{S2}, N_{S3})
Resonant inductor (L_R)	PQ2016(PL-13) • L_R: 30 [μH] • Number of Turns: 5 • Winding: 0.5 [mm]	PQ2016(PL-13) • L_R: 24 [μH] • Number of Turns: 5 • Winding: 0.5 [mm]
Resonant capacitor (C_R)	62 [nF] (KEMET) R76MF2470 (400 [V]/47 [nF]) + R76MF2150 (400 [V]/15 [nF])	
Secondary diode (D_{S1})	V20100C (100 V/20 A/0.58 V)	V20150C (150 V/20 A/0.69 V)
Secondary diode (D_{S2})	V20200C (200 V/20 A/0.68 V)	
Secondary capacitor (C_D)	24 [μF] (KEMET) R76IW5120 (250 [V]/12 [μF]) × 2 [EA]	
Experimental Stresses	**Proposed Voltage Tripler**	**Proposed Voltage Quadrupler**
Secondary diode (D_{S1})	Steady-State: 67 [V] (= $2V_O/3$) Maximum: 73[V]	Steady-State: 100 [V] (= V_O) Maximum: 140 [V]
Secondary diode (D_{S2})	Steady-State: 134 [V] (= $4V_O/3$) Maximum: 157 [V]	Steady-State: 100 [V] (= V_O) Maximum: 137 [V]

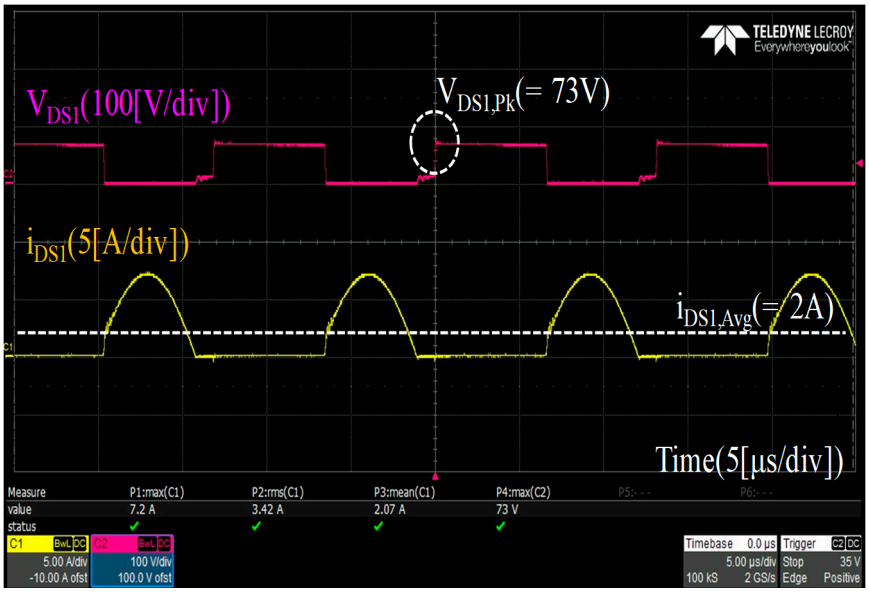


(**a**) Common primary circuit. (**b**) Proposed tripler. (**c**) Proposed quadrupler.

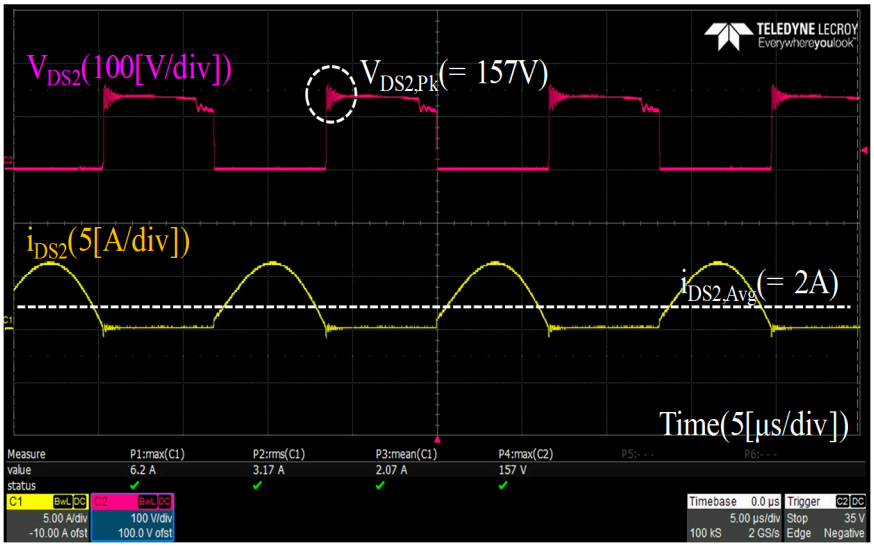
Figure 5. Experimental circuits of HB LLC resonant converter.



(**a**) Input voltage (V_S), output voltage (V_O), and primary resonant transformer current (i_{LR}).

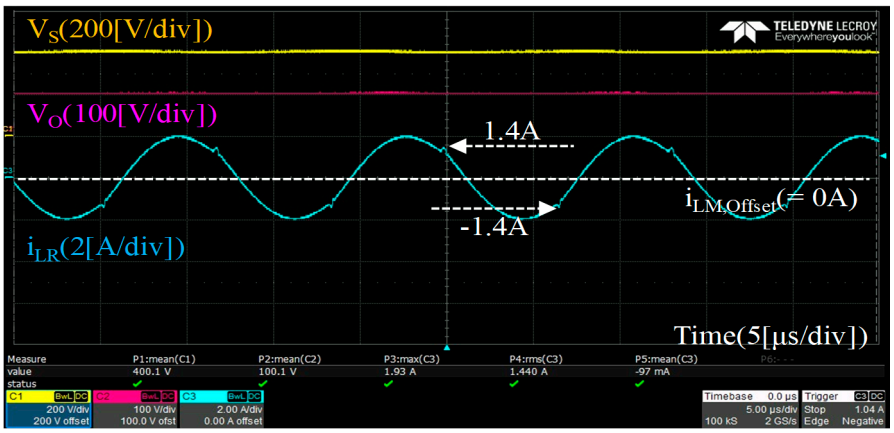


(**b**) Voltage and current on D_{S1} (V_{DS1} and i_{DS1}).

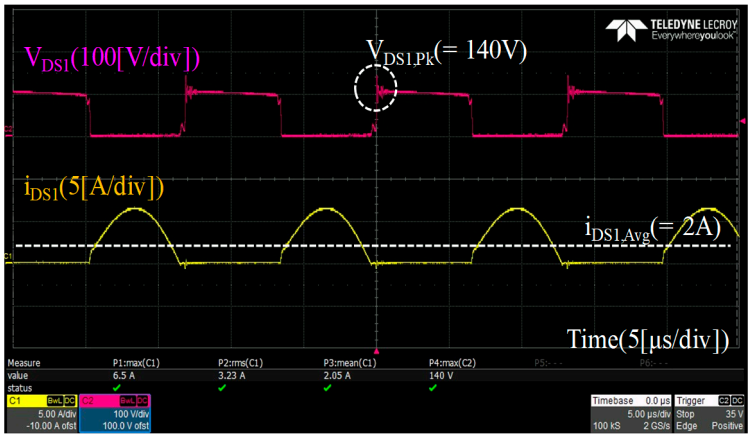


(**c**) Voltage and current on D_{S2} (V_{DS2} and i_{DS2}).

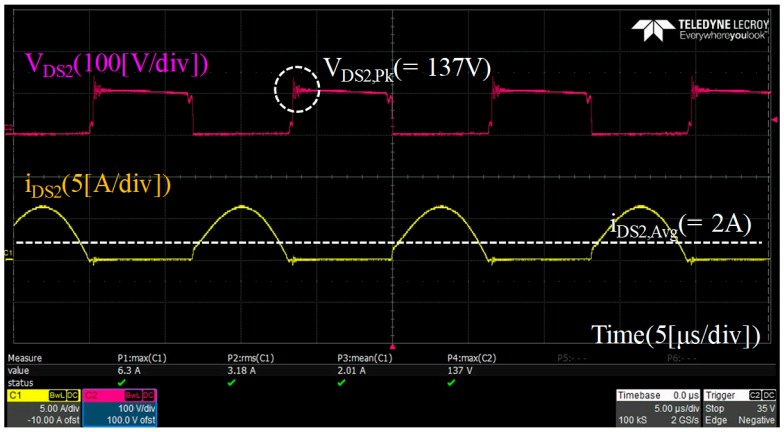
Figure 6. Experimental waveforms with a realized H/W in proposed tripler.



(**a**) Input voltage (V_S), output voltage (V_O), and primary resonant transformer current (i_{LR}).



(**b**) Voltage and current on D_{S1} (V_{DS1} and i_{DS1}).



(**c**) Voltage and current on D_{S2} (V_{DS2} and i_{DS2}).

Figure 7. Experimental waveforms with a realized H/W in proposed quadrupler.

The voltage tripler has asymmetric waveform in the primary current (i_{LR}), due to the magnetizing offset current about 0.33A (= I_O/n), as shown in Figure 6a. This results from operations shown in Figure 2a,b. During "undot direction like Figure 2a" and "dot direction like Figure 2b," $-2I_O/n$ and I_O/n are on average reflected to the primary side, respectively. In addition, "initial resonant currents" in i_{LR} are different at 1.8 A and -1.2 A, as shown in Figure 6a, due to the magnetizing offset current. This results in "below or above operation" alternatively in a switching period. However, the primary current (i_{LR}) is symmetrical, due to there being no magnetizing offset current in the voltage quadrupler, as shown in Figure 7a. This results from the operations, as shown in Figure 2c,d. During

"undot direction like Figure 2c" and "dot direction like Figure 2d," $-2I_O/n$ and $2I_O/n$ are on average reflected to the primary side, respectively. Therefore, i_{LR} in Figures 6a and 7a has different shapes, due to the magnetizing offset current.

On the other hand, the average and peak values of the diode currents (i_{DS1} and i_{DS2}) are about 2A (= I_O) and 6.3A (= πI_O), which are the same in the two rectifiers, as shown in Figure 6b,c and Figure 7b,c. The voltage stresses (V_{DS1} and V_{DS2}) of D_{S1} and D_{S2} in the voltage tripler are 73 V (= $2V_O/3$ [=67 V] + Ringing [=6 V]) and 157 V (= $4V_O/3$ [=134 V] + Ringing [=23 V]), respectively, as shown in Figure 6b,c. Those in the voltage quadrupler are 140 V (= V_O [=100 V] + Ringing [=40 V]) and 137 V (= V_O [=100 V] + Ringing [=37 V]), as shown in Figure 7b,c. The difference in the voltage stresses on the secondary diodes results from the parasitic pattern leakage inductance.

Finally, the efficiencies of the voltage tripler and quadrupler are measured at about 94.1% and 93.7% at full load condition, respectively. Figure 8 shows theoretical loss distribution in both voltage rectifiers. Both rectifiers use equal components "except for the secondary turns of the transformer and secondary diodes," due to a very small magnetizing offset current ($i_{LM,Offset} = I_O/n$) resulting from a large transformer turns-ratio (n), although the voltage tripler has $i_{LM,Offset}$.

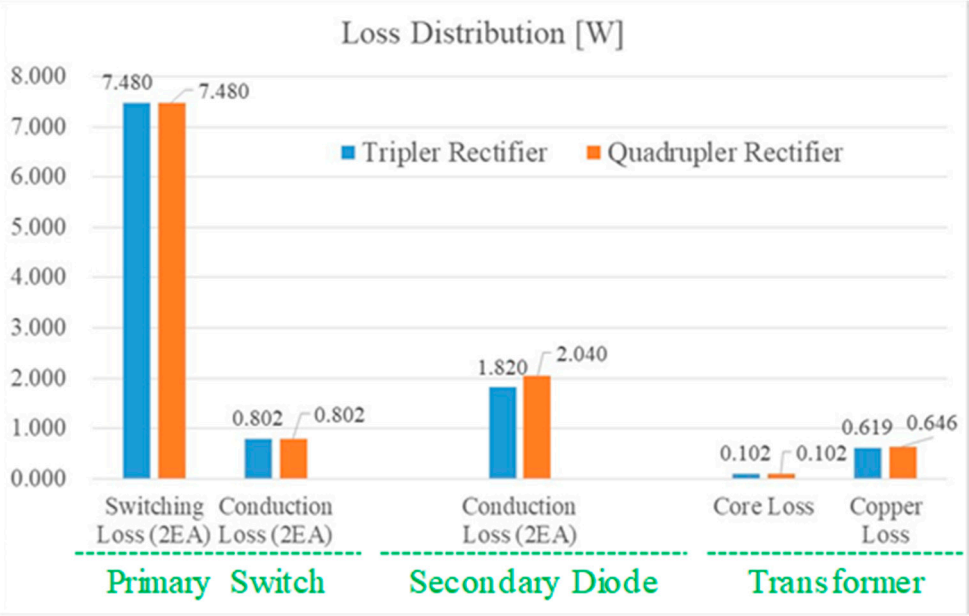


Figure 8. Loss distribution at full-load condition in voltage tripler and quadrupler.

As shown in Figure 8, the voltage tripler has less conduction loss on the secondary diodes (D_{S1} and D_{S2}). This results from the small forward voltage of V20100C with a 100 V rating, compared with V20150C with a 150 V rating in the voltage quadrupler. Moreover, since the voltage tripler has fewer total secondary turns (16T) than those (18T) of the voltage quadrupler, it has slightly less copper loss in the transformer.

Consequently, the voltage tripler has slightly higher efficiency, due to the smaller conduction and copper losses in the secondary side than those of the voltage quadrupler; however, both rectifiers have almost equal efficiency.

5. Conclusions

New rectifiers are proposed in this paper. The proposed voltage tripler and quadrupler rectifiers have a simple structure with one capacitor and two diodes, and higher voltage gain with an equal turns-ratio or the same voltage gain with a larger turns-ratio. The proposed tripler and quadrupler rectifiers have several advantages, such as low component counts, a smaller transformer magnetizing offset current resulting from a larger turns-

ratio, and no additional controls, compared with eight previous examples that can obtain additional I/O voltage gains in HB LLC resonant converters.

The rectifiers were compared and analyzed in respect of the transformer turns-ratio, the magnetizing offset current, and the voltage and current stresses of the secondary capacitor and diodes. Moreover, the design details, including the transformer turns-ratio, the resonant tanks, and the main transformer, which are different from those of conventional HB LLC resonant converters, were presented in this paper.

The validity of the basic operation and features was confirmed by the experiment using the half-bridge LLC resonant converter with 400 V input and 100 V/200 W output. Even though the diodes were adopted in the secondary side, the proposed tripler and quadrupler rectifiers achieved 94.1% and 93.7%, respectively. Moreover, the proposed tripler has the same size of transformer as the quadrupler rectifier, due to a much higher transformer turns-ratio, although it has a transformer magnetizing offset current.

This research will be helpful in applications requiring both high efficiency and a high step-up ratio in the half-bridge LLC resonant converter.

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