

## Article

# A 125 KHz, Single-Stage, Dual-Output Wireless Power Receiver with PSM Modulation

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**Abstract:** This paper presents a 125 KHz, single-stage, dual-output wireless power receiver with pulse skip modulation (PSM). Multi-output receivers are proposed to supply different modules in one system. Conventional multi-output receivers contain a rectifier and a multi-output regulator, which degrade the power conversion efficiency (PCE) due to interstage loss of the rectifier and the regulator. Additionally, existing single-inductor multi-output (SIMO) receivers exhibit a cross-regulation phenomenon because of the sharing inductor, which decreases the stability of the output voltages, and the use of an inductor in SIMO receivers increases the cost of the circuit. The proposed receiver in this article realizes rectification and regulation in only one stage, which eliminates interstage loss; this improves the power conversion efficiency of the system and realizes dual-output voltages with only four power transistors without an inductor, which reduces the chip area and minimizes cost. There is no cross-regulation in this dual-output architecture because the dual-output voltages are charged by different phases of the input signal. PSM modulation was adopted to regulate output voltages for higher efficiency. The proposed single-stage, dual-output regulating rectifier delivers a maximum power of 47 mW, and the dual-output voltages are 1.8 V and 2 V. This receiver is designed by a 0.18  $\mu\text{m}$  complementary metal-oxide-semiconductor (CMOS) process and realizes a peak efficiency of 86% when the output power ranges from 15 mW to 47 mW.

**Keywords:** power conversion efficiency; regulating rectifier; wireless power transfer



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## 1. Introduction

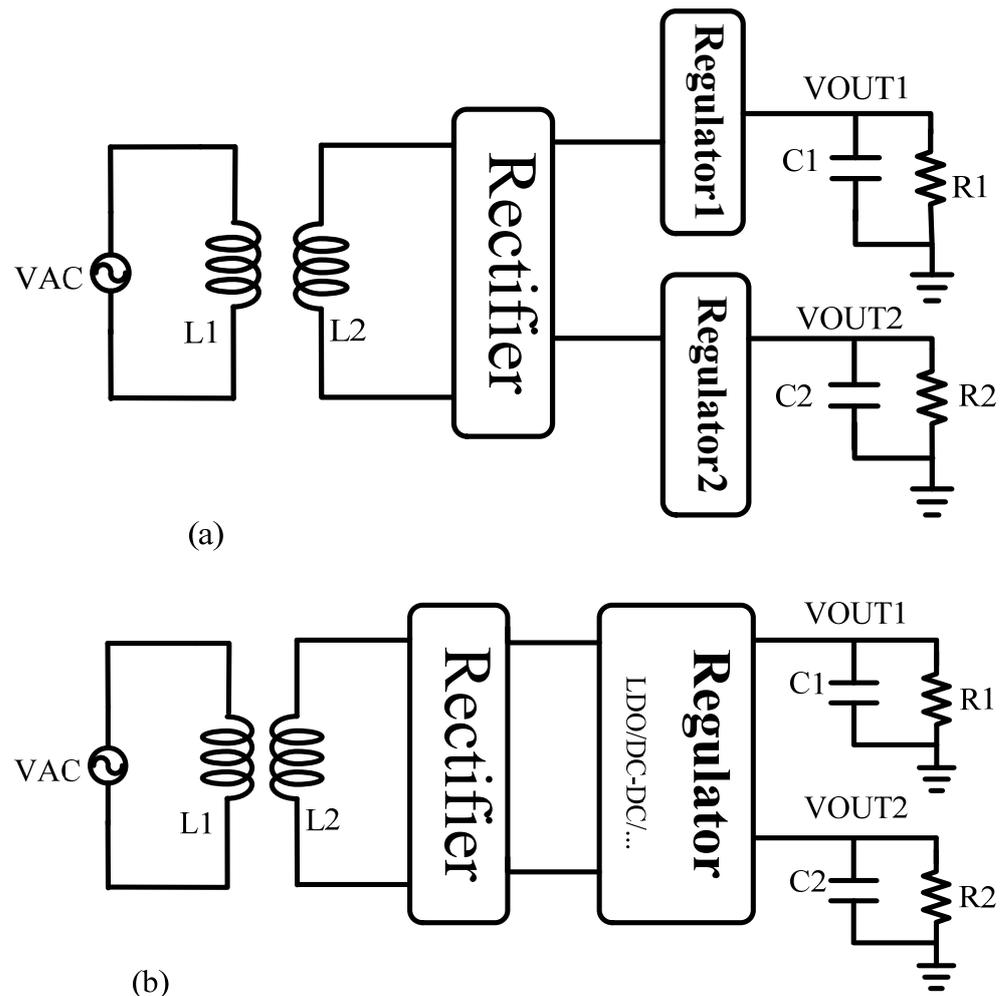
In recent years, wireless power transfer (WPT) has become increasingly popular for different applications, such as wireless charging, radio frequency identification devices (RFID), electric vehicles and implantable medical devices [1–4].

Wireless power receivers obtain power from the secondary coil of the WPT system, and the receiver achieves the conversion of alternating current to direct current (AC–DC). The direct current (DC) from the receiver is applied to different circuit blocks. The conventional receivers are usually made up of a rectifier and a regulator, which are referred to as a two-stage structure: The rectifier converts the alternating current (AC) signal to an unregulated DC signal, and the regulator realizes direct current to direct current (DC–DC) [5]. The most common regulators are the low-dropout (LDO) and DC–DC regulators.

In many applications, different modules need power supplies from one system, which requires multiple output voltages from a receiver. For example, for portable solid-state drives, two different voltages are applied to the power memory circuit and the core logic circuit. It is necessary to develop multi-output receivers. Many researchers have focused on multi-output receivers, which can be realized by different methods. The multi-output regulator in [6] adopts two separated DC–DC converters to produce two independent voltages, as shown in Figure 1a, which uses two inductors in the footprint. The classic method for wireless power receivers to realize multi-output regulating voltages is shown

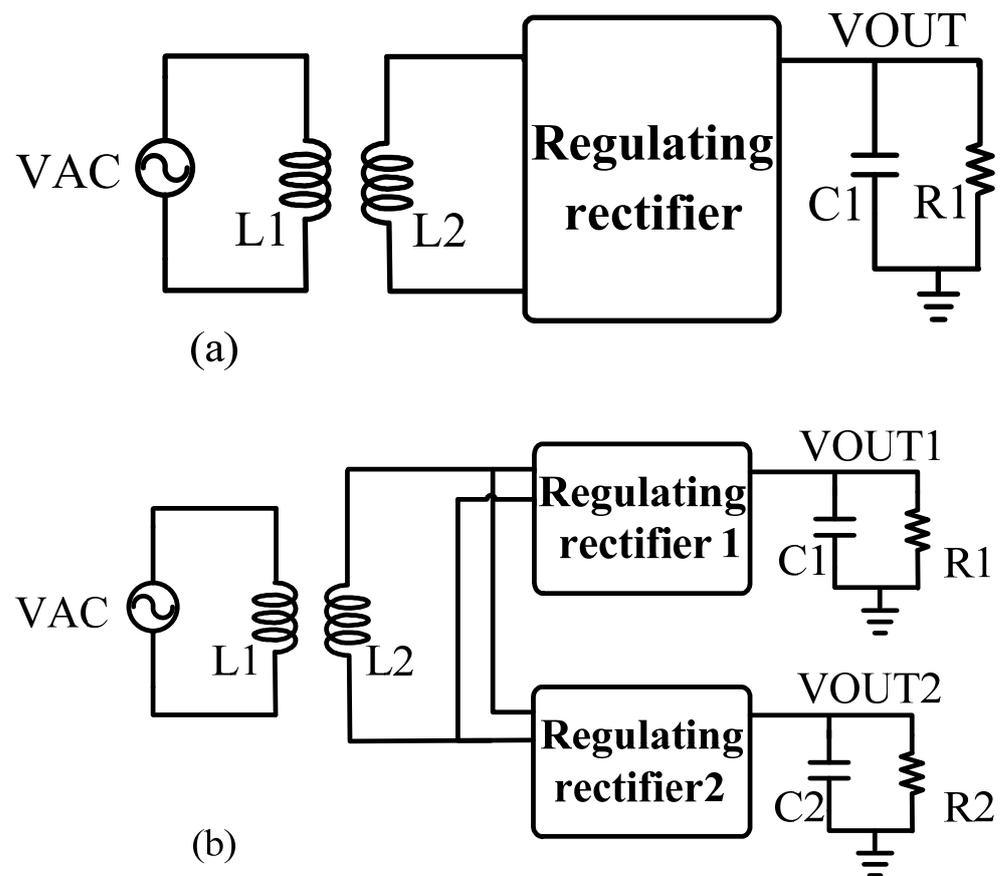
in Figure 1b [7]. The receiver in [7] uses a single-inductor, dual-output (SIDO) structure with only one inductor to reduce costs. However, SIDO receivers exhibit a cross-regulation phenomenon due to the sharing of power from one inductor, which means that when one output voltage changes, the other output voltage also changes [8]. The efficiency of a two-stage receiver is shown in Equation (1); the efficiencies of both the rectifier and the regulator influence system efficiency. Additionally, the interstage loss between the rectifier and the regulator degrades the overall efficiency of the receiver, which cannot be ignored.

$$\eta_{receiver} = \eta_{rectifier} * \eta_{regulator} \quad (1)$$



**Figure 1.** The diagram of a two-stage dual-output wireless power receiver; (a) receiver with dual-output regulator; (b) receiver with separated dual-output regulator.

Single-stage receivers have been developed for higher power conversion efficiency and fewer power transistors, which combine the functions of the rectifier and the regulator and convert the input AC signal to the regulating output DC signal [9,10], as shown in Figure 2a. The single-stage AC–DC converter is usually implemented in two ways: one way is by using a reconfigurable rectifier [11], and the other way is by controlling the conduction time of power transistors to regulate the output voltage [12,13]. In [9,10], the authors focus on converting the AC signal to the regulating DC signal directly, but the structures cannot deliver different output voltages.



**Figure 2.** Single-stage alternating current to direct current (AC–DC) direct converter (a) single-stage single-output AC–DC direct converter; (b) AC–DC multi-output converter.

In reality, some situations need single-stage multi-output receivers for the advantage of not needing an inductor. For example, for implanted medical devices, different voltages are needed to supply digital and analog modules; due to the special implanted environment, a small chip size is required. Figure 2b presents a single-stage dual-output receiver, which is realized by two self-regulating rectifiers linking with the same secondary coil in parallel [14]. However, cross-regulation occurs due to the shared inductor. In [8,9,13], the authors realize dual-output receivers in one stage, which adopts different controllers to regulate different output voltages simultaneously. In [15], a single-stage dual-output wireless power receiver with ten power transistors is described. In [13], an AC–DC single-stage receiver with six power transistors is described. Both receivers in [13,15] occupy a large chip area and increase costs. In [16], the receiver uses four power transistors to regulate two output voltages; however, its control structure is complex, needing six hysteretic comparators.

In this article, we only use four power transistors to convert the AC voltage into two regulating DC voltages, and the number of transistors and other components is less than those in [13,15]. The power transistors in [13,15] occupy a large chip area, which goes against the purpose of cost-saving. The controller of this work is more convenient to realize and has fewer components than [16], which uses a complex control structure. In this paper, the dual-output voltages obtain power from different phases of the input signal, which means that if one output voltage changes, it will not influence the other output voltage. In other words, there is no cross-regulation in this work. Additionally, pulse skip modulation (PSM) was adopted to regulate the two output voltages.

This paper is organized as follows: Section 1 provides the introduction; Section 2 illustrates the system structure and working principle; Section 3 introduces the circuit implementation; Section 4 presents the simulation results, followed by a conclusion in Section 5.

## 2. System Structure and Working Principle

### 2.1. System Structure

The secondary power-resonant tank of the wireless power receiver has two styles: series resonance and parallel resonance. Parallel resonance is applied to several milliwatt situations, such as implanted medical devices [17], while series resonance prefers watt-level applications, such as mobile electronic devices [18]. Additionally, the parallel-resonant inductor–capacitor (LC) tank has the characteristic of a voltage source, and the series-resonant inductor-capacitor LC tank behaves as a current source [19]. The characteristics of series resonance and parallel resonance are shown in Figure 3. In this work, parallel resonance is adopted.

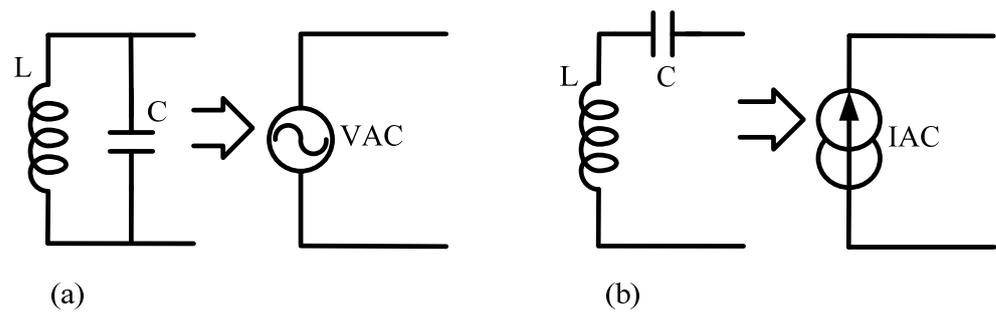


Figure 3. (a) Parallel-resonant equivalent; (b) series-resonant equivalent.

This article presents a single-stage, dual-output regulating rectifier, the diagram of which is shown in Figure 4. More outputs can be added by adding power transistors in this system, as shown in Figure 5. Adding  $N$  more outputs necessitates  $N$  more transistors, and the transistor number of  $N$  outputs can be presented as  $(N + 2)$ . The system clock doubles the input frequency and divides the input voltage into odd and even cycles.

Acronyms mentioned in this paper are presented as follows: VAC is the signal source;  $L_1$  and  $L_2$  represent primary and secondary coils, respectively;  $CR_1$  and  $CR_2$  represent resonant capacitors of primary and secondary stages, respectively;  $I_{ac}$  is the input current of the circuit;  $V_{in+}$  and  $V_{in-}$  are the inductive voltages of secondary stages and the input voltages of the proposed circuit, respectively; comparator 1 and comparator 2 are represented by  $CMP_1$  and  $CMP_2$ , respectively;  $V_{G1}$  and  $V_{G2}$  are the gate voltages of power transistors;  $V_{O1}$  and  $V_{O2}$  are dual-output voltages and are represented by  $V_O$ ;  $CS_1$  and  $CS_2$  represent the control signals of comparator 1 and 2, respectively;  $C_1$  and  $C_2$  are output capacitors;  $R_1$  and  $R_2$  represent output loads;  $V_{ref1}$  and  $V_{ref2}$  are reference voltages;  $P_1$ ,  $P_2$ ,  $N_1$  and  $N_2$  are power transistors.

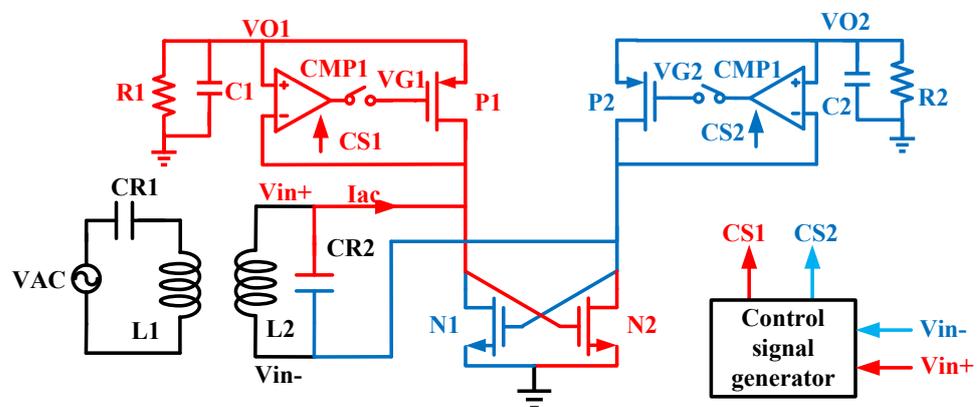
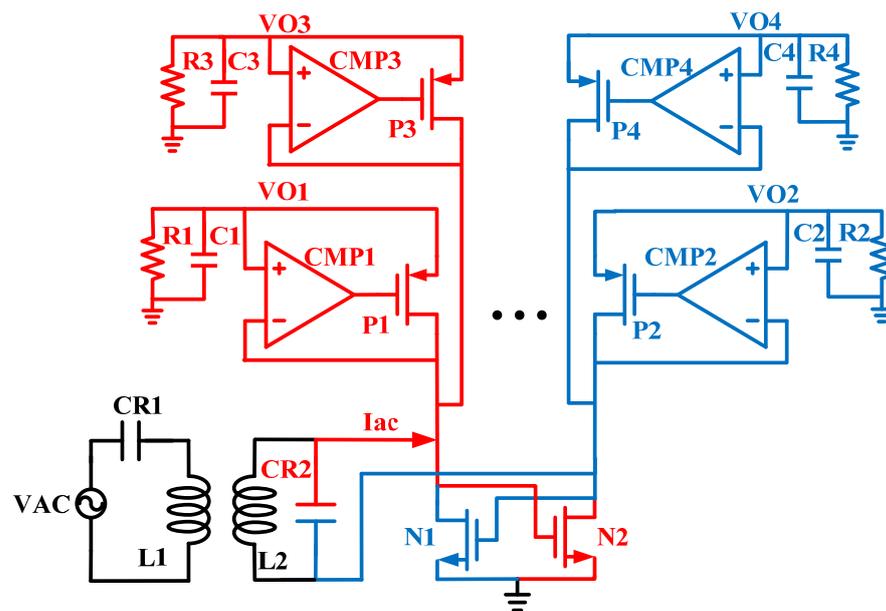


Figure 4. The diagram of the single-stage, dual-output converter in this article.



**Figure 5.** The diagram of the single-stage, multi-output wireless power receiver.

Different output voltages occupy different phases of the input signal, which means that the output voltage VO1 only works in odd cycles, and the output voltage VO2 only works in even cycles. By comparing the output voltage VO and the input voltage  $V_{in}$ , the dual-output voltages are charged to the desired values.

The advantages of this system are as follows: (1) delivering two different regulating voltages in one stage simultaneously; (2) using a lower number of on-chip power transistors and other components to reduce cost; (3) eliminating cross-regulation, which occurs in the SIMO system; (4) decreasing power consumption through PSM modulation.

## 2.2. Working Principle

Figure 4 presents the diagram of this system. This work adopted PSM modulation to control the output voltages VO1 and VO2. The controllers sampled VO1 and VO2 and generated control signals (CS) CS1 and CS2 to control the conduction of power transistors and to determine the charging states of output voltages. The CS signals are valid at a low voltage level to charge outputs VO1/VO2 by  $V_{in}$ , and the CS signals are valid at a high voltage level to charge outputs VO1/VO2 by output capacitors C1 and C2. As the control signals are generated from different phases in one period of the input signal, there is only one output voltage being charged at the same time.

According to the voltage level of control signals, the system works in three different states, namely State 1, State 2 and State 3. State 1 and State 2 represent the charging mode, which means output voltages are charged by  $V_{in}$  in these states, and State 3 represents the discharging mode, which means output voltages are charged by the output capacitor in this state. Additionally, State 1 can be represented by  $CS1 = 0, CS2 = 1, VO1 < V_{in+}$ ; State 2 can be represented by  $CS1 = 1, CS2 = 0, VO2 < V_{in-}$ ; State 3 can be represented by  $CS1 = 1, CS2 = 1/CS1 = 0, VO1 > V_{in+}, CS2 = 1/CS1 = 1, CS2 = 0, VO2 > V_{in-}$ . These are shown in Table 1.

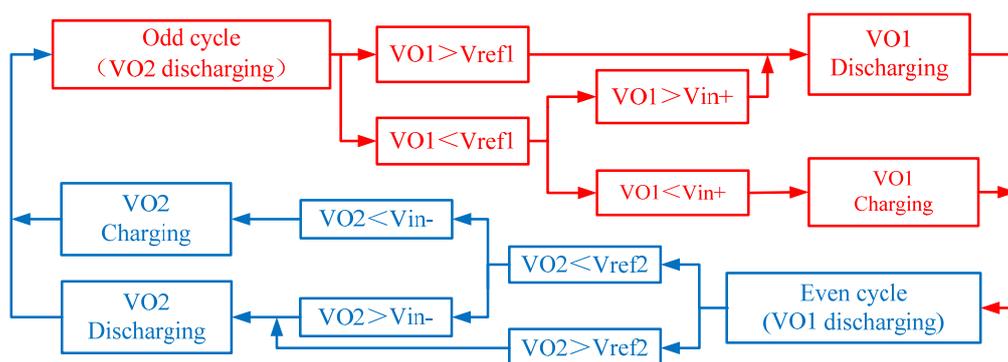
When the system works in State 1, power transistors P1 and N2 turn on to charge output voltage VO1, and at the same time, power transistors P2 and N1 turn off. Similarly, in State 2, transistors P2 and N1 conduct to charge output voltage VO2, while transistors P1 and N2 are cut off. In State 3, both transistors P1 and P2 shut off, and transistors N1 and N2 conduct alternately: when transistor N1 turns on,  $V_{in+}$  is clamped to the ground; similarly, when transistor N2 turns on,  $V_{in-}$  is clamped to the ground. In this state, loads R1 and R2 are charged by output capacitors C1 and C2, respectively, which means that there is no connection between the input voltage and the output voltage.

**Table 1.** System control principle and working state.

CS1	CS2	VO vs. Vin	VO1	VO2	ON	OFF	State
0	1	$VO1 < Vin+$	charging	discharging	P1 and N2	P2/N1	State 1
0	1	$VO1 > Vin+$	discharging	discharging	N1/N2	P1 and P2	State 3
1	0	$VO2 > Vin-$	discharging	charging	P2 and N1	P1/N2	State 2
1	0	$VO2 < Vin-$	discharging	charging	P2 and N1	P1/N2	State 2
1	1	no relationship	discharging	discharging	N1/N2	P1 and P2	State 3

The system adopts PSM to reduce power consumption. When  $VO1 > Vref1$  in odd cycles and  $VO2 > Vref2$  in even cycles, the cycles are skipped. Next, different working states are introduced according to the phases of input signals. When odd cycles arise, the output voltage  $VO1$  and the reference voltage  $Vref1$  are compared to determine the working mode of this system. When  $VO1 > Vref1$ , it means that the output voltage is large enough, and output voltage  $VO1$  does not need to be charged. Then, the cycles are skipped, and the system works in discharging mode (State 3). Output voltage  $VO1$  is powered by the output capacitor  $C1$  in this state. However, when  $VO1 < Vref1$ , two situations can occur. If  $VO1 < Vin+$ , the power transistors P1 and N2 turn on, and the output voltage  $VO1$  is charged by  $Vin+$ ; in this situation, the system works in charging mode (State 1). If  $VO1 > Vin+$ , the power transistors P1 and N2 turn off to cut off the channel of input and output voltages, and the output voltage  $VO1$  is charged by the output capacitor  $C1$ ; in this situation, the system works in the discharging mode (State 3).

When even cycles arise, the output voltage  $VO2$  is compared with the reference voltage  $Vref2$ . If  $VO2 > Vref2$ , it means that the output voltage is large enough and it does not need to be charged; thus, the cycles are skipped. The system works in the discharging mode (State 3), and the output voltage  $VO2$  is charged by the output capacitor  $C2$ . When  $VO2 < Vref2$ , two situations happen. If  $VO2 > Vin-$ , there is no current through the transistors P2 and N1, and the output voltage  $VO2$  is charged by the output capacitor  $C2$ ; in this situation, the system works in the discharging mode (State 3). If  $VO2 < Vin-$ , the transistors P2 and N1 turn on, and the output voltage  $VO2$  is charged by  $Vin-$ . The circuit works in the charging mode (State 2). The control principle of this system is shown in Table 1, and the control flow chart is shown in Figure 6.



**Figure 6.** Flow chart of the control principle of this article.

### 3. Implementation of the Control Signal Generator

Figure 7 presents the diagram of the control signal generator. It shows only one set of generators, and the other output has the same control structure. The timing generator produces a level signal (EN: EN1, EN2) and a clock signal (CLK: CLK1, CLK2) from  $Vin+$  and  $Vin-$ . The clock pulse signals (CP: CP1 and CP2) defer from the CLK signals. The EN signals control the conduction of the dual-output power transistors P1 and P2 alternately, and  $EN = 0$  is valid. The RST means a reset signal, which resets flip-flops at the start-up

stage of the system, and  $RST = 0$  is valid. The digital logic modules generate a control signal from the EN and a load signal (S) when CP signals trigger. Additionally, VO represents the output voltages VO1 and VO2.

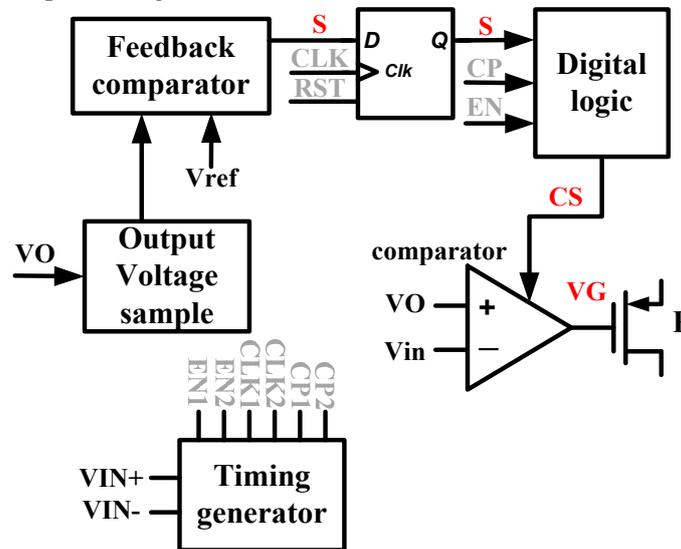


Figure 7. Control signal generator.

When EN1 enables, the output voltage VO1 is sampled, and the result is sent to feedback comparator 1. Then, feedback comparator 1 generates the load signal (S1) and sends the information to flip-flop 1. When pulse signal CLK1 works, the trigger sends the load signal S to digital logic 1. Additionally, the control signal CS1 is generated and sent to comparator 1 to control the conduction state of power transistor P1, as described in Section 2.2. Similarly, when EN2 enables, VO2 is sampled, and the result is sent to feedback comparator 2. Then, the sampling result and the reference voltage Vref are compared to generate the load signal S2 and to send S2 to flip-flop 2. S2 is delivered to the digital logic 2 module when the clock signal CLK2 arises, and the control signal CS2 is generated and sent to control the conduction state of P2 when CP2 triggers. The timing logic chart of control signals, level signals, clock signals and load signals is shown in Figure 8.

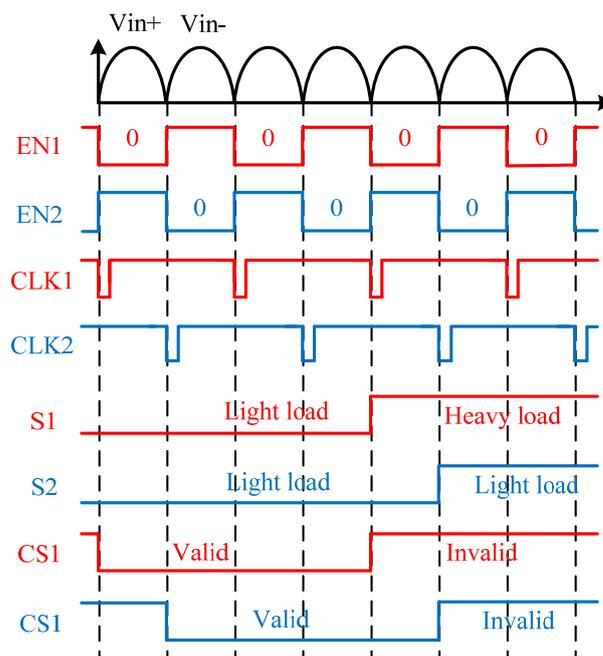


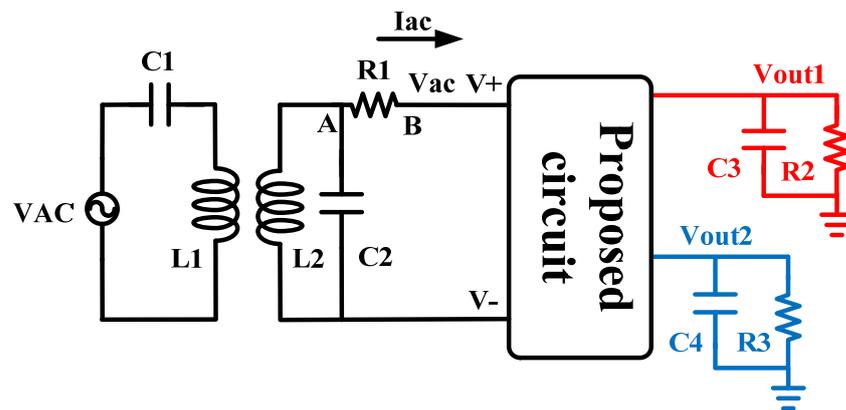
Figure 8. Timing diagram of clock and control signals.

#### 4. Simulation Results

The single-stage dual-output wireless power receiver in this work is designed by a 0.18  $\mu\text{m}$  CMOS process, and the operating frequency is 125 KHz. Figure 9 shows the testbench of the proposed circuit. As mentioned in Section 2, the secondary coil and the capacitor are equivalent to a voltage source due to parallel resonance, and the value of the equivalent voltage source in this circuit is  $V_{ac} = \pm 2.5$  V. R1 is a sensing resistor measuring input current  $I_{ac}$ ;  $I_{ac}$  is represented in Equation (2) with the value of R1 as 10  $\Omega$ . The input current is necessary to calculate the power conversion efficiency, as shown in Equation (3). The system efficiency is the ratio of the output power to input power. Output power is clear: the total power of two output branches. Additionally, the input power is the average value of the production of the input voltage and the input current during some periods. Additionally, the two off-chip capacitors are 5  $\mu\text{F}$ . The following simulation results are performed by using cadence.

$$I_{ac} = \frac{V_A - V_B}{R1} \quad (2)$$

$$\eta_{receiver} = \frac{\frac{V1^2}{R1} + \frac{V2^2}{R2}}{\frac{1}{nT} \int_{T1}^{T1+nT} V_{ac}(t) * I_{ac}(t) dt} * 100\% \quad (3)$$



**Figure 9.** The testbench circuit of the proposed single-stage, dual-output rectifier.

Figure 10 shows the simulation results of the dual-output voltages of this system. The dual-output voltages are 1.8 V and 2 V. Figure 11 presents the simulation waveform when the loads are light ( $I_{o1} = 1$  mA) and heavy ( $I_{o2} = 15$  mA). When control signal CS1 enables, the gate voltage VG1 of power transistor P1 is able to conduct transistor P1 to charge the output voltage VO1. PSM modulation is clearly observed: the charging activity is more frequent to meet the demand of VO1 when the load is heavy, while the charging activity is less frequent, which means the system skips cycles when the load is light. Comparing the control signals of the two different loads, it is obvious that the conduction time of the control signal in a heavy load is longer than in a light load every time. Additionally, at every conduction time, the number of charging output voltages in a heavy load is more than in a light load, resulting in a denser output voltage ripple. In a light load, the transistor P1 only takes a short time to charge output voltage VO1, and during that time, the ripple of output voltage VO1 increases quickly. Then, VO1 turns into discharging time and slowly decreases; during the decreasing time, pulse skip modulation appears to skip cycles. The results of this figure are simulated where  $I_{o2}$  is fixed at 5 mA.

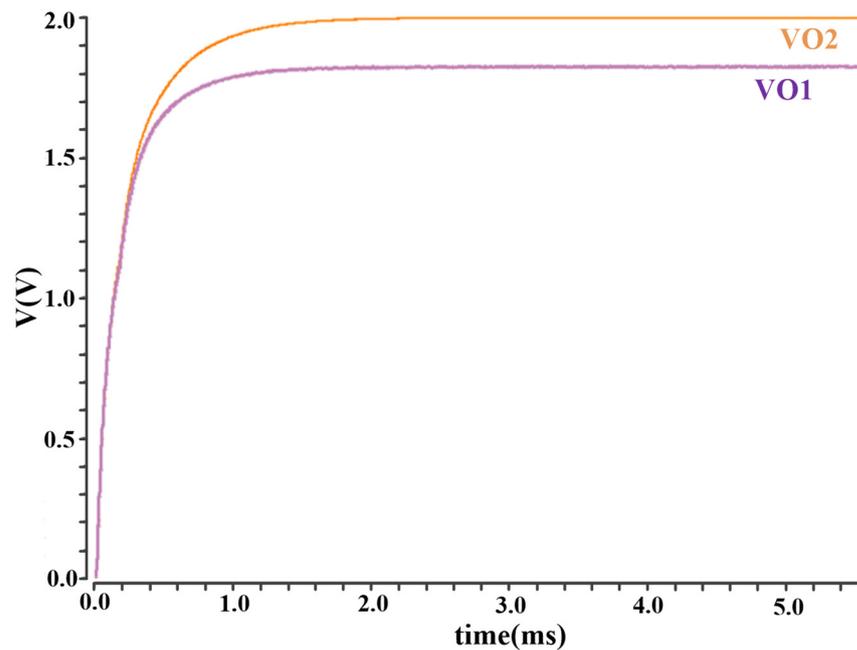


Figure 10. Dual-output regulating voltages of this receiver: VO1 = 1.8 V; VO2 = 2 V.

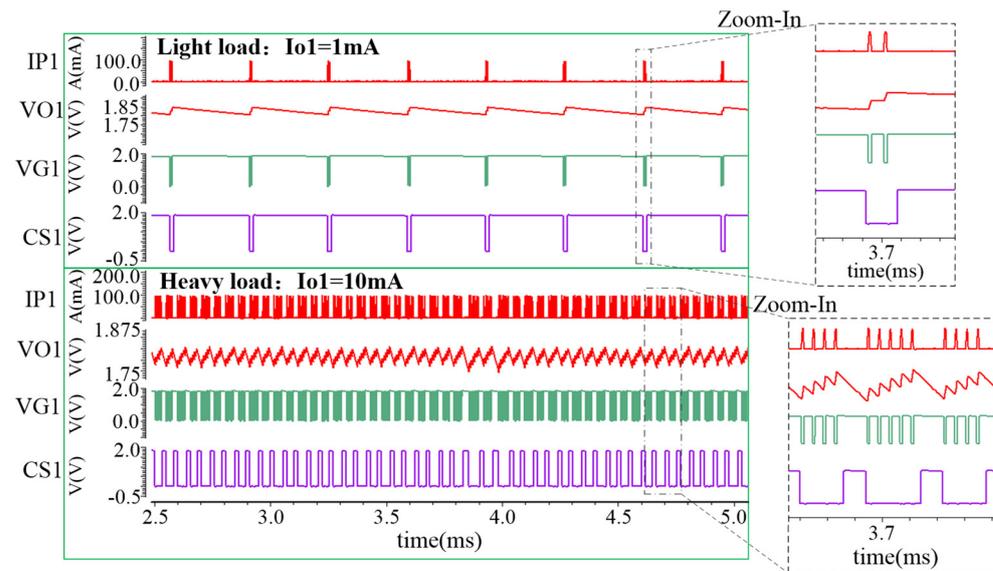
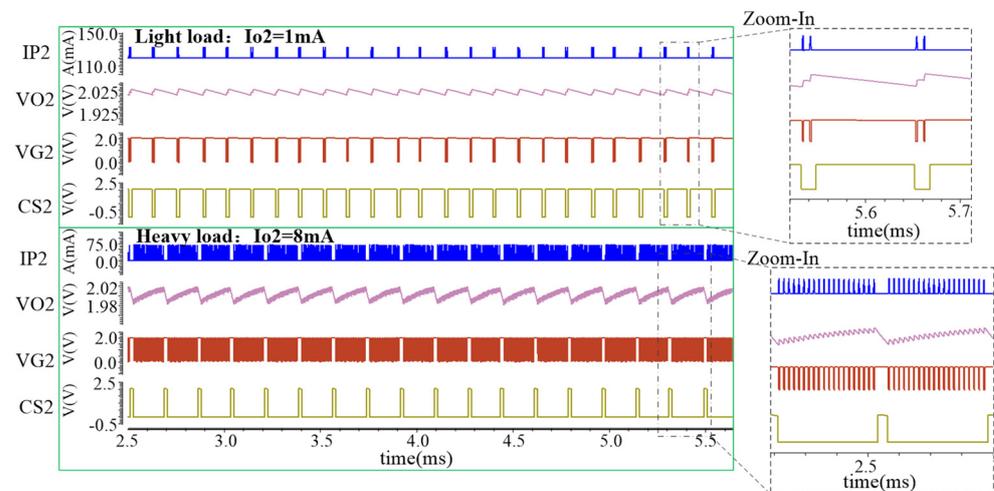


Figure 11. Simulation waveform: current flowing to power transistor P1 ( $I_{p1}$ ), output voltage (VO1), the gate voltage of P1 (VG1) and control signal (CS1), where VO1 has light ( $I_{o1} = 1 \text{ mA}$ ) and heavy load ( $I_{o1} = 15 \text{ mA}$ ).

Figure 12 shows the different waveforms of the output voltage VO2 in different load situations. Similarly, every time the control signal CS2 enables, the gate voltage VG2 of the power transistor P2 is able to conduct the transistor, and the output voltage VO2 is charged. In the charging mode, the output voltage increases; on the contrary, in the discharging mode, the output voltage drops. It is obvious that the valid time of the control signal in the heavy load is longer at every conduction time, and the conduction frequency of the power transistor P2 is greater in the heavy load than in the light load. In the light load, due to the short valid time of the control signal, there are only a few charging times quickly supplying output voltage VO2 to the expected value. Then, VO2 drops slowly, and the system skips some cycles. In the heavy load, due to the long valid time of the control signal, the conduction frequency of the power transistor P2 is higher, and the charging speed is

slower due to the heavy load. The results in this figure are simulated, where  $I_{o1}$  is fixed at 5 mA.



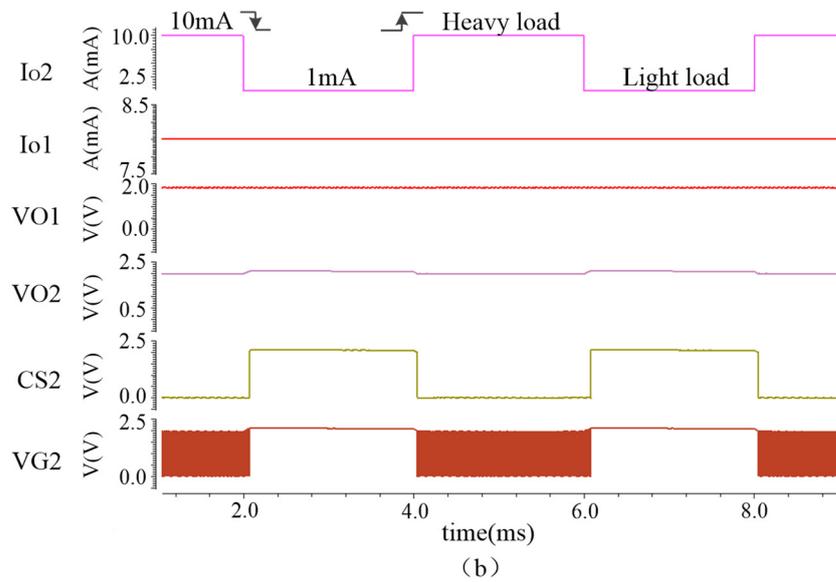
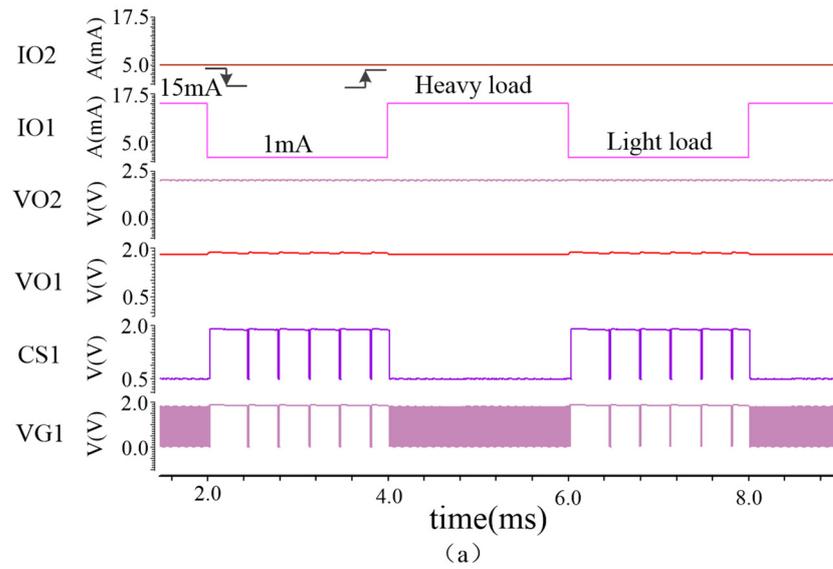
**Figure 12.** Simulation waveform: current flowing to power transistor P12 ( $I_{p2}$ ), output voltage ( $V_{O2}$ ), gate voltage of P2 ( $V_{G2}$ ) and control signal ( $C_{S2}$ ), where  $V_{O2}$  has light ( $I_{o2} = 1$  mA) and heavy load ( $I_{o2} = 8$  mA).

We can observe light loads in Figures 11 and 12. Compared to the charging frequency of output voltage  $V_{O2}$ , output voltage  $V_{O1}$  charges less and skips more cycles.  $V_{O2}$  charges more as the output voltage  $V_{O2}$  is higher. Additionally, the heavy loads of the two pictures are not comparable due to the different load currents.

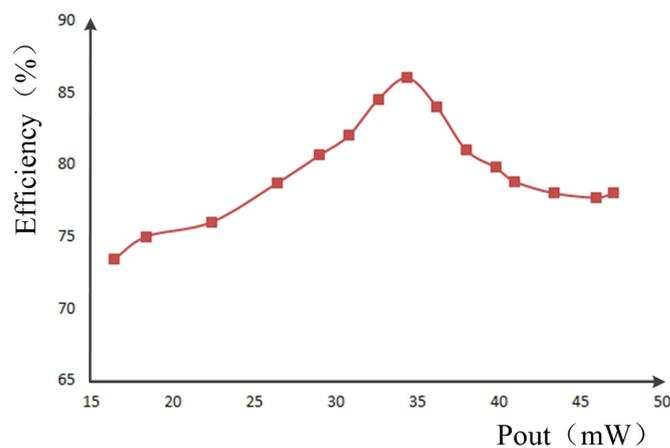
To verify the cross-regulation phenomenon, transient load changes were set in the simulation environment. Figure 13a plots the waveform of dual-output voltages  $V_{O1}$  and  $V_{O2}$ , dual-output currents  $I_{o1}$  and  $I_{o2}$ , the control signal  $C_{S1}$  and the gate voltage  $V_{G1}$  of transistor P1, where load R1 changes sharply from 15 mA to 1 mA and from 1 mA to 15 mA. When  $I_{o1}$  varies from 1 mA to 15 mA in 10 ns, it takes 15  $\mu$ s to recover from the undershoot voltage of 60 mV, and we can notice that when  $I_{o1}$  varies, the output voltage  $V_{O1}$  has a undershoot voltage of 60 mV. However, output voltage  $V_{O2}$  has no change, which means that there is no cross-regulation when  $I_{o1}$  changes from 1 mA to 15 mA. Similarly, the system needs 203  $\mu$ s to recover from a 60 mV overshoot voltage when  $I_{o1}$  changes from 15 mA to 1 mA in 10 ns, and there is no influence on the output voltage  $V_{O2}$ , which means that there is no cross-regulation in this situation. This figure is simulated when  $I_{o2}$  is fixed at 5 mA.

Figure 13b plots the waveform of dual-output voltages  $V_{O1}$  and  $V_{O2}$ , dual-output currents  $I_{o1}$  and  $I_{o2}$ , control signal  $C_{S2}$  and gate voltage  $V_{G2}$  of power transistor P2 when the load changes between 1 mA and 10 mA. It takes 40  $\mu$ s to recover from an overshoot of 60 mV when the  $I_{o2}$  increases from 1 mA to 10 mA in 10 ns. In this situation, the output voltage  $V_{O2}$  has a tiny change, and the output voltage  $V_{O1}$  has no variation, which means that there is no cross-regulation. Similarly, when the  $I_{o2}$  changes from 10 mA to 1 mA in 10 ns, the system takes 322  $\mu$ s to return back from an 80 mV undershoot voltage, and there is no influence on the output voltage  $V_{O1}$ , which indicates that there is no cross-regulation in this situation. This figure is simulated when  $I_{o1}$  is fixed at 5 mA.

Overall, there is no influence on one output voltage when the other output voltage changes. The reason is that the two output voltages are charged from different phases of the input signal, which eliminates the cross-regulation phenomenon that exists in the SIMO system due to the shared inductor. Figure 14 shows the efficiency of the proposed single-stage, dual-output receiver. A maximum efficiency of 86% can be reached in this system when the output power changes from 15 mW to 47 mW for dual-output voltages of 2 V and 1.8 V. The efficiency decreases after peak efficiency because of the increasing on-resistance losses.



**Figure 13.** (a) The waveform of the output current of load R2 ( $I_{o2}$ ),  $VO_2$  and  $VO_1$ , control signal (CS) and the gate voltage of P1 when  $I_{o1}$  changes sharply; (b) the waveform of the output current of load R2 ( $I_{o2}$ ),  $VO_2$  and  $VO_1$ , control signal (CS) and the gate voltage of P2 when  $I_{o2}$  changes sharply.



**Figure 14.** The system efficiency of this architecture.

Table 2 summarizes the comparison of state-of-the-art works and the proposed single-stage, dual-output wireless power receiver. ISSCC [13] and JSSC [5] represent two-stage AC–DC receivers with only one output voltage. TPE [7] delivers dual-output voltages with a rectify stage and a SIMO stage. JSSC [12] and TPE [1] show single-stage receivers with only one output voltage. It is obvious that the efficiency of single-stage single-output receivers is higher than two-stage, single-output receivers because of the elimination of interstage loss. CICC [15] shows single-stage, dual-output receivers with a closed-loop delay controller and ten power transistors. The work in this paper converts AC to dual-regulating DC directly in only one stage with only four power transistors. The peak efficiency of this system can reach 86% when the output power ranges from 15 mW to 47 mW due to the PSM modulation. However, this system can only realize two similar outputs, and the output power is limited.

**Table 2.** Comparison to state-of-the-art of wireless power receivers.

	ISSCC [13]	JSSC [5]	TPE [7]	JSSC [12]	CICC [15]	TPE [1]	This Work
<b>Technology</b>	0.18 $\mu\text{m}$ –CMOS	0.35 $\mu\text{m}$ –BCD	0.35 $\mu\text{m}$ –CMOS	0.35 $\mu\text{m}$ –CMOS	0.18 $\mu\text{m}$ –CMOS	0.18 $\mu\text{m}$ –CMOS	0.18 $\mu\text{m}$ –CMOS
<b>Frequency</b>	200 KHz–3.3 MHz	6.78 M	6.78 M	6.78 M	13.56 M	6.78 M	125 KHz
<b>Receiver structure</b>	rectifier	rectifier + charge bump	rectifier + SIMO	rectifier	dual-output rectifier	rectifier	dual-output rectifier
<b>Control scheme</b>	Timing Controller	PWM	3–mode	PWM	Close-loop Delay Controller	Hysteretic control	PSM
<b>Power switches</b>	4	7	8	4	10	4	4
<b>Power stages</b>	2	2	2	1	1	1	1
<b>Off-chip components</b>	1 cap	1 cap	4 cap + 1 ind	1 cap	8 cap	1 cap	2 cap
<b>Output voltages</b>	1.8 V	5 V	1.8 V + 3.8 V	5 V	1.8 V + 2.75 V	3.3 V	1.8 V + 2 V
<b>Number of outputs</b>	1	1	2	1	2	1	2
<b>max.POUT</b>	10 mW	6 W	0.6 W	6 W	7.1 mW	1.98 W	47 mW
<b>max.PCE</b>	87.10%	86% *	80.50%	92.2% #	79%	92.14% #	86%
<b>Cross regulation</b>	NA	NA	NA	NA	NA	NA	unnoticeable

#: need one extra on chip inductor. \*: single output rectifier.

## 5. Conclusions

This paper presents a single-stage, dual-output wireless power receiver that adopts pulse skip modulation to save power. The system uses only four power transistors and no inductor to realize dual-output in only one stage. Additionally, this architecture can be integrated into a small chip to reduce costs. PSM is adopted to regulate dual outputs and to save power. The circuit is designed by a 0.18  $\mu\text{m}$  CMOS process. Additionally, the dual-output voltages are 1.8 V and 2 V. The output voltages are charged from different phases of the input signal; therefore, there is no cross-regulation in this system. The peak efficiency of the system can reach 86% when the output power ranges from 15 mW to 47 mW.

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