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Editorial

Design of Ultra-Low Voltage/Power Circuits and Systems

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Over the last years, the Internet of Things (IoT), wireless sensor networks and the emergence of other energy-constrained applications have pushed the demand for low-cost systems-on-chip solutions, entailing tight area and small power/voltage budgets [1,2]. In response to such requests, considerable effort has been spent in defining novel ultra-low voltage/power analog (e.g., [3–6]), mixed-signal (e.g., [7–9]), digital circuits (e.g., [10–12]), as well as energy-efficient and high-density memory solutions [13–16].

In the above context, this Special Issue features five research papers [17–21] that present original contributions for a wide range of applications, including image sensors, sensor interfaces, cryogenic computing, deep neural networks, and memory design. These five papers are briefly summarized as follows. A. M. Brunetti et al. [17] presented a logarithmic six-transistor pixel circuit for CMOS image sensors, which exploits low-voltage photodiode biasing to enable low dark current. The proposal was experimentally validated in 110 nm CIS process technology and compared against the typical logarithmic three-transistor pixel circuit. Experimental results prove that, when compared to the standard design, the proposed implementation achieves a dark current reduction by 34.5 dB at the expense of three additional transistors. This improvement in dark current also translates into increased dynamic range, reaching a value larger than 160 dB, which is a record for logarithmic pixels.

A. Ria et al. [18] proposed a low-power CMOS bandgap voltage reference for sensor interfaces, which is able to work with supply voltages down to 0.5 V. The proposal is based on a classic CMOS bandgap core, whose design was properly modified to be compatible with low-threshold or zero-threshold MOSFETs. The core was combined with a recently proposed switched capacitor, inverter-like integrator implementing offset cancellation and low-frequency noise reduction techniques. Both theoretical analysis and numerical simulations were presented to describe circuit operation. A prototype was also fabricated in a commercial 180 nm CMOS technology. The experimental results show that the proposed circuit provides a reference voltage of 220 mV at 0.5 V supply with a power consumption of 315 nW and a temperature sensitivity of 45 ppm/°C across a 10–50 °C temperature range.

E. Garzón et al. [19] investigated three appealing embedded memory technologies such as six-transistor static random-access memory (6T-SRAM), gain-cell embedded DRAM (GC-eDRAM) and non-volatile spin-transfer torque magnetic random access memory (STT-MRAM) under cryogenic (77 K) operation. The study was carried out using a commercial 65 nm 1.2 V CMOS technology fully calibrated under silicon measurements at cryogenic temperatures. The obtained results demonstrate that as the temperature goes down to 77 K, 6T-SRAM exhibits slight improvements in static noise margin (SNM) during hold and read operations, while suffering from lower (−16%) write SNM. GC-eDRAM shows significant benefits under cryogenic operation with read voltage margins and data retention time improved by about 2× and 900×, respectively. STT-MRAM based on single- or double-barrier magnetic tunnel junctions (MTJs) exhibit higher read voltage sensing

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margins (36% and 48%, respectively) at the cost of longer write access time (1.45× and 2.1×, respectively). Overall, the performed analysis points out that embedded memory technologies can be attractive candidates for cryogenic applications not only for high-performance computing but also for bridging the gap from room temperature to the realm of cryogenic applications that operate down to liquid helium temperatures and below.

M. Vatalaro et al. [20] presented a novel low-power, low-voltage analog implementation of the softmax function to be used in deep neural network (DNN) applications. The proposal is based on a modular and scalable PMOS-only design, which enables electrically adjustable amplitude and slope parameters. More specifically, the architecture is composed of input current–voltage linear converter stages, MOSFETs operating in a subthreshold regime implementing the exponential functions, and analog divider stages. The softmax circuit was designed in 180-nm CMOS technology and validated through circuit simulations. The obtained results show that the circuit is able to operate at supply voltages down to 0.5 V. A 10-input/10-output implementation occupies a chip area of 2570 μm^2 with a power consumption of only 3 µW, thus resulting in a very compact and energy-efficient solution as compared to digital implementations.

K. Vicuña et al. [21] presented a 1024 bit self-adaptive memory address decoder based on the Dual Mode Logic (DML) design style to allow working in two modes of operation, i.e., dynamic for high-performance and static for energy-saving. The main novelty of the proposal concerns the design of a controlling mechanism that mixes both of these modes of operation to simultaneously benefit from their inherent advantages. When performance is the primary target, the mixed operating mode is enabled. As a consequence, the self-adjustment mechanism identifies at run time the logic gates that have to work in the energy-efficient mode (i.e., static mode), while those belonging to the critical path operate in the faster dynamic mode. In addition, the decoder can operate in the fully static mode to achieve the lowest energy consumption when speed is not a primary concern. The memory address decoder design was implemented in 65-nm CMOS technology and simulated to be compared against other logically equivalent dynamic and static solutions. When operating in the mixed mode, the proposed circuit exhibits negligible speed reduction (8.7%) in comparison with a dynamic logic-based design, while presenting significantly reduced energy consumption (28%). On the contrary, further energy is saved (29%) with respect to conventional logic styles when the circuit works in the fully static mode.

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References

1. Alioto, M. *Enabling the Internet of Things: From Integrated Circuits to Integrated Systems*; Springer: Cham, Switzerland, 2017.
2. Kim, B.; Lee, S.; Trivedi, A.R.; Song, W.J. Energy-Efficient Acceleration of Deep Neural Networks on Realtime-Constrained Embedded Edge Devices. *IEEE Access* **2020**, *8*, 216259–216270. [CrossRef]
3. Seok, M.; Kim, G.; Blaauw, D.; Sylvester, D. A portable 2-transistor picowatt temperature-compensated voltage reference operating at 0.5 V. *IEEE J. Solid-State Circuits* **2012**, *47*, 2534–2545. [CrossRef]
4. Fassio, L.; Lin, L.; De Rose, R.; Lanuzza, M.; Crupi, F.; Alioto, M. Trimming-Less Voltage Reference for Highly Uncertain Harvesting Down to 0.25 V, 5.4 pW. *IEEE J. Solid-State Circuits* **2021**, *56*, 3134–3144. [CrossRef]
5. Nguyen, V.; Schembari, F.; Staszewski, R.B. A Deep-Subthreshold Variation-Aware 0.2-V Open-Loop VCO-Based ADC. *IEEE J. Solid-State Circuits* **2021**. [CrossRef]
6. Fassio, L.; Lin, L.; De Rose, R.; Lanuzza, M.; Crupi, F.; Alioto, M. A 0.6-to-1.8 V CMOS Current Reference with Near-100% Power Utilization. *IEEE Trans. Circuits Syst. II Express Briefs* **2021**, *68*, 3038–3042. [CrossRef]
7. Abdelraheem, M.; Abdelhafeez, M.; Nassr, A. IoT-Based Interdigital Capacitance Sensing System for Damage Detection in CFRP-Concrete Structures. *IEEE Access* **2021**, *9*, 138658–138667. [CrossRef]

8. Wang, X.; Wang, P.H.P.; Cao, Y.; Mercier, P.P. A 0.6 V 75nW all-CMOS temperature sensor with 1.67 m° C/mV supply sensitivity. *IEEE Trans. Circuits Syst. I Regul. Pap.* **2017**, *64*, 2274–2283. [CrossRef]
9. Zambrano, B.; Garzón, E.; Strangio, S.; Crupi, F.; Lanuzza, M. A 0.05 mm^2, 350 mV, 14 nW Fully-Integrated Temperature Sensor in 180-nm CMOS. *IEEE Trans. Circuits Syst. II Express Briefs* **2021**. [CrossRef]
10. Taco, R.; Levi, I.; Lanuzza, M.; Fish, A. An 88-fJ/40-MHz [0.4 V]–0.61-pJ/1-GHz [0.9 V] Dual-Mode Logic 8×8 bit Multiplier Accumulator with a Self-Adjustment Mechanism in 28-nm FD-SOI. *IEEE J. Solid-State Circuits* **2019**, *54*, 560–568. [CrossRef]
11. Gebregiorgis, A.; Tahoori, M.B. Fine-Grained Energy-Constrained Microprocessor Pipeline Design. *IEEE Trans. Very Large Scale Integr. VLSI Syst.* **2018**, *26*, 457–469. [CrossRef]
12. Shavit, N.; Stanger, I.; Taco, R.; Lanuzza, M.; Fish, A. A 0.8-V, 1.54-pJ/940-MHz dual-mode logic-based 16× 16-b booth multiplier in 16-nm FinFET. *IEEE Solid-State Circuits Lett.* **2020**, *3*, 314–317. [CrossRef]
13. Garzón, E.; Greenblatt, Y.; Harel, O.; Lanuzza, M.; Teman, A. Gain-Cell Embedded DRAM Under Cryogenic Operation—A First Study. *IEEE Trans. Very Large Scale Integr. VLSI Syst.* **2021**, *29*, 1319–1324. [CrossRef]
14. IRDS-IEEE. International Roadmap for Devices and Systems—Cryogenic Electronics and Quantum Information Processing. Available online: https://irds.ieee.org/editions/2021 (accessed on 1 February 2022).
15. Yang, Y.; Park, J.; Song, S.C.; Wang, J.; Yeap, G.; Jung, S.O. Single-Ended 9T SRAM Cell for Near-Threshold Voltage Operation with Enhanced Read Performance in 22-nm FinFET Technology. *IEEE Trans. Very Large Scale Integr. VLSI Syst.* **2015**, *23*, 2748–2752. [CrossRef]
16. Garzón, E.; De Rose, R.; Crupi, F.; Teman, A.; Lanuzza, M. Exploiting STT-MRAMs for cryogenic non-volatile cache applications. *IEEE Trans. Nanotechnol.* **2021**, *20*, 123–128. [CrossRef]
17. Brunetti, A.M.; Choubey, B. A low dark current 160 dB logarithmic pixel with low voltage photodiode biasing. *Electronics* **2021**, *10*, 1096. [CrossRef]
18. Ria, A.; Catania, A.; Bruschi, P.; Piotto, M. A Low-Power CMOS Bandgap Voltage Reference for Supply Voltages Down to 0.5 V. *Electronics* **2021**, *10*, 1901. [CrossRef]
19. Garzón, E.; Teman, A.; Lanuzza, M. Embedded Memories for Cryogenic Applications. *Electronics* **2022**, *11*, 61. [CrossRef]
20. Vatalaro, M.; Moposita, T.; Strangio, S.; Trojman, L.; Vladimirescu, A.; Lanuzza, M.; Crupi, F. A low-voltage, low-power reconfigurable current-mode softmax circuit for analog neural networks. *Electronics* **2021**, *10*, 1004. [CrossRef]
21. Vicuña, K.; Mosquera, C.; Musello, A.; Benedictis, S.; Rendón, M.; Garzón, E.; Prócel, L.M.; Trojman, L.; Taco, R. Energy Efficient Self-Adaptive Dual Mode Logic Address Decoder. *Electronics* **2021**, *10*, 1052. [CrossRef]