

Article

Design and Implementation of Low Noise Amplifier Operating at 868 MHz for Duty Cycled Wake-Up Receiver Front-End

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Abstract: The integration of wireless communication, e.g., in real- or quasi-real-time applications, is related to many challenges such as energy consumption, communication range, quality of service, and reliability. The improvement of wireless sensor networks (WSN) performance starts by enhancing the capabilities of each sensor node. To minimize latencies without increasing energy consumption, wake-up receiver (WuRx) nodes have been introduced in recent works since they can be always-on or power-gated with short latencies by a power consumption in the range of some microwatts. Compared to standard receiver technologies, they are usually characterized by drawbacks in terms of sensitivity. To overcome the limitation of the sensitivity of WuRxs, a design of a low noise amplifier (LNA) with several design specifications is required. The challenging task of the LNA design is to provide equitable trade-off performances such as gain, power consumption, the noise figure, stability, linearity, and impedance matching. The design of fast settling LNA for a duty-cycled WuRx front-end operating at a 868 MHz frequency band is investigated in this work. The paper details the trade-offs between design challenges and illustrates practical considerations for the simulation and implementation of a radio frequency (RF) circuit. The implemented LNA competes with many commercialized designs where it reaches single-stage 12 dB gain at a 1.8 V voltage supply and consumes only a 1.6 mA current. The obtained results could be made tunable by working with off-the-shelf components for different wake-up based application exigencies.

Keywords: wireless sensor networks; wake-up receiver; duty cycled; low noise amplifier; sensitivity; power consumption; radio frequency; hardware challenges; performances analyses



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1. Introduction

With recent technological advancements, the internet of things (IoT) is nowadays at the cutting edge of transforming various fields to a level of smartness by storing and processing data in a distributed manner to enhance productivity.

Internet of things (IoT) technology is based on powerful wireless devices interconnected in a complex ecosystem that enables one to gather, share, and analyze information and take actions appropriately [1]. These wireless devices are called sensor nodes, dispersed through different technologies and communicating at different frequency levels in a wide network. A number of applications such as weather [2], health, military, transport, localization [3,4], and smart automotive depend on the potential of sensor nodes to overcome the challenges of wireless sensor nodes [5]. In contrast, the specific requirements and performances for sensor nodes obviously depend on the application they will serve [6], the effect to be sensed, the amount of the data rate transferred [7], and subsequently on the power consumed [8]. Data rate, transmission power, and power consumption in the sensor node are also related to the operating frequency.

Some RF bands, such as 2.4 and 5 GHz, are highly populated bands that enable connectivity and coverage but face much interference from the extensive demand of other

devices. Additionally, those RF bands suffer from path losses, low communication range, and require multi-hop communications, which results in the need for a large number of devices connected to the network [9]. The results of this are increasing complexity and synchronization issues. On the other hand, operating in sub-gigahertz band frequencies, e.g., the 868 MHz band, seems to be a promising solution for the improvement of coverage and connectivity [10]. Additionally, it enhances the communication range in indoor applications with many obstacles and distributing factors. Furthermore, improving the receiver node's sensitivity could also enhance the communication range alongside the operating frequency.

Wireless communication is defined as “over the air” to create a telecommunications channel between two points. Technologies differ from the used frequency channel and the operating techniques used for successful radio transmission. In recent works, many technologies have been introduced such as infrared communication, satellite communication, microwave transmission, wireless fidelity (Wi-Fi), worldwide interoperability for microwave access (WiMAX), long term evolution (LTE), the field area network (FAN), etc. [11]. Aiming for reliable and power-efficient wireless communication is the common concern of all used technologies, and that is the reason behind implementing smart techniques for improving network specifications. An example is code division multiple access (CDMA), which is a channel multiple access technique, where several transmitters can send information simultaneously over a single communication channel [12]. This approach improves the quality of service and real-time communication schemes which reduce the consumed energy and guarantee better link qualifications. Recent research using the efficient uplink protocol works within the range of mW-W of power consumption, which is much higher than the required power consumption for the proposed sensor nodes. Investigating hardware-based techniques which implement a pure asynchronous rendezvous can decrease the power hunger of the normal receivers compared with other technologies.

The implementation of the wake-up receiver (WuRx) nodes is an essential investigation in the WSN. The WuRx approach represents a promising solution with which to implement an energy-efficient network operation with low latency [6]. Alongside always-on transceivers, power gates with an appropriate duty cycle are also investigated. Among the challenges of wireless sensor nodes, the communication range is not the only essential matter for improving internet of things (IoT) applications; the minimization of the power consumption of sensor nodes is nowadays also a concern of researchers and developers in this field [13]. Furthermore, maximizing the battery life-time is a crucial parameter for energy-efficient applications [14].

The standard building block of a wake-up receiver circuit is based on passive components and called the direct RF architecture as presented in Figure 1. It is an always-on circuit which has the role of identifying the wake-up packet (WuPt). Once the identifier of the WuRx recognizes that the received telegram corresponds to a WuPt, an interruption is generated and sent to the main radio, which changes the state immediately from sleep to active.

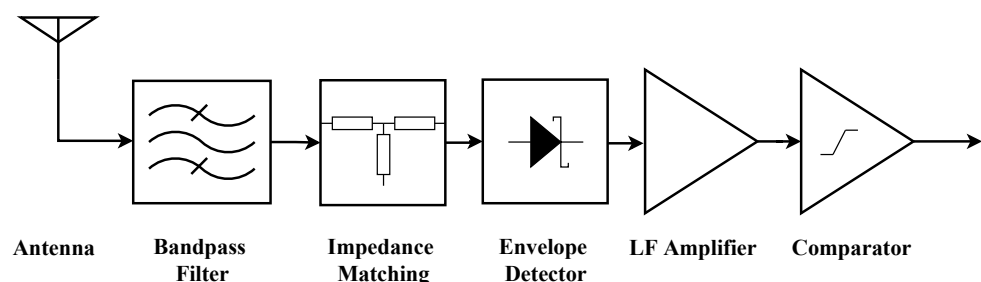


Figure 1. The architecture of the wake-up receiver based on passive components according to [15].

WuRx nodes are characterized by ultra-low battery-powered nodes, typically consume below 10 μ W [16] and ensure low latency. However, their sensitivity is related to the

adopted architecture and whether it includes an LNA in the receiver front end or not. As with many other standard receivers, the integration of an LNA block in the front-end antenna has the role to boost the incoming RF signals and detect the lower ones.

In WuRx nodes based on direct RF architectures, many issues related to communication range and coverage appear while deploying a wireless network. This sensitivity limitation affects the performance of the whole network, while with the development of tuned RF (TRF) architecture with the integration of LNA in the receiver front-end, the limitation of sensitivity related to the envelope detector was improved.

Although many works with different technologies are available for the design of LNA, the requirements of LNA for a duty-cycled WuRx should be adhered to so as to maintain the overall circuit performances. The exigencies for designing an LNA for duty-cycled WuRx are primarily an ultra-low power consumption with good sensitivity and latency as well as settling time.

This work illustrates in detail the theoretical background for the design of the LNA with various trade-off performances. Additionally, the design is well structured from the simulation issues and hardware implementation points of view. The last part is dedicated to comparing the results of the designed LNA with those of a commercial off-the-shelf (COTS) LNA. MAX2640 is selected to be integrated into the same duty cycled WuRx board for accurate comparison and specific power consumption calculation. A discussion is also undertaken to evaluate the achieved results.

2. Low Noise Amplifier in Radio Frequency Front-End Antenna

Radio frequency (RF) amplifiers are indispensable to any wireless system. The RF amplifiers act as power amplifiers in transmitters or LNAs in the receivers. This paper focuses on the main functionality of the LNA, which is placed on the receiver side. In addition, several performances such as ultra-low power consumption and good sensitivity behavior should be considered in the designed LNA in the interest of implementing a WuRx node circuit operating at 868 MHz frequency [15].

As wireless communication faces excessive noise, which is largely produced through the crosswalk of an electromagnetic wave in the air, the LNA could overcome this problem by amplifying the very low-power signal with minimal additive distortion at the receiver input. However, the noise present at the input of the amplifier could also introduce some amplification. Within the design, additional noise should be treated and minimized. In the front-end, the LNA is placed after a bandpass filter to improve the selectivity of the reception and to suppress the parasitic signals outside the 868 MHz. Figure 2 shows the placement of LNA in the front-end antenna.

The amplitude of the weak signal entering the LNA is increased and prepared to be treated by the rest of the blocks. The treated signal is later introduced into the down-conversion mixer, where the signal's frequency will be reduced. Thus, the rest of the blocks of the receiver operate at a lower frequency than the frequency of the LNA and mixer. It is essential to have an LNA with high performance in order to ensure the reliability of data transmission.

The main challenge of an LNA design is to make a trade-off between the following performances:

- High gain;
- Low power consumption;
- Minimum noise figure;
- Good matching at input and output;
- Stable system;
- Linearity within its operational band.

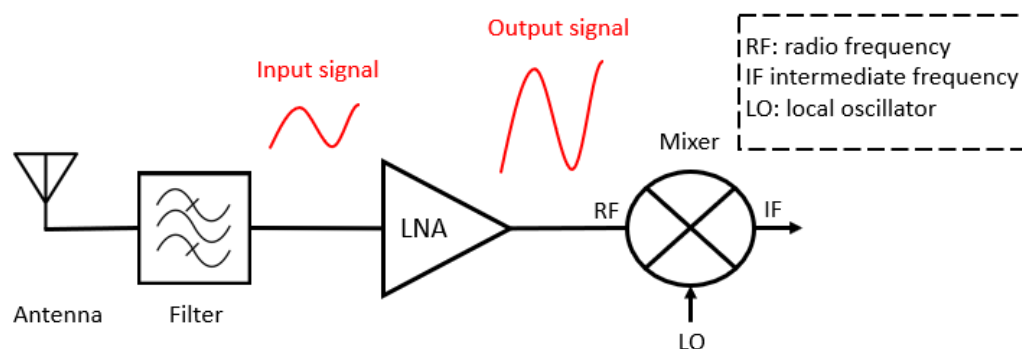


Figure 2. Low noise amplifier (LNA) block in front end antenna.

In the literature, LNA is used in many different fields [17] including medical, transport, military, etc. The main purpose in various applications is always to increase gain in the receiver path with a minimum signal-to-noise ratio (SNR). The selection of transistors as well as the number of cascaded stages determine the type of LNA design.

2.1. Design and Implementation of Low Noise Amplifier from State of the Art Overview

In advanced wireless communication research, the increasing demand for receiver sensitivity has produced an exciting amount of work on LNA designs. The current architectures operate in different communication frequency ranges and utilize different topologies based on a bipolar junction transistor (BJT) or field-effect transistor (FET). Regarding design challenges, the LNAs presented in the state of the art (SoA) or in the commercialized prototypes tend to balance performances and provide a clear trade-off. For most internet of things (IoT) application scenarios based on WuRx, a sensitivity level of better than -70 dBm is required. However, in the state of the art, many WuRx works, including LNAs, either focus on high sensitivity with huge energy consumption or emphasize ultra-low power consumption together with low sensitivity.

An in-depth study of different LNA designs was conducted to meet the desired requirements. Table 1 presents some LNA designs which are selected based on their architectural performances. Most of the selected LNA designs are based on metal-oxide semiconductor (CMOS) technology, representing the first selection criterion that did not match the required performances. This work will be developed based on discrete components due to its low-cost implementation, also for the reason that designing an RF circuit may lead to plenty of frequency problems such as shift and drift in magnificent proportions. Thus, using off-the-shelf components provides more flexibility in manufacturing and enhances moment-to-moment revision and changes in the architecture. The frequency shift problem could be solved by hardware tuning using lab equipment.

Table 1. Selection of different LNA designs operating in different frequency ranges.

Reference	Technology	Frequency (GHz)	Gain (dB)	Supply Current (mA)	Supply Voltage (V)	Settling Time (ns)	Noise Figure (dB)
[18]	CMOS	5–7.5	18–21	2.2	1	9.5	6.2–7.8
[19]	CMOS	0.405	53.5	0.47	1.8	100	3.19
[20]	Discrete	1.9	16	65	3	-	0.8
[21]	CMOS	0.7–9	28.3	17.8	1.2	-	3.38
[22]	CMOS	2.4	20	0.75	2.5	200	3.3
[23]	CMOS	2	24	5	1	-	1.9

“-”: Not Available.

Taking as an example the design presented in [21], which is based on off-the-shelf components, the 868 MHz band was included within the operational frequency range; however, the total current consumption of the circuit is extremely high and failed to achieve the need for low power consumption for the WuRx.

Most of the LNA works in SoA are made for mobile and radar communication applications operating in wide and ultra-wide bands. Conversely, the proposed LNA is designed for operating in 868 MHz. Thus, it is another factor that enhances the uniqueness of this work.

The in-depth study of LNA designs provided in the SoA is essential to strengthen the theoretical background behind RF design, and also to discover different architectures, and extract weaknesses and strengths behind the use of transistors with the best operating points and the RF signal behavior through the adopted design. The design specifications for the WuRx application are detailed in the following section.

2.2. Aimed Design Specifications and Requirements

Many commercialized LNAs were selected to compare their performances with the desired ones and to investigate how far they can adhere to the need for a developed WuRx. Table 2 summarizes the selection of different LNA designs for various applications. The table illustrates some mounted evaluation boards of LNA operation in 868 MHz. The comparison among different commercially available products mentions the technology used as well as performance parameters.

Table 2. Comparative study of commercialized off-the-shelf LNAs.

LNA	Technology	Frequency (GHz)	Gain (dB) @868MHz	Supply Current (mA)	Supply Voltage (V)	Noise Figure (dB)
BGU7003 [24]	integrated	0.040–6	20	15	3	1
BGU8051X [25]	integrated	0.3–1.5	20	36	5	0.43
MAX2642 [26]	integrated	0.8–1	16	5.3	2.7–5.5	2.7
MAX2640 [27]	integrated	0.3–2.5	15	5.3	2.7–5	1.8

The trade-off between power consumption and gain is always a difficult task that can compromise the intended objectives. For example, BGU7003 and BGU8051X both reach a gain of 20 dB but consume, respectively, 15 mA and 36 mA, which can not be implemented in a circuit consuming some micro-watts in total.

The integration of LNA into WuRx should maintain the approach for ultra-low power consumption to conserve the overall system assumption [28]. Compared to SoA, all LNAs operating at 868 MHz are power hungry. Therefore, the designed amplifier should consider the current currying in a single amplification stage in the range of 1–2 mA, with a flexibility increase if the need for higher gain becomes apparent in the adopted application.

Considering the stable range for the transistor operating characteristics, non-elevation of the voltage supply for feeding the active device is also a significant factor in keeping low current consumption. On the other hand, the excessive noise in wireless communication, which is largely produced at the receiver front end of RF receivers, is an inherent problem.

To overcome this problem, it is necessary to design the LNA by considering the concept of amplifying the incoming weak signals without adding further noise stages and minimizing them. The noise figure in the designed RF amplifier should not exceed 2 dB for one stage.

One of the most critical design requirements is to treat the system's stability to ensure normal amplification behavior and avoid oscillating circuits. Stability is related to the determination of the S-parameters of the circuit, which also have the role of identifying the input and output return losses. Both factors should be kept below -10 dB to minimize reflections and ensure a maximum power transfer through the RF path.

Lastly, we mention the most critical design specification, which is the gain that situates the designed LNA well within the SoA by increasing the sensitivity of the receiver node. The mentioned design performances will be explained theoretically in the next section with the presentation of simulated results for each obtained parameter.

Achieving the simultaneous requirements of high gain, low current consumption, and a low noise figure are challenging tasks for balancing the trade-offs of the overall design. However, by analyzing Figure 3, it is clear that the specifications set for the present work are very well considered in terms of current market trends.

The main focus of this work is to provide a solid structured design for the development and optimization of LNA for a given set of performance parameters.

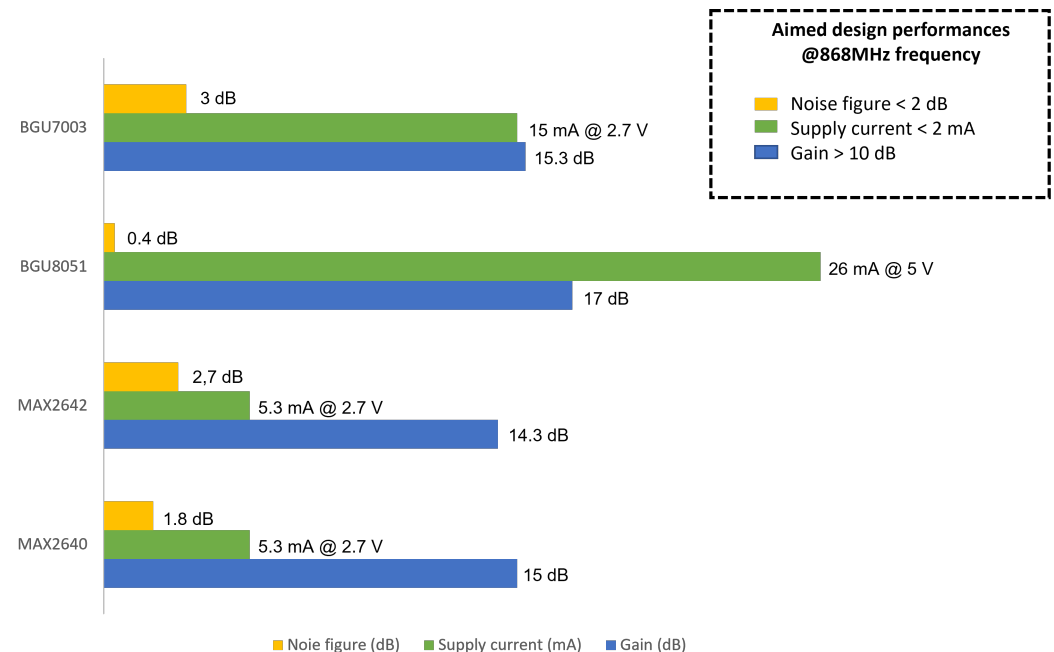


Figure 3. Identification of design requirements based on selected commercialized off-the-shelf LNA performance at 868 MHz.

3. Low Noise Amplifier Design Considerations and Simulation Results

In wireless communication systems, the LNA improves the receiver channel communication by boosting the received signal with the lowest possible noise figure (NF) addition. For an ideal LNA performance, all the design requirements should agree based on figures of merits such as stability, low noise figure, good gain, and excellent matching performance. All those performances were well studied and simulated to extract the best selection criteria for a stable LNA design.

3.1. Transistor Selection

A step that precedes the setting of the RF parameters is transistor selection which is the critical factor of the LNA design as long as the gain adopted in the LNA's complete circuit derives essentially from the transistor's internal gain. Additionally, the simultaneous requirements of the transistors are considered to be essential parameters for building the whole design. LNAs are constructed differently in the literature, either based on a bipolar junction transistor (BJT) or field-effect transistor (FET).

The meeting of requirements is also structured differently in both types. Field-effect transistors (FETs) feature better linearity and noise at a very high transition frequency [29]. Furthermore, they require proper circuit stabilization, as they are prone to oscillate due to their high switching capabilities. However, BJTs lead to a better speed at the same physical attitude and price, as they have very little input capacitance. They can also provide better gain performance. BJTs can support higher output currents for signal outputs and have a lower output impedance. This is a considerable advantage for amplifiers built to drive a low input impedance load or deliver significant amounts of power [30].

To conclude, the chosen transistor technology is the bipolar junction transistor (BJT) to achieve a low-cost LNA with a minimum number of external matching and biasing

networks as standard requirements. Furthermore, it provides a certain degree of flexibility in order to alternate all the parameters. In this work, different families of bipolar junction transistors (BJTs) were tested under specific conditions to extract their response to design requirements. Finally, BFP740 was selected due to its good compromise between high gain and a low noise figure together with the lowest possible power consumption.

3.2. Architecture of LNA

As described in Section 3.1, the choice for the proposed application is BJTs due to their high performance. To enhance good amplification of the incoming signal, the BFP740 transistors are mounted in a common emitter (CE) architecture and operated by using an alternating current (AC) as the input signal. Compared to the common base (CB) topology, the CE topology delivers good gain and noise performance in a narrow bandwidth. For this topology, the amplifier input is taken from the base terminal, the output is collected from the collector terminal, and the emitter terminal is common for both terminals [29].

Figure 4 shows the connection of the BFP740 in the proposed CE architecture, with the presence of a matching circuit to 50 Ohm in the input and output, respectively, using (C_{in1} , L_{in2} , C_{in2} for input and C_{out1} , C_{out2} and L_{out} for output). The inductors $L1$ and $L2$ handle the overpass of the RF signal through the micro strip-line from input to output. The resistance $R2$ is the biasing resistor, which is involved in determining the operating point. The resistors in the collector branch also serve to determine current consumption and introduce stability and linearity. The parallel capacitors decrease noise and also introduce the stability of the circuit.

During the simulation of the following design using the Advanced Design System (ADS), an important outcome is demonstrated: every component in the circuit does not have a single role. Working at a high-frequency level causes a very sensitive behavior for the component. Each element could introduce the role of others, and stability or matching could be degraded with every change in the simulation.

In conclusion, the tuning of certain values was performed carefully, considering after every iteration all the required performance of the LNA. Additionally, the trade-off between all desired performances is well studied to obtain the best results.

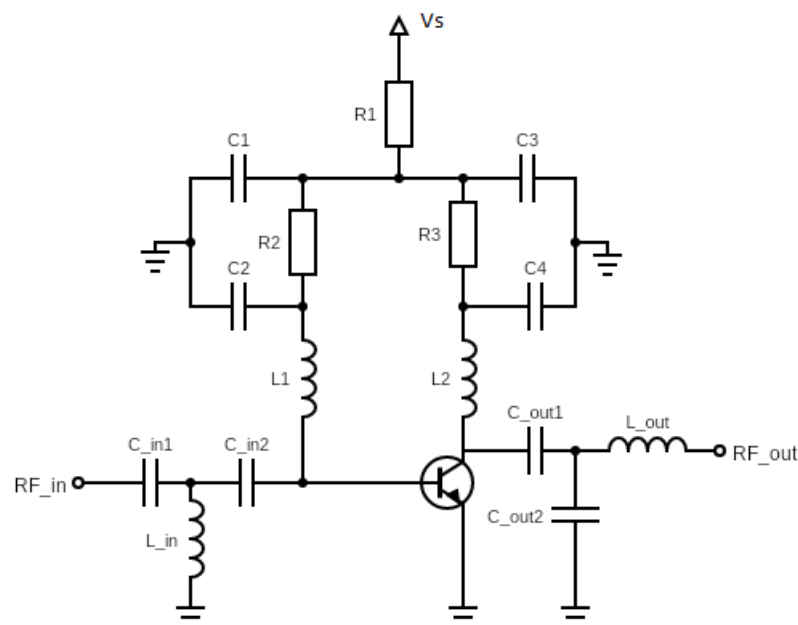


Figure 4. Common emitter LNA architecture based BFP740 transistor.

The studied architecture is implemented in ADS to determine the exact component values for an appropriate amplified signal behavior before implementation. ADS is a

powerful simulation tool introduced in the pre and post-hardware phase. Before the hardware implementation, structuring the architecture, configuring the exact lumped component values, and extracting the best simulation results is the aim of running several simulations. After mounting the chosen component onto the printed board, ADS was used again to correct several hardware problems faced during the implementation phase.

This simulator has various advanced capabilities in high-frequency simulations and electromagnetic behavior recognition. As the first viewpoint for CE topology, the selected BFP740 transistor was integrated into the ADS library and supplied under different voltage levels to determine the chosen transistor's operating conditions.

The Q-point is set at the lowest bias for a low-power design while providing the required gain. The design architecture is tuned with a DC power of 1–3 V, the gain was varied at 8–20 dB. Additionally, the current consumption changes with the tuning of voltage. The S-parameter resumes the input–output reflection factors, stability, noise figure, and gain resulting from S_{21} . Furthermore, the linearity and the amplified transient signal are simulated and illustrated in the following sections.

3.3. Scattering Parameters Characterization and Simulation

Since it is challenging to measure voltage or current in RF applications, the terms used to characterize the system performance and behavior are energy and power. The scattering parameters of the two-port system are the power characterization parameters. The S-parameters describe the relationship between the input and output of two ports of the system. A port is defined as input or output where voltage and current are delivered to ensure communication between two radios.

Considering the required LNA design as the RF system present in Figure 5, port 1 is the input impedance, and port 2 is the output impedance of the system. The scattering parameters are as follows:

- S_{11} is the input reflection coefficient;
- S_{22} is the output reflection coefficient;
- S_{21} is the forward transmission coefficient;
- S_{12} is the reverse transmission coefficient.

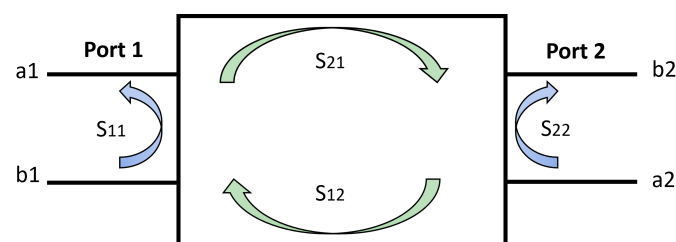


Figure 5. Identification of S-parameters in two-port system.

A small-signal AC simulation was performed to characterize a passive RF component and establish the small-signal characteristics of a device at a specific bias and temperature. The operating point was set with different power supply voltages in the range of 1–3 V. The operating point was set at 1 mA with a supply voltage of 1.8 V. For the device's most typical operating points, the manufacturer supplies embedded S-parameter data to analyze S-parameter performances in ADS. Using this setup, DC biasing is independent of the S-parameter analysis.

3.3.1. Impedance Matching

As mentioned in Figure 5, S_{11} and S_{22} determine the input and output reflection coefficients. They indicate how well the LNA is matched to the source and load 50 Ohm impedance at the 868 MHz design frequency band of interest. Accordingly, input and output return losses S_{11} and S_{22} , respectively, have to be kept below 10 dB for fewer

reflections and maximum power transfer. If the device has a poor output match, mismatch errors will degrade the whole LNA performance [31].

In the adopted architecture, the match is designed in the input port by combining two capacitors in the series and directing one inductor to the ground. In the output, the lumped component chosen for the matching is a capacitor, the inductor in the series, and one capacitor in the branch is matched to the ground. The matching system is verified using an S-parameter chart in ADS as shown in Figure 6. At 868 MHz, $S_{11} = -10.33$ dB and $S_{22} = -13.85$ dB.

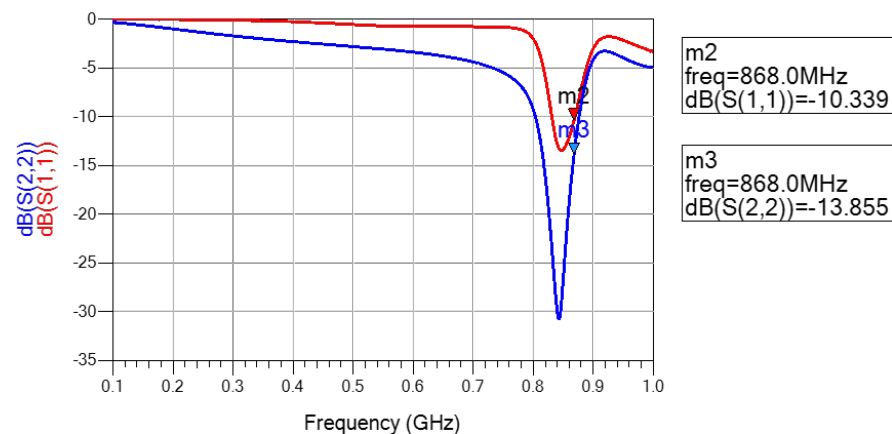


Figure 6. Input (S_{11}) and Output (S_{22}) reflection coefficients.

3.3.2. Stability

Stability is also a critical parameter used to determine the correct behavior of any amplifier. The main goal in designing the RF amplifier is to have an unconditionally stable circuit within a specific operating frequency to avoid turning it into an RF oscillator. The calculation of the Rollett stability factor (K-factor) using S-parameters derived from the simulation or from the hardware measurements is a common method by which to determine the stability of the designed system.

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} \quad (1)$$

$$\Delta = S_{11}S_{22} - S_{12}S_{21} \quad (2)$$

When $K > 1$ and $|\Delta| < 1$, the LNA is said to be unconditionally stable [31]. This is also called the small signal stability test, which is valid for a specific bias and frequency point. Therefore, the input and output ports are matched and the LNA is stable as described in the impedance matching section.

During the simulation, the stability of the circuit was verified at an early stage together with the matching phase. To ensure the stability of the amplifier over a wide range of frequency points, the factor K was tested on ADS with a frequency sweep of 0.5–1.5 GHz. With any tuning or value changes in the architecture, K is kept larger than the unity as shown in Figure 7. The circuit is stable and facilitates any connection to the passive elements at input and output ports. Additionally, a feedback loop analysis is run after every simulation phase; if K is less than one, the last modifications are reinitialized to avoid the transistor generating unwanted distortions or the circuit turning into an oscillator.

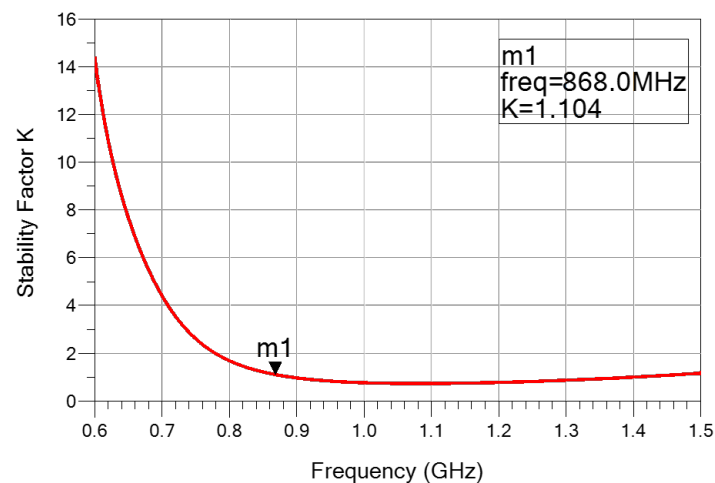


Figure 7. Simulation of the stability of the designed LNA circuit.

3.3.3. Gain

Theoretically, the gain is expressed in different ways as the transducer power gain, available power gain, and operating power gain. The main goal of the LNA design in the radio receiver is to amplify the incoming weak signals from the antenna and forward them to the rest of the circuit. Generally, the gain is the ratio between the output power of the LNA and its input power.

$$G_T = \frac{P_L}{P_S} = \frac{|S_{21}|^2 (1 - |\Gamma_L|^2) (1 - |\Gamma_S|^2)}{|1 - \Gamma_{in} \Gamma_S|^2 |1 - S_{22} \Gamma_L|^2} \quad (3)$$

The Equation (3) indicates that the transducer gain G_T is the ratio of the load impedance P_L and source impedance P_S [31]. Furthermore, G_T is expressed as function of S-parameters with $\Gamma_S = \Gamma_L$, which are, respectively, the reflection coefficients associated with the source impedance and the load impedance. When the two ports are connected to a source and load with impedance Z_0 , the result of $\Gamma_L = \Gamma_S = 0$ and the gain is expressed as the square value of S_{21}

$$G_T = |S_{21}|^2$$

In the literature, the gain level varies with the transistor and cascaded stages in the adopted architecture. The typical COTS LNA available in the market offer a gain level of up to 20 dB together with a low NF, but with a higher power consumption level, which does not match with the requirement of duty-cycled WuRx. With the designed prototype, the gain will reach a comparable level to that of the state of the art and also an ultra-low current consumption performance.

Many simulations were run to extract the best trade-off between gain and power consumption for the single and dual stages of the design. The implemented architecture of S_{21} was simulated as 14 dB gain, as mentioned in Figure 8. Table 3 presents other S_{21} levels simulated with the tuning of voltage supply for other optimizations through hardware tuning.

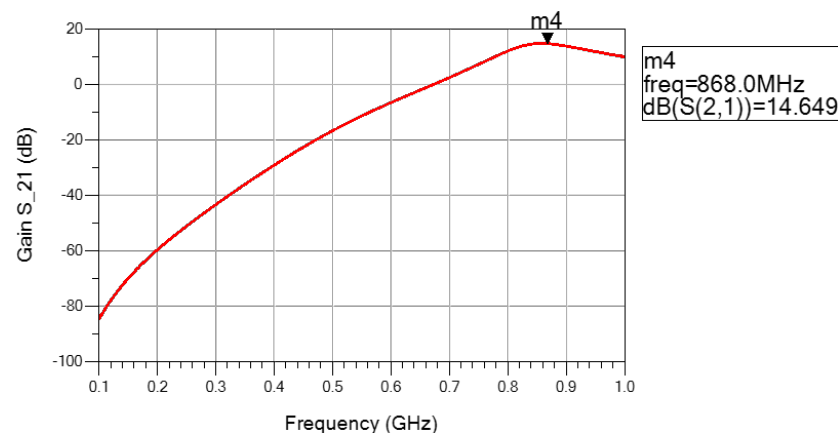


Figure 8. Simulation of (S_{21}) value at 868 MHz.

Table 3. Variation of gain and current consumption under tuned supply voltages.

Architecture	Single Stage				Dual Stage			
Supply voltage (V)	1.8	2	2.5	3	1.8	2	2.5	3
Gain (dB)	12	12.3	12	12.5	34.9	42	43	44
Supply current (mA)	1.6	2.2	2.6	3.4	3.2	3.5	5.3	6.8

3.3.4. Current Consumption

Current consumption is not related to a specific formula for an LNA design. The selection of passive components in the designed architecture results in feedback on the power consumption of the whole circuit. The LNA is designed to be placed in a duty-cycled WuRx node. Thus, the need for the lowest possible consumption of LNA should be maintained relative to the power need of the whole WuRx circuit. The comparison between LNA designs in the SoA and commercially available prototypes identifies a range in consumption for the LNA design of around 1–2 mA for a single stage.

To achieve the minimum power consumption, the total current derived from the circuit was calculated using the current probe in ADS mounted in a series with the resistor R1 from the mentioned architecture in Figure 4. The supply current was simulated by tuning the supply voltage, and an increase in gain with each successive voltage level was observed. Table 3 shows the simulated results. The obtained results for current and gain performances under different supply voltages are kept for further applications that require a higher communication range and to consolidate increased power consumption.

3.3.5. Noise Figure (NF)

The NF is also an important parameter that should be considered in the design, especially in designing a multi-stage cascaded amplifier. The noise of the LNA design should be minimized to avoid affecting the system sensitivity and to enhance further stages. Friis' Formula (4) explains the calculation of the NF of a cascade of stages, each with its noise factor and power gain (assuming that the impedance is well matched at each stage).

$$F = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \frac{F_4 - 1}{G_1 G_2 G_3} + \dots + \frac{F_n - 1}{G_1 G_2 G_3 \dots G_{n-1}} \quad (4)$$

F_i and G_i in the formula are, respectively, the NF and the gain for each stage.

NF is the practical noise figure of an RF network, NFmin is the ideal noise figure of a circuit and Mnf is the matched network factor.

$$NF = NF_{min} + Mnf$$

The LNA's NF should be kept as low as achievable to avoid affecting the overall system sensitivity. The lowest NF is not always found at the characteristic impedance Z_0

or at the conjugate match impedance that maximizes the gain. When conjugally matching the source impedance with an optimum impedance, the LNA has the lowest NFmin. In most cases, the input of an LNA will be matched for the minimum noise figure, which may result in a mismatch in terms of power performance. Increasing the biasing current for improving stability could also amplify the parallel current noise source, which will lead to undesirable behavior of LNA. Tuning and simulating light intervals can maintain the desired design performances without external distortions and noise.

An NFmin must be at its minimum, with the bias point of LNA selected to be around 1 mA. Figures 9 and 10 show the minimized NF performances for the proposed design at 868 MHz and at a low bias current for the operating transistor. NF = 0.629 dBm and NFmin = 0.516 dBm.

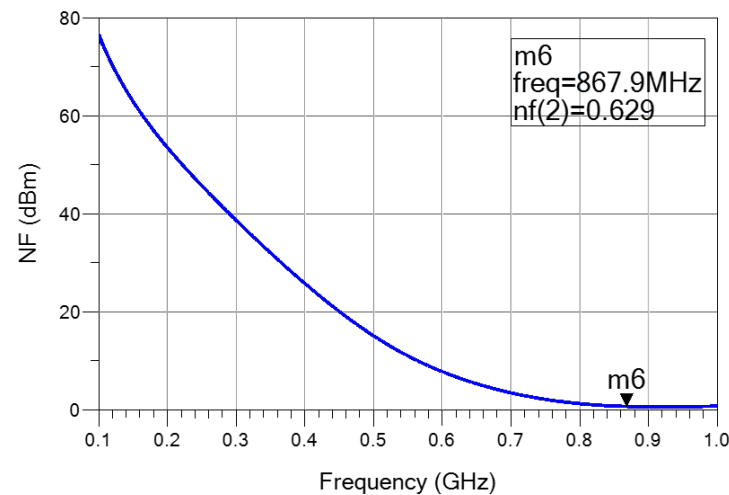


Figure 9. Simulation of the noise figure NF at 868 MHz.

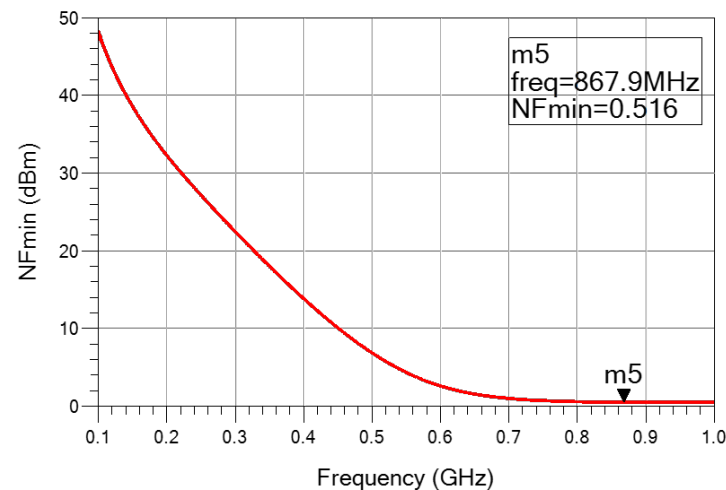


Figure 10. Simulation of the NFmin at 868 MHz.

3.3.6. Linearity

The investigation of LNA linearity requires the interpretation the gain compression and inter-modulation distortions against different input powers [29]. The 1-dB compression point (P_{1dB}) is the output power level at which the gain decreases by 1 dB from its constant value. The Equation (5) explains the estimation of the 1-dB compression point from the difference between the theoretical linear power P_{ThR} and P_{out}

$$P_{ThR} - P_{out} = 1 \text{ dB} \quad (5)$$

It is necessary to characterize the former in order to estimate the input power at which compression and distortions begin. For this purpose, a linearity analysis is extracted from the ADS simulation as shown in Figure 11. The linear region for the LNA is below -37.3 dBm, which is acceptable for the adopted approach.

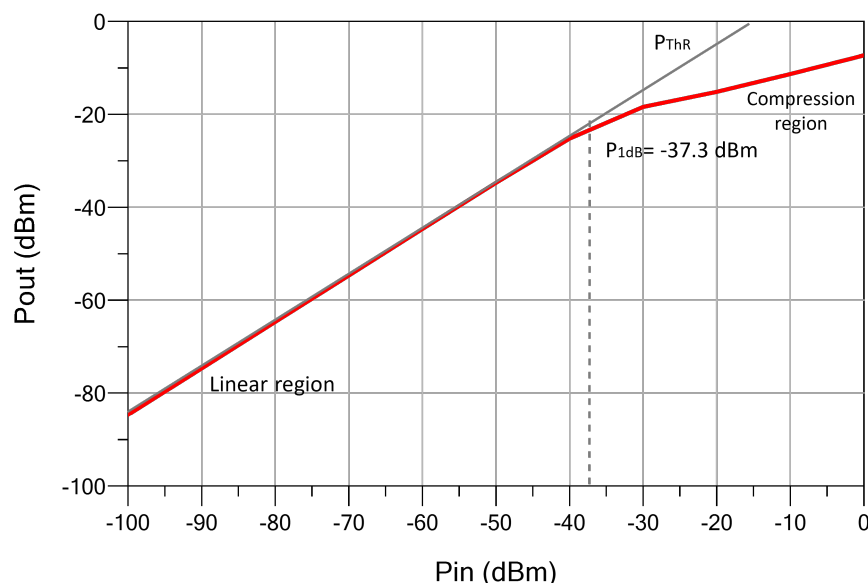


Figure 11. Simulation of 1-dB compression point for LNA.

3.4. Trade-Offs Between LNA Parameters

As described in the previous subsections, all the design parameters, such as stability, matching, linearity, consumption, noise figure, and gain, are equally important. To maximize the performance of the design, inevitable trade-offs should be considered, especially when RF components are highly sensitive, and a variation in some parameters could disturb the behavior of others [31].

Some parameters have priorities. For example, stability should never decrease below 1 so as to avoid an unstable circuit. In SoA, a placement of resistor load at the output of LNA has the role of improving the stability but can decrease the 3 dB level from the gain scale, which is not tolerable in this application.

Those consequences were detected during the simulation of the circuit. In this case, the decision is to eliminate the resistor at the output to avoid decreasing the gain. Additionally, careful tuning is reacquired to keep the k factor of stability greater than the unity.

Moreover, the output matching network of LNA is usually designed to achieve maximum gain using conjugate matching. Simultaneously increasing the demand for the high linearity of LNAs, the trade-off between good compression points for better linearity and high gain must be considered. The linearity is an essential aspect for the on–off keying (OOK) modulation that will be adopted in the WuRx nodes. On the other hand, gain and power consumption should be treated simultaneously. For example, the variation of resistor values in the collector branch could improve the gain slightly but increase the current of the whole circuit.

Additionally, the RF amplifier related to the Friis Formula (4) will introduce some additional noise by increasing the gain level and additional cascaded stages. There are other methods for minimizing the LNA noise by choosing low noise components, operating points, and circuit topologies. At this point, it is also mandatory to maintain a balance between all design goals such as power consumption and impedance matching.

The cost is also among the most important trade-offs that should be taken into consideration. During the selection of the lumped component or the printing process, a comparison is continuously taking place and the value for cost is considered. Furthermore, after comparison to the LNA design architectures in the SoA, a design process using off-the-shelf

and lumped element was selected to save both time and cost, as the integrated CMOS technology have a higher processing time and design expenditure.

To conclude, the LNA designed for duty-cycled WuRx imposes specific criteria and trade-offs between these parameters. Therefore, the primary important design task during the simulation is to have multiple considerations to prepare for the hardware phase, which is typically very sensitive in RF.

4. Hardware Implementation and Measurement Results

4.1. Challenges of LNA Printed Circuit Board (PCB) Design

After running many simulations on ADS and extracting the best performances of the circuit, the hardware design still has multiple challenges and requirements that should be carefully considered. The transitional phase first uses electromagnetic compatibility (EMC) simulations to connect the simulation world to the real one. Generating such advanced EMC simulations did not prevent certain complications, which were treated by manually tuning some of the components. Hence, the advantages of the off-the-shelf design are the ease of reparation and corrections, and the accessibility to any desired improvement. The design phase was treated carefully to ensure a robust and reliable behavior for RF components assembled for the implementation. The layout is worked out using Altium designer as an advanced designer tool. Many competencies in hardware designing characterize this phase because RF board stack-up requires attention to details such as isolation between traces and components, several PCB layers and arrangement, power supply decoupling, placement of components, etc.

Additionally, an adequate calculation of RF traces in which the incoming signals propagate could lead to transmission losses and interference issues. A ground plane is placed below the layer to make the current flow path as short as possible with the introduction of parallel vias to reduce the parasitic effect of capacitance and, therefore, to reduce the interference at 868 MHz frequency [32].

4.2. Hardware Testing Process

Hardware testing is usually performed in the transition phase between the simulation and emulation of the implemented PCB. For example, Figure 12 shows a single-stage LNA implemented under the first testing phase. For the LNA design, testing is needed to ensure that every circuit component performs well according to the specific requirements. The first testing setup is to verify the operating point of the transistor by measuring the current flow and base and collector voltage.

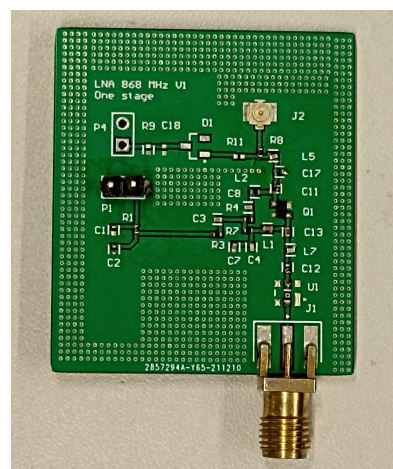


Figure 12. Assembled LNA Printed Circuit Board.

The amplifier gain was measured by feeding the LNA with a frequency generator and measuring the output with a spectrum analyser. The compression point and the

linearity were measured by this setup too. Figure 13 shows the measurement setup. The measurements will determine whether there exists adequate behavior within the circuit.

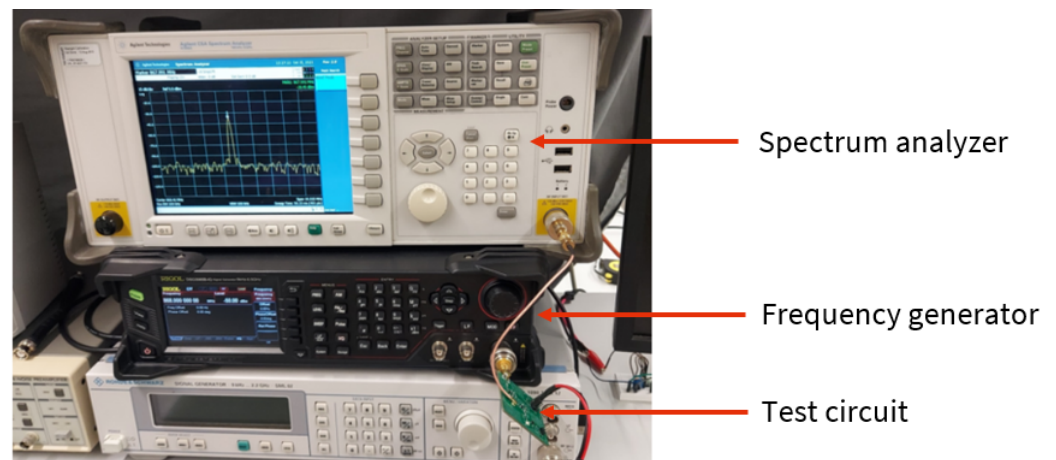


Figure 13. Measurement setup for measuring amplifier gain, compression point and linearity.

The final step in testing is the identification of the S-parameters using the Vector Network Analyser (VNA) as shown in Figure 14. The VNA was configured with its minimum output power $V_{out} = -45$ dBm.

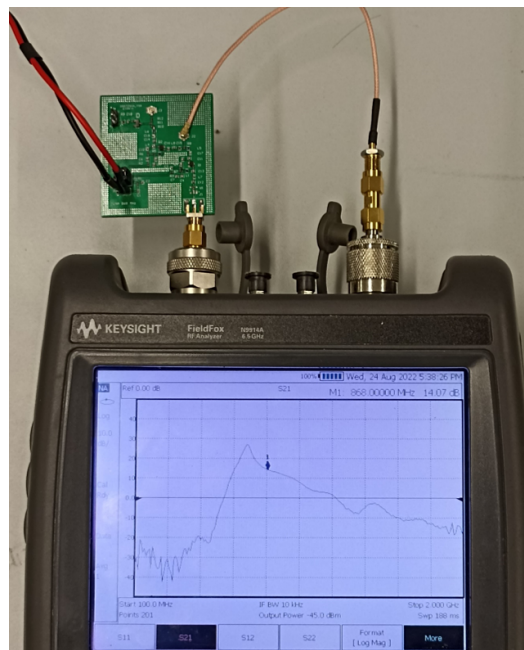


Figure 14. Measurement setup for measuring the S-parameters using a Vector Network Analyser.

4.3. Hardware Measurement Results

4.3.1. S-Parameters Measurements

As discussed in the previous section, S-parameters were measured using VNA and determine the overall related performances. The measurement results are depicted in Figure 15. The following measurements are the best obtained for matching input and output after many frequency shifts in the obtained values.

At 868 MHz, the return loss for the input port S_{11} was measured as -3.482 dB which is acceptable and did not affect the performance of the other parameters. The return loss for the output port S_{22} was -14.08 dB, which allows for a maximum power transfer for the envelope detector, which is placed after the LNA in the WuRx design. The value of S_{12}

is -27.33 dB, which is a more powerful reverse isolation that eases the task of impedance matching and improves amplifier stability. Finally, the S_{21} was measured as 14.68 dB, which reflects a good result for one-stage amplifier gain.

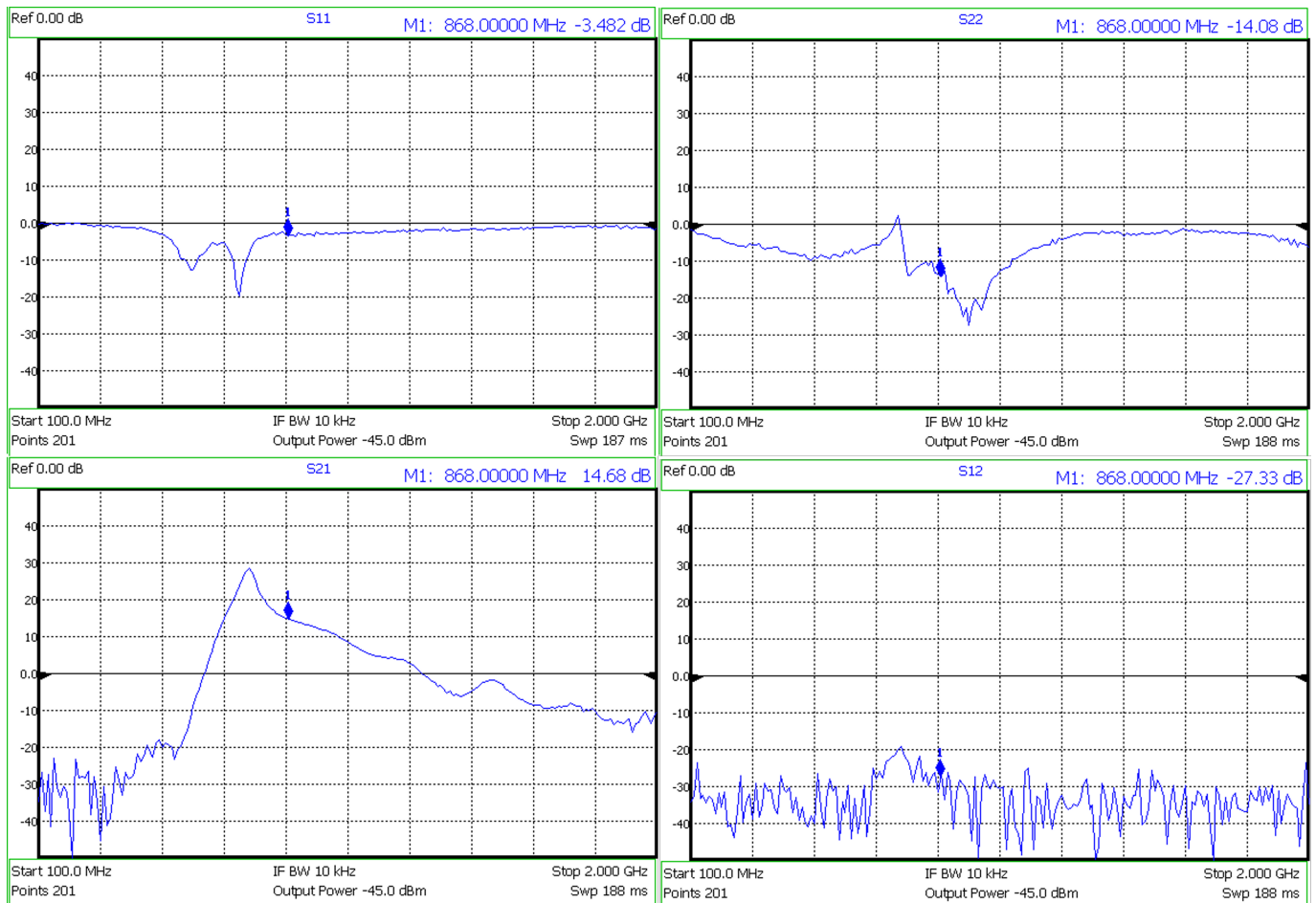


Figure 15. Results of S-parameters of the proposed amplifier.

The observation of S-parameters results at 747 MHz shows more promising values for S_{11} and S_{21} which reach, respectively, -17 dB and 27.48 dB. The results in this shifted frequency are the basis of future improvements aiming for a single-stage higher gain with better input impedance matching.

4.3.2. Behavior of Gain with the Variation of Input Power

The gain behavior with the input power variation at a fixed supply voltage was studied. Using a frequency generator in input enhances testing with very low input power to test the sensitivity of the front-end. Figure 16 confirms that the gain is stable while varying the incoming power. This measurement setup also concludes the system's stability and linearity within a lower power range.

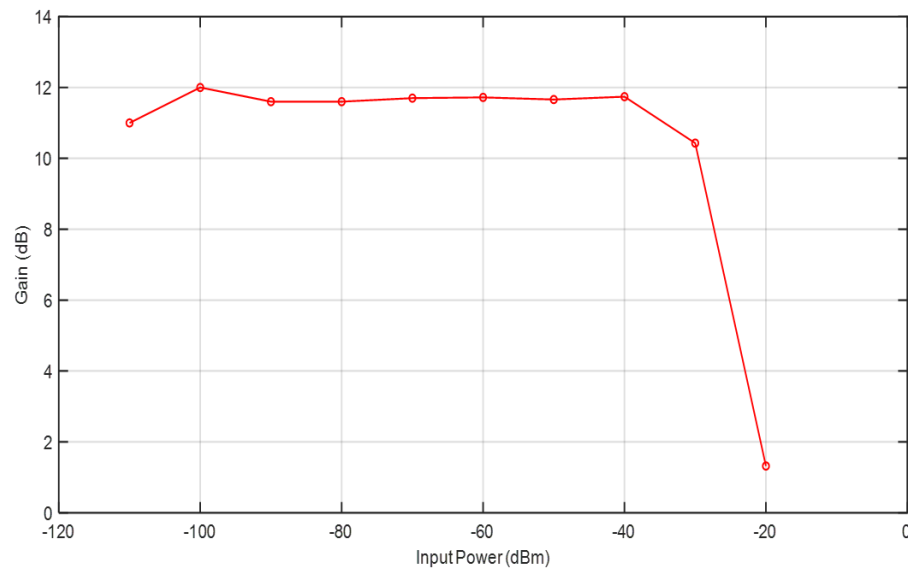


Figure 16. Gain behavior under input power variation.

4.3.3. Behavior of Gain and Current with the Variation of Supply Voltage

As in the simulation phase, the supply of the LNA was tuned in the range of 1.8–3.3 V to extract all working states for the circuit and conclude the best parameters trade-offs.

The curves in Figure 17 present both the simulation and measurement results for the gain and the supply current under the different voltage levels. The measurement results are very close to the simulation. For example, the gain indicates a slight increase where the current varies in the range of 1.8–3.5 mA.

This variation enhances the ability of the proposed LNA to work under different conditions and to serve different applications.

The decision of which supply voltage will be selected is related to the essential need for the duty cycled WuRx, which is the primary purpose of the LNA design. In addition to the need for ultra-low power consumption for this node, technologies deal with a moderate gain and avoid higher current levels. Furthermore, as the design is based on off-the-shelf technology, different architectures could be implemented for different wake-up-based applications.

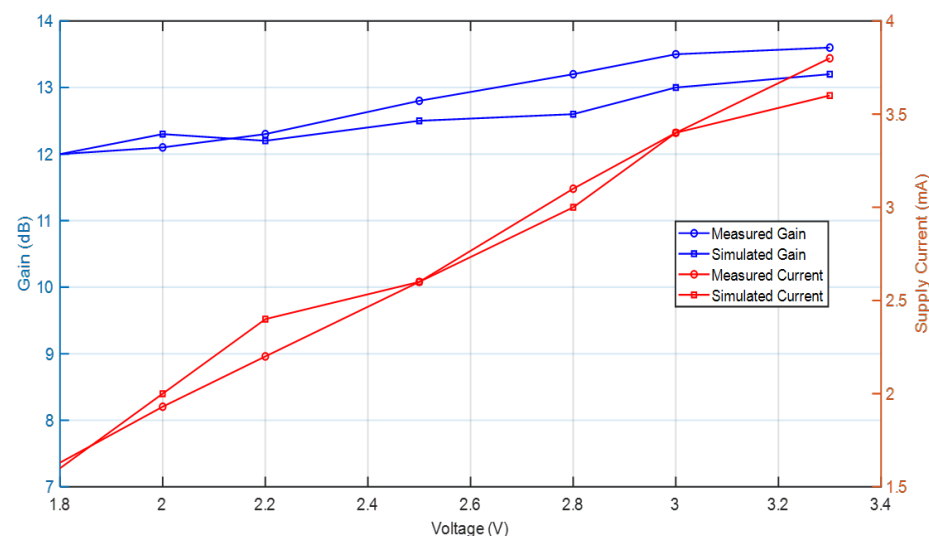


Figure 17. Behaviour of simulated and measured gain and supply current under tuned supply voltage 1.8–3.3 V.

4.3.4. Settling Time Measurement of Low Noise Amplifier

As the LNA circuit is designed for duty-cycled WuRx nodes, the settling of the circuit seems an essential factor that should be taken into consideration among the other design criteria. A higher speed of LNA settling following turning on will be advantageous in integrating other wake-up blocks.

The whole process is based on the duty cycled approach. A long turn-on time will degrade the capabilities of the receiver. In the COTS LNA works, the settling time is not often mentioned, making this parameter comparison relatively harder.

The settling time measurement setup is achieved after mounting the output of the LNA with an envelope detector designed based on SMS7630 diode from Skyworks and matched for the LNA measurements purposes. The observed delay between the LNA signal and transient response of the supply voltage and the rectified signal are illustrated in Figure 18. A delay of 47.7 ns can be observed between both signals, which is ultimately the settling time of the LNA. Compared to other LNA designs in Table 1, the obtained turn-on time of the designed amplifier is a promising result for integration with the WuRx.

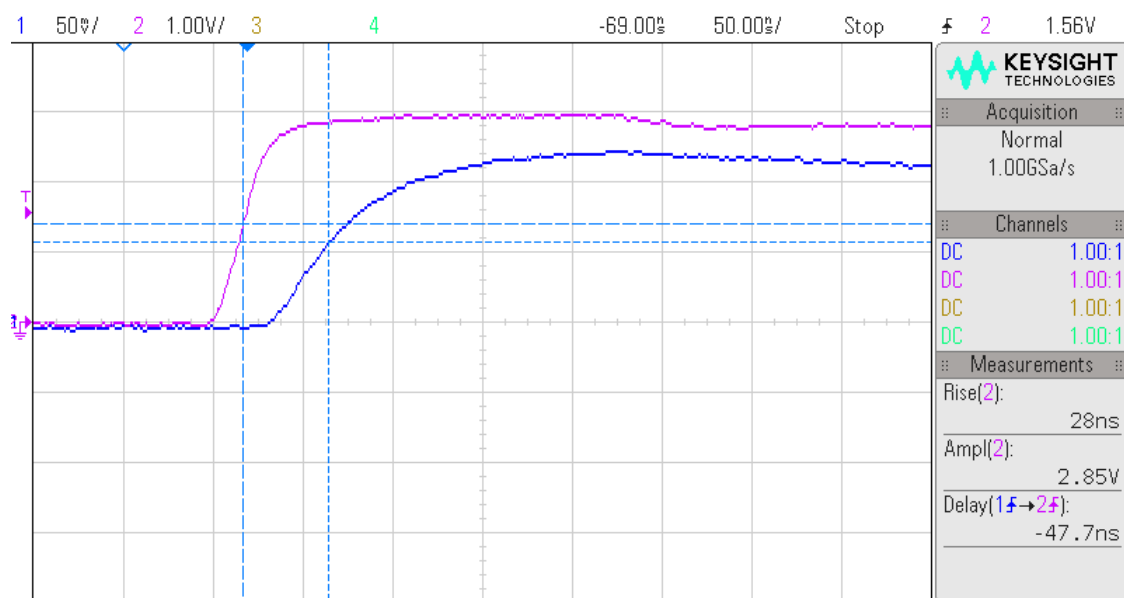


Figure 18. Settling time evaluation using envelope detector module. The pink color refers to the transient response of the supply voltage and the blue color refers to the LNA response signal with a delay of 47.7 ns

5. Performance Analysis for Duty-Cycled Wake-Up Receiver Based on Low Noise Amplifier

As described at the beginning of this paper, the WuRx is characterized by the continuous listening of the receiving channel, the identification of WuPt and the activation of the awaking signal of the main unit, which is the MSP430 micro-controller in this of this work. The duty cycling process is well structured, with defined periods for each communication phase.

The timing diagram in Figure 19 explains the duty-cycled communication. The receiving phase is characterized by a peak in time which is reduced so as to be as short as possible to reduce the overall power consumption. The t_{peak} is the necessary duration for detecting a wake-up packet, and t_{sleep} is the duration between two active phases. The transmitting phase includes the t_{WuPt} , which is the duration of the signal wake-up packet for transmitting the wake-up address. The address decoding of the wake-up, t_{addr} , needs to be at least twice the WuPt to ensure a complete reception of the address.

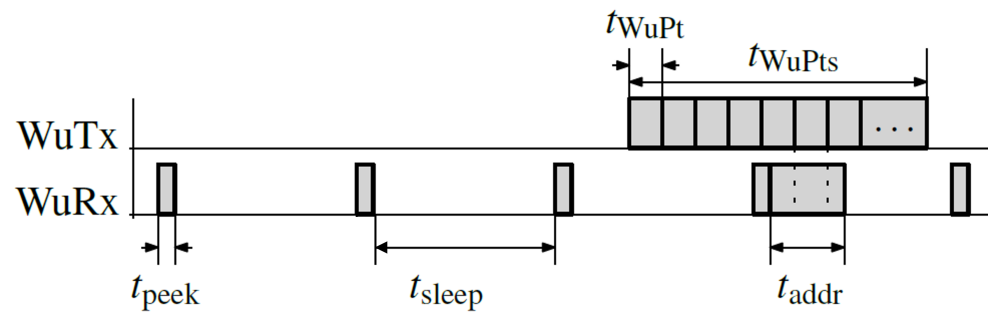


Figure 19. The timing diagram for duty-cycled wake-up communication based on [16].

A timer configuration in MSP430 programming generates an interruption every t_{sleep} to activate the wake-up. After the necessary time execution, if the wake-up signal detected is valid, the interruption is generated by the microcontroller, and the wake-up component is turned off again. When talking about scheduling the time of the reception process, it is mandatory during the design phase to ensure the fast settling time of the LNA. The duty cycled approach of the WuRx will be based on minimizing the active time of the receiver. The long settling time can be a factor that degrades the whole system design. The successful duty cycled approach is generally ensured only if the trade-off between energy consumption, latency, and sensitivity is considered.

This section compares the results obtained from the designed LNA with other COTS LNA in terms of gain and power consumption. Then, the MAX2640 is selected and mounted on the same WuRx board to achieve an accurate sensitivity analysis based on the same envelope detector sensitivity and for a precise power consumption calculation of the overall system design.

5.1. Comparison with Commercialized Off-the-Shelf Commercialized Low Noise Amplifiers

The hardware measurements presented in the previous section satisfy the requirements for the designed LNA. For better performance analysis, comparing the LNA metrics with other designs in the SoA is mandatory. A comparison with other technologies operating in other frequency ranges, as mentioned in Table 1, would not reflect the improved qualifications offered by this work. For validation, a comparison was made with the COTS LNA presented in Table 2. Figure 20 presents an observation of the amplifier gain and power consumption of this work toward the other works operating in 868 MHz. The gain level for a single design stage compared to the other COTS LNAs is at the same level. As the designed LNA offers a gain range of 12–15 dB at 868 MHz, which is the same as MAX2640 and MAX2642. Even BGU7003 and BGU8051 achieve the 20 dB gain; in term of power consumption, the designed LNA consumes five times less power compared to the MAX LNAs and twenty times less than the BGU LNA family. This enhanced the proposed design and helped to determine it as having the best design performance in terms of power consumption with the same gain level as the available COTS LNAs.

Finally, a notable investigation of the total circuit's consumed power is obtained. Finally, the trade-off between those two parameters is determined.

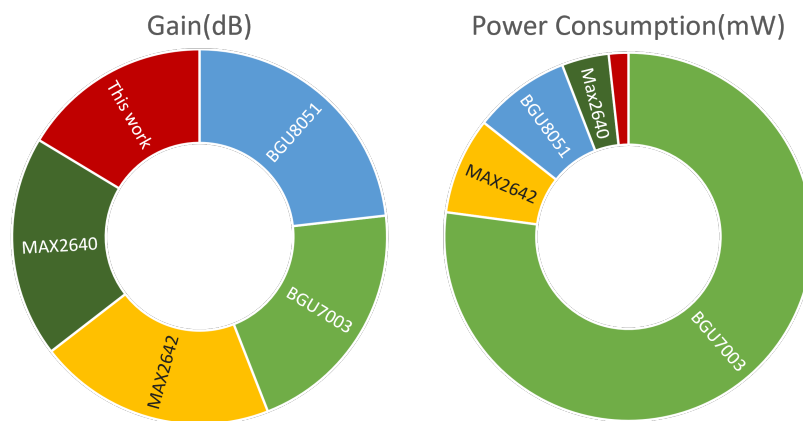


Figure 20. Comparison of gain and power consumption trade-offs in this work with 4 COTS LNA.

5.2. Comparison of the Designed with the Commercial MAX2640 Low Noise Amplifier

For the comparison, because relating the extracted parameters from datasheets could sometimes be misleading, the idea was to compare the designed LNA with one of the COTS LNAs mounted in a duty-cycled WuRx front end. For this observation, MAX2640 LNA is matched to the hardware design of duty-cycled WuRx. The demonstration of the wake-up implementation and the overall approach for successful wake-up packet reception is detailed in [16]. For gathering packet error rate (PER) measurements and power consumption measurements, the overall system should contain a Micro Controller Unit (MCU) for data aggregation, which is the MSP430. Figure 21 shows the measurement system design for implementing the duty cycled WuRx including LNA.

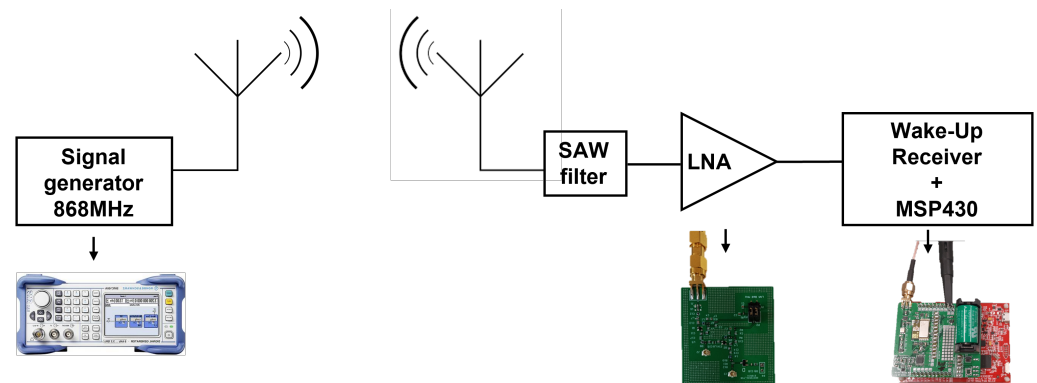


Figure 21. Measurement setup for integration of LNA in duty cycled Wake-up receiver.

Table 4 shows the power consumption during the active state of the WuRx as well as the total current consumed during WuPt transmission, which includes both the active and sleep phase from the wake-up timing approach. The mean power consumed is identified according to the voltage supply of the circuit. As the used envelope detector implemented in the designed WuRx is limited with a -60 dBm sensitivity, the whole circuit based on MAX2640 reached a -80 dBm sensitivity when consuming $14.3 \mu\text{W}$.

Table 4. Performances of designed LNAs integrated in duty-cycled wake-up receiver.

	Sensitivity (dBm)	LNA Current Consumption in Active Phase (mA)	Total Current Consumption during WuPt Transmission (mA)	Mean Power Consumed (μW)
COTS MAX2640 LNA [16]	-80	6.7	7.19	14.3
The designed LNA at 1.8 V	-70	1.6	2.09	3.14
The designed LNA at 3.3 V	-75	3.5	3.99	8.9

To summarize, the whole measurement setup, the overall system, including the designed LNA, reaches -75 dBm and consumes $8.9 \mu\text{W}$ when supplied by 3.3 V. For the same design, when it is powered by 1.8 V, it achieves a lower sensitivity level -70 dBm with a promising result in the total power consumed, which is $3.14 \mu\text{W}$.

6. Summary

Based on the measurements resulting from integrating the designed LNA into the architecture of the duty-cycled WuRx, it is mandatory to compare with other wake-up works either in the same frequency or in other bands based on other architecture. The reason behind this is the lack of similar works in the SoA which enhance the particularity and exclusivity of this work in such a new field of research.

Taking into consideration the two main axes, which are the sensitivity and power consumption at 868 MHz, the developed work, as mentioned in Figure 22 shows lower power consumption with sensitivity levels of up to -75 dBm. Furthermore, depending on the supply voltage and the tuned values used to select the desired performances, lower sensitivity is also accepted with $3.14 \mu\text{W}$ consumption for the whole circuit.

In the same chart, other references are indicated, citing the approach of [33,34], and they exceed the amount of power specified, which is not adequate for WuRx designs. Additionally, refs. [35–37] used technologies that are integrated or off-the-shelf designs, which are limited to possessing low sensitivity levels [38–41], which does not provide a good communication range. The present work provides the optimum trade-off between power consumption and gain among the other WuRx architectures.

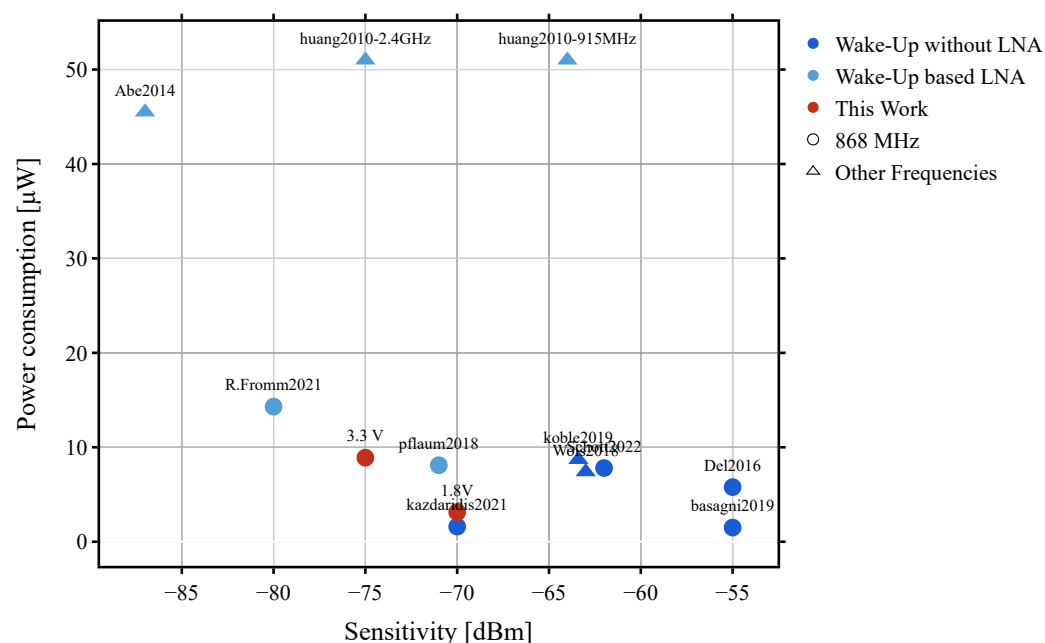


Figure 22. Comparison of the effect of LNA integration with SoA of WURX.

7. Conclusions

In this paper, a recent research field is investigated, i.e., the adoption of WuRx nodes in the wireless communication area. Due to the receivers' importance in energy efficiency, it is important to conduct investigations for its behavior improvements. Improving the sensitivity of sensor nodes is a concern of the work presented in this paper.

Improving the sensitivity in a front-end antenna while keeping the overall circulating current as small as possible is a challenging task. The critical factor to success in this regard is to consider the overall of design performances and find a way to achieve the desired specifications. Specifically, the purpose is to achieve the highest gain level with the lowest power consumption possible. Other design performances such as stability, linearity, the

noise figure, and input and output matching are taken into consideration in the overall design phase.

The BFP740 bipolar junction transistor (BJT) was selected as an active device for amplification in a CE architecture set in an ideal operating range. The circuit is implemented with commercial off-the-shelf components due to the availability, low cost, flexibility, and ease of implementation, from considering basics in determining LNA design performances to running multiple simulations on ADS.

The benefit of simulation is extracting the strange behavior of the signal in the time domain, verifying the stability and matching of the impedance port, and tuning the lumped component to extract the best trade-off between gain and current consumption. Despite this, the simulation phase required modifications and improvements, and the hardware implementation phase presented plenty of challenges. Many soldering problems were faced, especially in the fine-tuning of some values and frequency shift problems due to the sensitive RF component and the high operating frequency band. Moreover, the results obtained from a single design stage are convincing, and the placement of the proposed design among the COTS LANs demonstrates an impressive result in terms of power consumption.

Finally, the integration of the design with duty-cycled LNA and the comparison with MAX2640, and with the whole front-end design, reveal the investigation prospects of the proposed design.

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Abbreviations

The following abbreviations are used in this manuscript:

AC	alternating current
ADS	Advanced Design System
BJT	bipolar junction transistor
COTS	commercial off-the-shelf
CMOS	complementary metal-oxide semiconductor
CE	common emitter
CB	common base
CDMA	code-division multiple access
DC	direct current
EMC	electromagnetic compatibility
FET	field-effect transistor
FAN	the field area network
HF	high frequency
IC	integrated circuit
IoT	internet of things
LF	low frequency
LNA	low noise amplifier
LTE	long term evolution
MCU	Micro Controller Unit
Mnf	matched network factor

NF	noise figure
NFmin	ideal noise figure
OOK	on-off keying
PCB	printed circuit board
PER	packet error rate
RF	radio frequency
SAW	surface acoustic wave
SNR	signal-to-noise ratio
SoA	state of the art
TRF	tuned RF
VNA	Vector Network Analyser
WSN	wireless sensor networks
WuPt	wake-up packet
WuRx	wake-up receiver
WuTx	wake-up transmitter
Wi-Fi	wireless fidelity
WiMAX	worldwide interoperability for microwave access

References

- Houssaini, D.E.; Abdullah, Z.; Khriji, S.; Besbes, K.; Kanoun, O. Design of a Guideline for Range-based Localization Algorithms Evaluation using Multiple Linear Regressions. In Proceedings of the 11th International Conference on Sensor Networks, SENSORNETS 2022, Online, 7–8 February 2022; pp. 256–262. [\[CrossRef\]](#)
- El Houssaini, D.; Guesmi, A.; Khriji, S.; Keutel, T.; Besbes, K.; Kanoun, O. Experimental investigation on weather changes influences on wireless localization system. In Proceedings of the 2019 IEEE International Symposium on Measurements and Networking (M and N), Catania, Italy, 8–10 July 2019; pp. 1–6.
- El Houssaini, D.; Khriji, S.; Besbes, K.; Kanoun, O. Iot based tracking of wireless sensor nodes with rssi offset compensation. In Proceedings of the 2020 17th International Multi-Conference on Systems, Signals and Devices (SSD), Monastir, Tunisia, 20–23 July 2020; pp. 897–902.
- Guidara, A.; Derbel, F. A real-time indoor localization platform based on wireless sensor networks. In Proceedings of the 2015 IEEE 12th International Multi-Conference on Systems, Signals and Devices (SSD15), Mahdia, Tunisia, 16–19 March 2015; pp. 1–8.
- Ball, E. Design and field trial measurement results for a portable and low cost VHF/UHF channel sounder platform for IoT propagation research. *IET Microw. Antennas Propag.* **2019**, *13*, 714–724. [\[CrossRef\]](#)
- Bdiri, S.; Derbel, F. A nanowatt Wake-Up Receiver for industrial production line. In Proceedings of the 2014 IEEE 11th International Multi-Conference on Systems, Signals and Devices (SSD14), Barcelona, Spain, 11–14 February 2014; pp. 1–6.
- El Houssaini, D.; Khriji, S.; Mukhtar, M.W.; Derbel, F.; Besbes, K.; Kanoun, O. A Secure and Efficient Login and Data Exchange Scheme for an IoT Laboratory Management System. In Proceedings of the 2020 IEEE 6th World Forum on Internet of Things (WF-IoT), New Orleans, LA, USA, 2–16 June 2020; pp. 1–6.
- Huang, L.; Ashouei, M.; Yazicioglu, F.; Penders, J.; Vullers, R.; Dolmans, G.; Merken, P.; Huisken, J.; de Groot, H.; Van Hoof, C.; et al. Ultra-low power sensor design for wireless body area networks: Challenges, potential solutions, and applications. *Int. J. Digit. Content Technol. Its Appl.* **2009**, *3*, 136–148. [\[CrossRef\]](#)
- Trabelsi, H.; Bouzid, G.; Derbel, F.; Masmoudi, M. A 863–870-Mhz spread-spectrum direct conversion receiver design for wireless sensor. *Int. J. Electron.* **2008**, *95*, 291–303. [\[CrossRef\]](#)
- Moazzeni, S.; Sawan, M.; Cowan, G.E. An ultra-low-power energy-efficient dual-mode wake-up receiver. *IEEE Trans. Circuits Syst. I Regul. Pap.* **2014**, *62*, 517–526. [\[CrossRef\]](#)
- Ibhaze, A.E.; Imoize, A.L.; Okoyeigbo, O. A Brief Overview of Energy Efficiency Resources in Emerging Wireless Communication Systems. *Telecom* **2022**, *3*, 281–300. [\[CrossRef\]](#)
- Kastrinogiannis, T.; Tsiropoulou, E.E.; Papavassiliou, S. Utility-based uplink power control in CDMA wireless networks with real-time services. In *Ad-Hoc Networks and Wireless*; Springer: Berlin/Heidelberg, Germany, 2008; pp. 307–320.
- Yang, K. *Wireless Sensor Networks*; Springer: Berlin/Heidelberg, Germany, 2014.
- Kanoun, O.; Bradai, S.; Khriji, S.; Bouattour, G.; El Houssaini, D.; Ben Ammar, M.; Naifar, S.; Bouhamed, A.; Derbel, F.; Viehweger, C. Energy-aware system design for autonomous wireless sensor nodes: A comprehensive review. *Sensors* **2021**, *21*, 548. [\[CrossRef\]](#)
- Fromm, R.; Schott, L.; Derbel, F. An Efficient Low-power Wake-up Receiver Architecture for Power Saving for Transmitter and Receiver Communications. In Proceedings of the 10th International Conference on Sensor Networks—SENSORNETS, INSTICC, Vienna, Austria, 9–10 February 2021; SciTePress: Setúbal, Portugal, 2021; pp. 61–68. [\[CrossRef\]](#)
- Fromm, R.; Kanoun, O.; Derbel, F. Reliable Wake-up Receiver with Increased Sensitivity using Low-Noise Amplifiers. In Proceedings of the 19th IEEE International Multi-Conference on Systems, Signals and Devices 2022, Setif, Algeria, 6–10 May 2022.
- Piyare, R.; Murphy, A.L.; Kiraly, C.; Tosato, P.; Brunelli, D. Ultra Low Power Wake-Up Radios: A Hardware and Networking Survey. *IEEE Commun. Surv. Tutor.* **2017**, *19*, 2117–2157. [\[CrossRef\]](#)

18. Ma, R.; Kreißig, M.; Ellinger, F. A Fast Switchable and Band-Tunable 5–7.5 GHz LNA in 45 nm CMOS SOI Technology for Multi-Standard Wake-up Radios. In Proceedings of the 25th IEEE International Conference on Electronics, Circuits and Systems, Bordeaux, France, 9–12 December 2018; pp. 829–832. [\[CrossRef\]](#)
19. Ma, R.; El Agroudy, N.; Joram, N.; Ellinger, F. A 405-MHz 850- μ W low-noise amplifier with 53.5-dB voltage gain and 100-ns settling time. In Proceedings of the 2020 IEEE Asia-Pacific Microwave Conference (APMC), Hong Kong, China, 8–11 December 2020; pp. 669–671.
20. Akamatsu, S.; Muir, S.; Dunleavy, L. Simulation Procedures for Successful Low Noise Amplifier (LNA) Design Using Discrete Components. In *High Frequency Electronics*; Modelithics, Inc.: Tampa, FL, USA, 2012; pp. 22–30.
21. Zhang, Y.; Huang, F.; Tang, X.; Zhao, D. A 0.7–9GHz CMOS broadband high-gain low noise amplifier for multi-band use. In Proceedings of the 2012 International Conference on Microwave and Millimeter Wave Technology (ICMMT), Shenzhen, China, 5–8 May 2012; Volume 1, pp. 1–4.
22. Tzschoppe, C.; Kostack, R.; Wagner, J.; Paulo, R.; Ellinger, F. A 2.4 GHz fast switchable LNA with transformer matching for wireless wake-up receivers. In Proceedings of the 2014 9th European Microwave Integrated Circuit Conference, Rome, Italy, 6–7 October 2014; pp. 178–181.
23. Kostack, R.; Tzschoppe, C.; Stockinger, H.; Jörges, U.; Ellinger, F. A 2 GHz low noise amplifier with transformer input matching in 28 nm CMOS. In Proceedings of the 2016 IEEE Nordic Circuits and Systems Conference (NORCAS), Copenhagen, Denmark, 1–2 November 2016; pp. 1–6.
24. NXP Semiconductors. BGU7003, Wideband Silicon Germanium Low-Noise Amplifier MMIC; Rev. 1–30 August 2011. Datasheet. Available online: <https://www.nxp.com/docs/en/data-sheet/BGU7003.pdf> (accessed on 12 September 2022).
25. NXP Semiconductors. Low Noise High Linearity Amplifier, Rev. 7–8 June 2017. Datasheet. Available online: <https://www.nxp.com/docs/en/data-sheet/BGU8051.pdf> (accessed on 12 September 2022).
26. Maxim Integrated. 900MHz SiGe, High-Variable IP3, Low-Noise Amplifier, MAX2642-V01, 2018. Datasheet. Available online: <https://www.maximintegrated.com/en/products/comms/wireless-rf/MAX2642.html> (accessed on 12 September 2022).
27. Maxim Integrated. 300MHz to 2500MHz SiGe Ultra-Low-Noise Amplifiers, 19-1384; Rev 1; 2/99 2015. Datasheet. Available online: <https://www.maximintegrated.com/en/products/comms/wireless-rf/MAX2640.html> (accessed on 12 September 2022).
28. Weber, M.; Fersi, G.; Fromm, R.; Derbel, F. Wake-Up Receiver-Based Routing for Clustered Multihop Wireless Sensor Networks. *Sensors* **2022**, *22*, 3254. [\[CrossRef\]](#) [\[PubMed\]](#)
29. Das, T. *Practical Considerations for Low Noise Amplifier Design*; Freescale Semiconductor, Inc.: Austin, TX, USA, 2013; Volume 10.
30. Maalik, S. Structured LNA Design for Next Generation Mobile Communication. Master's Thesis, Chalmers University of Technology, Göteborg, Sweden, 2014.
31. Gilmore, R.; Besser, L. *Practical RF Circuit Design for Modern Wireless Systems: Active Circuits and Systems, Volume 2*; Artech House: Boston, MA, USA; London, UK, 2003; Volume 1.
32. Pan, K.; Ha, J.H.; Pham, V.L.; Wang, H.; Xu, J.; Park, S. The effect of solder paste volume on solder joint shape and self-alignment of passive components. In Proceedings of the 2020 IEEE 70th Electronic Components and Technology Conference (ECTC), Orlando, FL, USA, 3–30 June 2020; pp. 1289–1297. [\[CrossRef\]](#)
33. Huang, X.; Rampu, S.; Wang, X.; Dolmans, G.; de Groot, H. A 2.4 GHz/915MHz 51 μ W wake-up receiver with offset and noise suppression. In Proceedings of the 2010 IEEE International Solid-State Circuits Conference-(ISSCC), San Francisco, CA, USA, 7–11 February 2010; pp. 222–223.
34. Abe, T.; Morie, T.; Satou, K.; Nomasaki, D.; Nakamura, S.; Horiuchi, Y.; Imamura, K. An ultra-low-power 2-step wake-up receiver for IEEE 802.15. 4g wireless sensor networks. In Proceedings of the 2014 Symposium on VLSI Circuits Digest of Technical Papers, Honolulu, HI, USA, 10–13 June 2014; pp. 1–2.
35. Köble, S.; Heller, S.; Woias, P. A narrow-band and ultra-low-power 433 MHz wake-up receiver. *J. Phys. Conf. Ser.* **2019**, *1407*, 012093. [\[CrossRef\]](#)
36. Pflaum, F.; Weigel, R.; Koelpin, A. Ultra-low-power sensor node with wake-up-functionality for smart-sensor-applications. In Proceedings of the 2018 IEEE Topical Conference on Wireless Sensors and Sensor Networks (WiSNet), Anaheim, CA, USA, 14–17 January 2018; pp. 107–110.
37. Kazdaridis, G.; Sidiropoulos, N.; Zografopoulos, I.; Korakis, T. A Novel Architecture for Semi-Active Wake-Up Radios Attaining Sensitivity Beyond-70 dBm: Demo Abstract. In Proceedings of the 20th International Conference on Information Processing in Sensor Networks (Co-Located with CPS-IoT Week 2021), Nashville, TN, USA, 18–21 May 2021; pp. 398–399.
38. Del Prete, M.; Masotti, D.; Costanzo, A.; Magno, M.; Benini, L. A dual-band wake-up radio for ultra-low power wireless sensor networks. In Proceedings of the 2016 IEEE Topical Conference on Wireless Sensors and Sensor Networks (WiSNet), Austin, TX, USA, 24–27 January 2016; pp. 81–84.
39. Basagni, S.; Ceccarelli, F.; Petrioli, C.; Raman, N.; Sheshashayee, A.V. Wake-up radio ranges: A performance study. In Proceedings of the 2019 IEEE Wireless Communications and Networking Conference (WCNC), Marrakesh, Morocco, 15–18 April 2019; pp. 1–6.
40. Woias, P.; Heller, S.; Pelz, U. A highly sensitive and ultra-low-power wake-up receiver for energy-autonomous embedded systems. *J. Phys. Conf. Ser.* **2018**, *1052*, 012024. [\[CrossRef\]](#)
41. Schott, L.; Fromm, R.; Bouattour, G.; Kanoun, O.; Derbel, F. Analytical and Experimental Performance Analysis of Enhanced Wake-Up Receivers Based on Low-Power Base-Band Amplifiers. *Sensors* **2022**, *22*, 2169. [\[CrossRef\]](#) [\[PubMed\]](#)