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A Capacitorless Flipped Voltage Follower LDO with Fast Transient Using Dynamic Bias

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Abstract: The output capacitorless low-dropout regulator (OCL-LDO) has developed rapidly in recent years. This paper presents a flipped voltage follower (FVF) OCL-LDO with fast transient response. By adding a dynamic bias circuit to the FVF circuit, the proposed LDO has the ability to quickly adjust the gate voltage of the power transistor, without extra power consumption. The proposed LDO was designed in 0.18 μm CMOS process. The simulation results show that the recovery time is 52 ns when the load changes from 0.1 mA to 20 mA with a slew rate of 20 mA/ps, while the quiescent current is 92 μA with 1 V regulated output. The undershoot and overshoot voltage are 242 mV and 250 mV, respectively.

Keywords: low-dropout regulator; flipped voltage; follower capacitorless; dynamic bias

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1. Introduction

Power management integrated circuits (PMICs) are playing an increasingly important role in system-on-a-chip (SOC). The function of electronic products is related to PMICs. High-performance PMICs with high stability, fast dynamic response and high efficiency have become more important. With the advantages of simple structure, low quiescent current, wide bandwidth and noise suppression ability [1–5], LDOs are widely used in wearable intelligence devices, memory, etc. [6–10].

Due to the existence of a large off-chip capacitor in traditional LDOs [11–18], the stability of the traditional LDO is not guaranteed. The dominant pole of the traditional LDO is at the output node, so the dominant pole of the traditional LDO will change under different load conditions. With an increase in load, the dominant pole moves to a low frequency, which causes instability of the LDO system. The traditional LDO regulator with a large output capacitor has the disadvantages of high design complexity, large chip area and high cost [1,19], and this will limit the fully integrated ability of modern SOCs. However, in fully integrated LDOs, the transient and stability will degrade significantly due to the absence of the off-chip capacitor, thus becoming major design challenges.

Many methods have emerged to tackle these issues. For example, in [12,18], a slew-rate enhancement circuit and dynamic transient control circuit were used to improve the transient response, but the impedance of the output still changed with the load, so a large Miller capacitor was used to ensure stability at low load. The FVF structure [20–23] gives another way of compensation, and it can make the output pole independent of the loading. Figure 1a shows the FVF circuit. M_P is the power transistor, and V_{SET} is the input voltage. Because of the small impedance of the FVF structure [24], the output pole is independent of the load and moves to a high frequency. The output impedance can be expressed as

$$R_{OUT} = \frac{1}{g_{m1}} || R_{load} \quad (1)$$

In Equation (1), g_{m1} is the transconductance of M_1. Equation (1) indicates that R_{OUT} is related to g_{m1} and much smaller than the load resistance; therefore, the output pole does not vary with the load, and the stability problem is solved.

In Figure 1a, the FVF structure decreases the output resistance [25,26] and moves the non-dominant pole, which is constituted by output resistance and output capacitance, into a high frequency, but the stability issues still need to be considered if the two poles are close enough. However, the low loop gain of the FVF structure affects the response time, line regulation and load regulation in the stable output state [8,27,28]. The FVF structure can be replaced by a folded FVF structure [25,29–32], as illustrated in Figure 1b. With the addition of cascade transistor M_2 in the feedback loop, the loop gain of the folded FVF is improved.

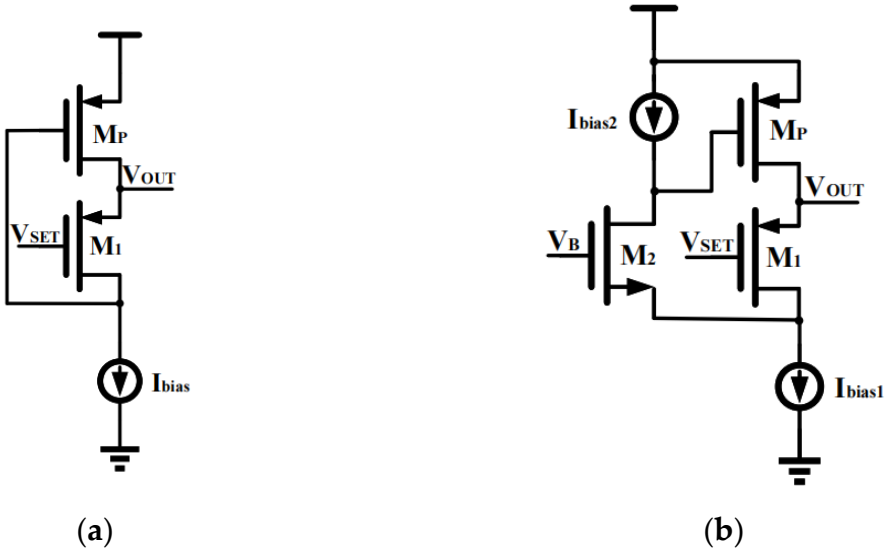


Figure 1. (**a**) Structure of an FVF; (**b**) Structure of a folded FVF.

However, fast transient response is an important requirement in the OCL-LDO because there is no external output capacitor to decrease the output variations when the transient occurs. In Figure 1b, I_{bias1} and I_{bias2} determine the transient response, and a large bias current will consume more power. The authors of [29] presented a voltage spike detection circuit based on capacitive coupling. This circuit realized bias current change in load changes, but the capacitor consumed a greater area. The authors of [33] proposed a novel positive transient detection circuit to improve the transient response, but the better effect was achieved only with heavy to light load changes. This paper proposes a dynamic bias generation circuit for fast charging/discharging of the large gate-source parasitic capacitance of the power transistor M_P by using an MOS to detect changes in the output. Fast transient response is achieved by dynamically adjusting the bias currents I_{bias1} and I_{bias2} when the load changes.

This article is organized as follows. Section 2 elaborates on the structure and principle of the proposed dynamic bias circuit. In Section 3, the implementation of the LDO circuit is described. Simulation results are presented in Section 4. Finally, Section 5 concludes the paper.

2. Proposed Dynamic Bias Circuit

The concept of the proposed dynamic bias circuit is illustrated in Figure 2. The circuit consists of five MOS transistors, $M_{D1\text{-}5}$, and two constant bias currents, I_{bias} and I_2. V_{REF} is a constant voltage. The function of M_{D2} is to detect the change in voltage V_{OUT} directly. I_1 is influenced by the change in V_{OUT} and then affects I_3 because $I_3 = I_2 + I_1$. In the steady

state, V_{OUT} remains constant, and V_{GS1} is constant to give a fixed current I_1. The current I_1 can be expressed as

$$I_1 = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_{MD2}(V_{GS2} - V_{TH})^2 \tag{2}$$

In Equation (2), V_{GS2} is the gate-source voltage of M_{D2} in the steady state. The gate and source voltages of M_{D2} remain unchanged; consequently, I_3 is a stationary current in steady state.

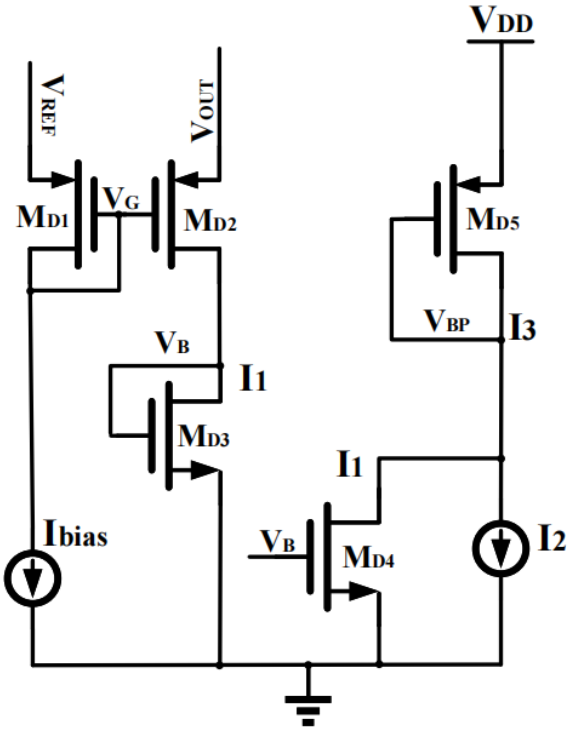


Figure 2. Structure of the proposed dynamic bias circuits.

In the steady state, V_{OUT} equals V_{REF}. However, when V_{OUT} increases instantaneously, the variation is ΔV. The source of M_{D2} detects the change, then $|V_{GS2}|$ increases momentarily to increase I_1. I_1 can be found from

$$\begin{aligned} I_1 + \Delta I_1 &= \tfrac{1}{2}\mu_n C_{ox}\left(\tfrac{W}{L}\right)_{MD2}(V_{G,MD2} - V_{OUT} - V_{TH})^2 \\ &= \tfrac{1}{2}\mu_n C_{ox}\left(\tfrac{W}{L}\right)_{MD2}(|V_{GS2}| + \Delta V - V_{TH})^2 \end{aligned} \tag{3}$$

The extract current ΔI_1 is given by

$$\begin{aligned} \Delta I_1 &= \tfrac{1}{2}\mu_n C_{ox}\left(\tfrac{W}{L}\right)_{MD2}[(|V_{GS2}| + \Delta V - V_{TH})^2 - (|V_{GS2}| - V_{TH})^2] \\ &= \mu_n C_{ox}\left(\tfrac{W}{L}\right)_{MD2}(|V_{GS2}| + \tfrac{\Delta V}{2} - V_{TH})\Delta V \end{aligned} \tag{4}$$

Equation (4) shows that large W/L and ΔV are conducive to increasing I_1; thus, M_{D2} injects more transient current into I3. When V_{OUT} returns to a constant voltage level, V_{GS2} is in a steady state once again, then I_1 returns to the stable value.

Similarly, when V_{OUT} decreases, $|V_{GS2}|$ decreases, then I_1 is reduced, and I_3 is also affected. Figure 3 illustrates the variation in I_1 and I_2 when V_{OUT} changes. I_1 changes with the variation in V_{OUT}, and I_3 changes as well.

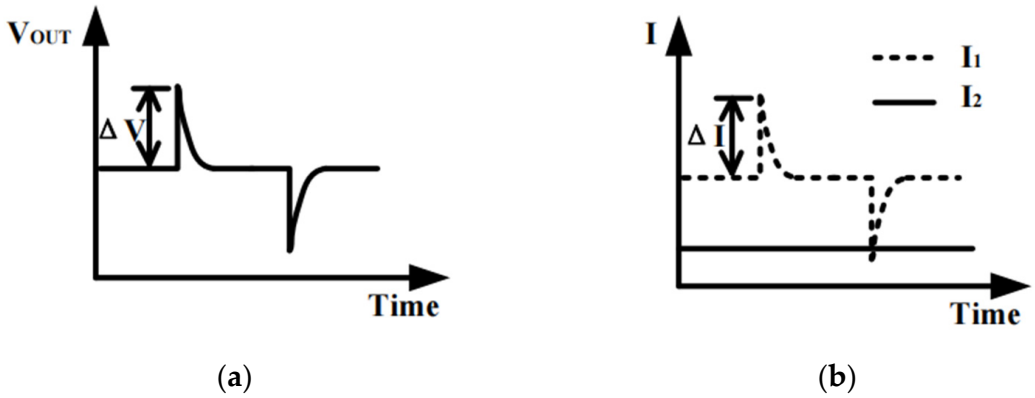


Figure 3. (**a**) Change in V_{OUT}; (**b**) Variation in I_1 and I_2.

3. Circuit Design

The proposed LDO circuit structure implementation presented in this paper is shown in Figure 4.

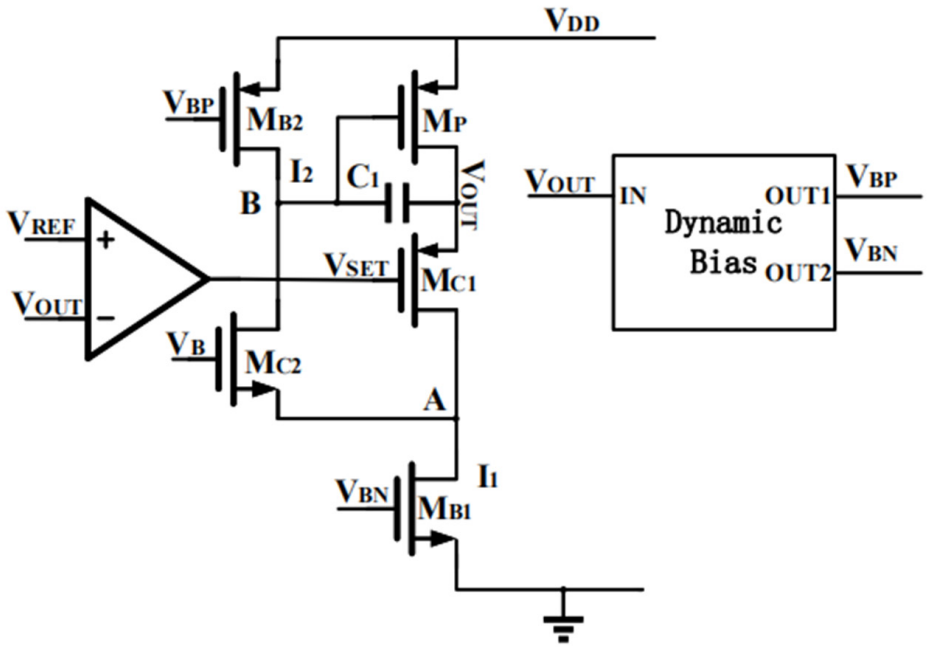


Figure 4. Proposed LDO circuit structure.

The proposed LDO is formed by a folded FVF circuit, the proposed dynamic bias circuit, an amplifier, and a power transistor, M_P. To ensure the performance of the circuit, the folded FVF was adopted to improve the circuit gain. M_{C1}–M_{C2} and two bias currents I_1–I_2 make up the folded FVF circuit. V_{SET} as the input of the folded FVF is generated by the amplifier. V_B is a constant voltage.

Figure 5 shows the dynamic bias circuit. MOS transistors M_{D1}–M_{D14} comprise the dynamic bias circuit. V_{B1} and V_{B2} are constant voltages. The sources of M_{D1} and M_{D4} are connected to V_{OUT} to achieve direct detection of the voltage spike created at the transient instant. M_{D3} and M_{D6} were developed to generate new dynamic bias voltages V_{BN} and V_{BP}; they are dynamic bias currents I_1 and I_2 in the folded FVF circuit.

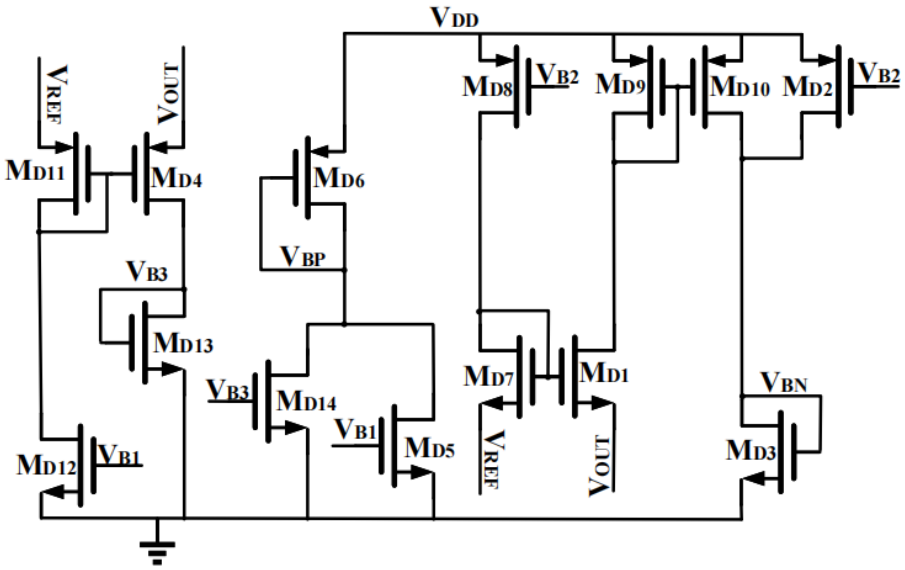


Figure 5. Dynamic bias circuit.

In the dynamic bias circuit, the drop (or increase) in V_{OUT} is detected by the source of MD1 and subsequently decreases (or increases) the gate voltage of M_P through the signal path formed by M_{D3} and I_1. Similarly, M_{D4} also senses the drop (or increase) in V_{OUT} to increase (or decrease) the gate voltage of M_{D6} and finally decrease (or increase) the gate voltage of M_P via the signal path formed by I_2 and M_{C2}.

The constant current sources generated by M_{D2} and M_{D5} are added to the circuit. This avoids excessively high or low V_{OUT} resulting in extremely low currents generated by M_{D1} and M_{D4}.

When I_{LOAD} suddenly increases, V_{OUT} drops rapidly. The signal response is shown in Figure 6. In Figure 6, the capacitor C is the parasitic capacitor of the gate and source of MP. The direction of the arrow in the capacitor represents discharge or charge current.

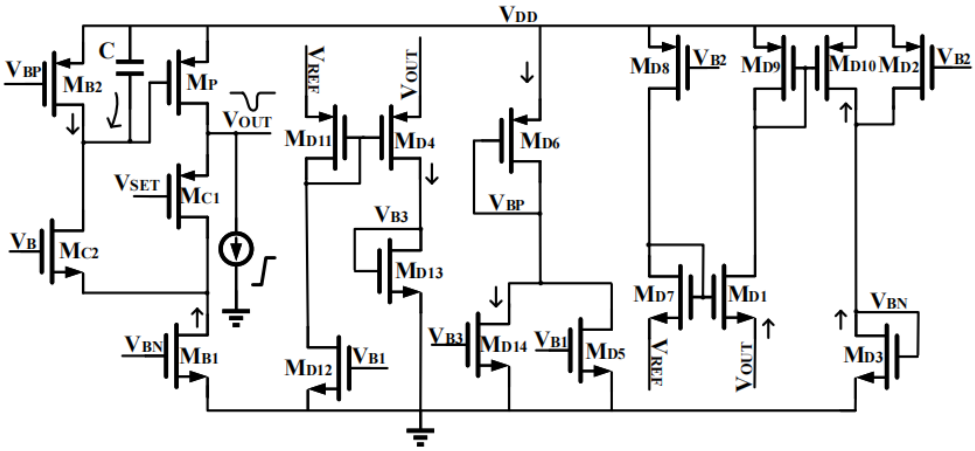


Figure 6. Signal response when I_{OUT} increases.

The change is sensed by the source of M_{D1} and M_{D4}. Due to the drop in V_{OUT}, $|V_{GS}|$ of M_{D1} increases; thus, the current of M_{D3} rises. At the same time, the alteration of the voltage leads to a sharp and momentary decrease in $|V_{GS}|$ of M_{D4}, which reduces the current of M_{D4}. Because of the drop in V_{OUT}, $|V_{GS}|$ of M_{C1} decreases, and then the current of M_{C1} is diminished. The current flowing through M_{C2} is

$$I_{MC2} = I_{MB1} - I_{MC1} = I_{MD1} + \Delta I_{MD1} + I_{MD2} - (I_{MC1} - \Delta I_{MC1}) \quad (5)$$

In Equation (5), I_{MC1} and I_{MD1} are the steady-state currents of M_{C1} and M_{D1}. ΔI_{MC1} and ΔI_{MD1} are the variations. We know from Equation (5) that I_{MC2} increases. The capacitor C then discharges. The discharge current of C is

$$I_{discharge} = I_{MC2} - I_{MB2} = I_{MC2} - (I_{MD4} - \Delta I_{MD4} + I_{MD5}) \quad (6)$$

I_{MD4} is the current of M_{D4} in the steady state, and ΔI_{MD4} is the variation. Accelerated discharge of C, decreased gate voltage of M_P, and increased output current are achieved due to M_{C1}, M_{B1-} and M_{B2}. When V_{OUT} is regulated back to the nominal value, the bias condition of the circuit returns to normal.

Similarly, when I_{LOAD} decreases suddenly, V_{OUT} increases. The signal response is shown in Figure 7.

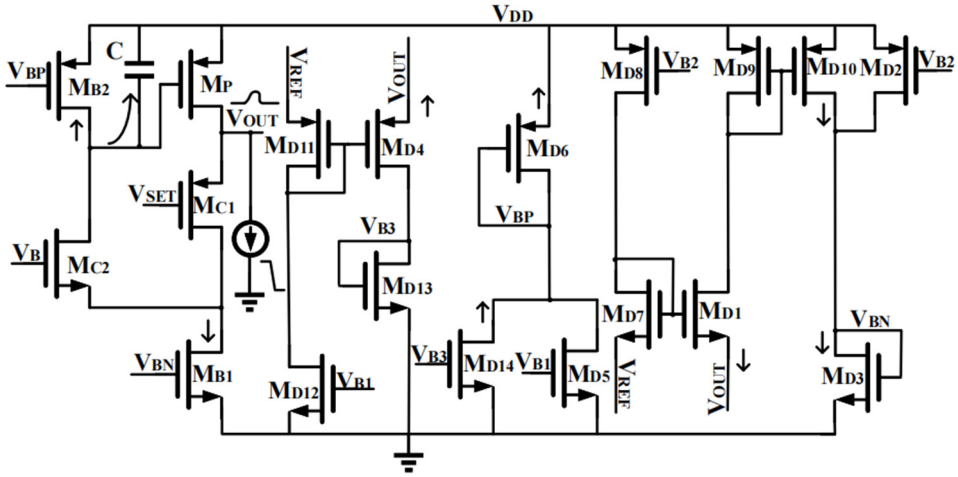


Figure 7. Signal response when I_{OUT} decreases.

The change in V_{OUT} is detected by M_{D1} and M_{D4} again to reduce the $|V_{GS}|$ of M_{D1} and increase the $|V_{GS}|$ of M_{D4} simultaneously. Due to the sharp increase in V_{OUT}, $|V_{GS}|$ of M_{C1} goes up, and the current of M_{C1} rises. The current flowing through M_{C2} is

$$I_{MC2} = I_{MB1} - I_{MC1} = I_{MD1} - \Delta I_{MD1} + I_{MD2} - (I_{MC1} + \Delta I_{MC1}) \quad (7)$$

We know from Equation (7) that $I_{M_{C2}}$ decreases. The capacitor C is then charged. The charging current of C is

$$I_{charge} = I_{MB2} - I_{MC2} = (I_{MD4} + \Delta I_{MD4} + I_{MD5}) - I_{MC2} \quad (8)$$

C is charged up to reduce the current provided by M_P to the load. The operation is automatically shut down again when V_{OUT} returns to the steady state.

The small-signal model of the proposed folded FVF LDO is shown in Figure 8.

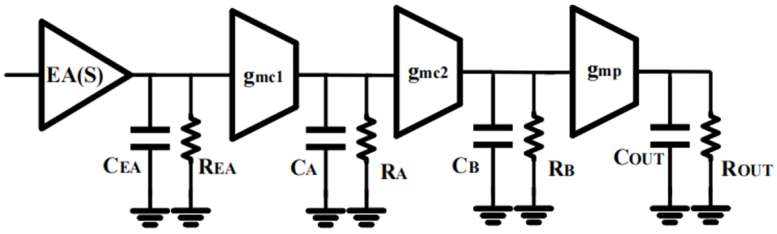


Figure 8. Small-signal model.

R_B and C_B are the equivalent resistance and capacitance at node B. The resistance and capacitance are

$$R_B = r_{oMB2} \,||\, g_{mc2} \cdot r_{oMC2} \cdot r_{oMB1} \tag{9}$$

$$C_B = C_{GSP} + (1 + g_{mp} \cdot R_{out})C_1 \tag{10}$$

In Equations (9) and (10), gM_{C2} and gmp are the transconductances of M_{C2} and M_P; r_{oMB1}, r_{oMB2} and r_{oMC2} are the drain output resistances of M_{B1}, M_{B2} and M_{C2}; and C_{GSP} is the gate source capacitance of M_P.

The resistance and capacitance of the output node are

$$R_{OUT} = \frac{1}{g_{mc1}} || \frac{1}{g_{mD1}} || \frac{1}{g_{mD4}} || r_{op} || R_{load} \tag{11}$$

$$C_{OUT} = C_1 + C_{GSMC1} + C_{GSMD1} + C_{GSMD4} + C_{para} \tag{12}$$

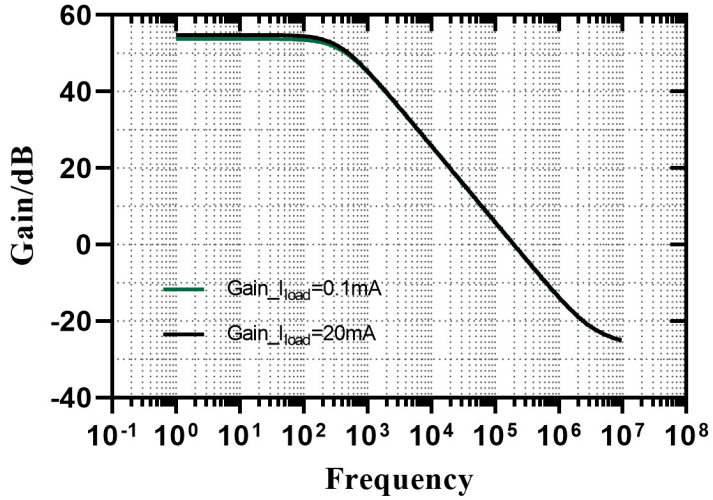
In Equations (11) and (12), gM_{C1}, g_{mD1} and g_{mD4} are the transconductances of M_{C1}, M_{D1} and M_{D4}; r_{op} is the drain output resistor of M_P; $CGSM_{C1}$, C_{GSMD1} and C_{GSMD4} are the gate source capacitance of M_{C1}, M_{D1} and M_{D4}; and C_{para} is the parasitic capacitance in output node. The large R_B and C_B determine the position of the dominant pole.

Generally, R_{load} is larger than $1/g_m$; then, the output resistance is related to $1/g_m$, and this means that the R_{OUT} has little correlation with R_{load}. The dominant pole is at node B, and the non-dominant pole at the output node is almost unchanged when the load changes, so the circuit is stable.

4. Simulation Results

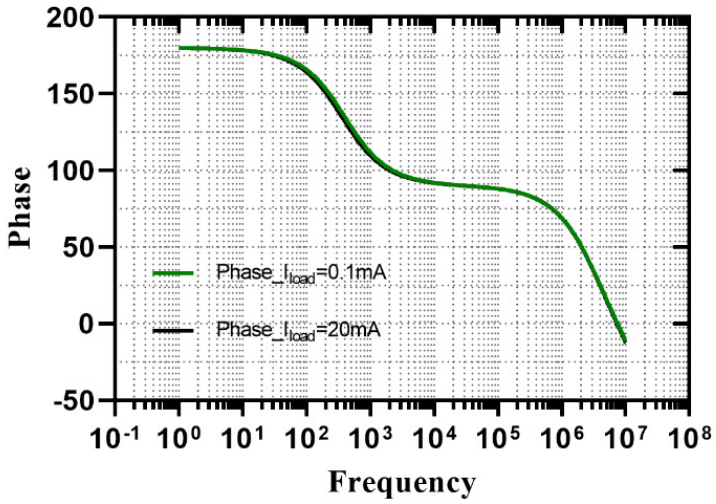
The proposed LDO circuit was designed using 0.18 µm standard CMOS technology. The supply voltage was 1.8 V. The simulation results are presented here.

Figure 9 shows the frequency response of the proposed LDO at different I_{LOAD} values (I_{LOAD} = 0.1 mA and I_{LOAD} = 20 mA). It can be seen that the phase margins are more than 85 in all conditions. This circuit is stable.



(**a**) Gain of the frequency response at different I_{OUT} values.

Figure 9. *Cont.*



(**b**) Phase of the frequency response at different I_{OUT} values

Figure 9. Frequency response at different I_{OUT} values.

Figure 10 displays the quiescent current for different temperatures (−40 °C, 27 °C and 85 °C) and process corners. The quiescent current of the LDO circuit is 92 µA in the TT corner and at 27 °C. During load transition, the change in dynamic bias current causes the quiescent current to change; however, in the steady state, the quiescent current is constant. Therefore, the quiescent of LDO is stable at zero load and full load.

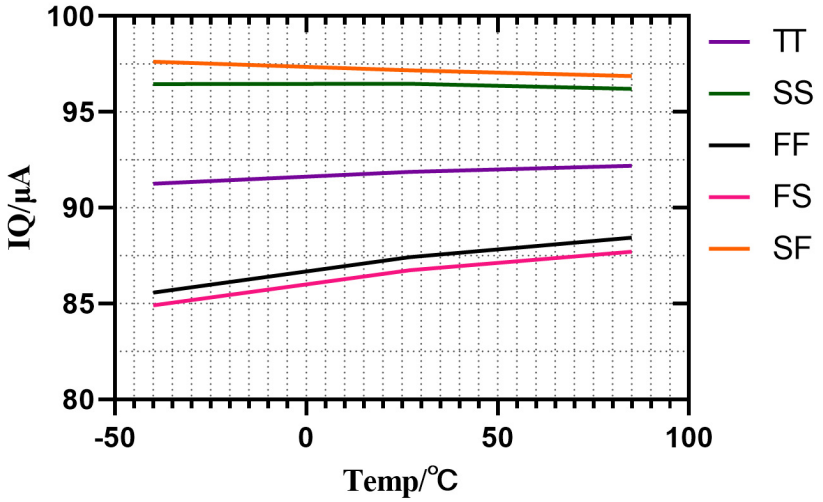
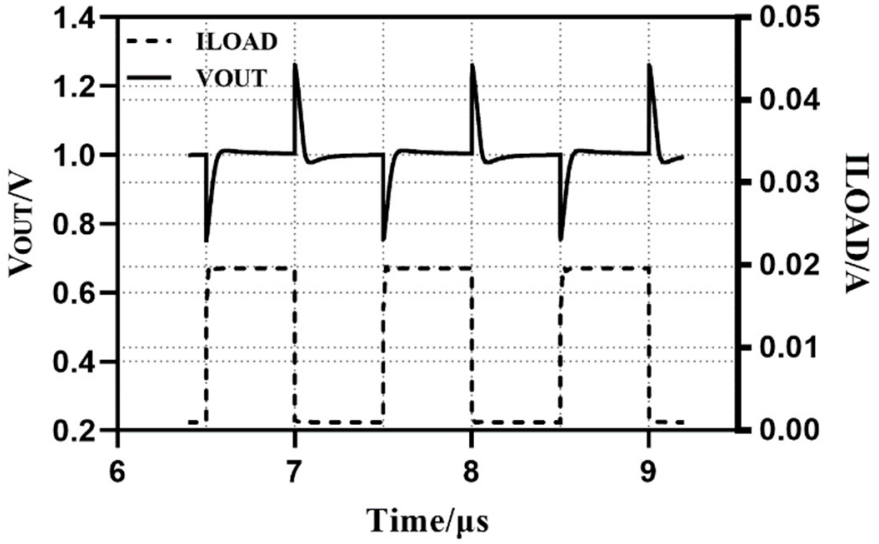
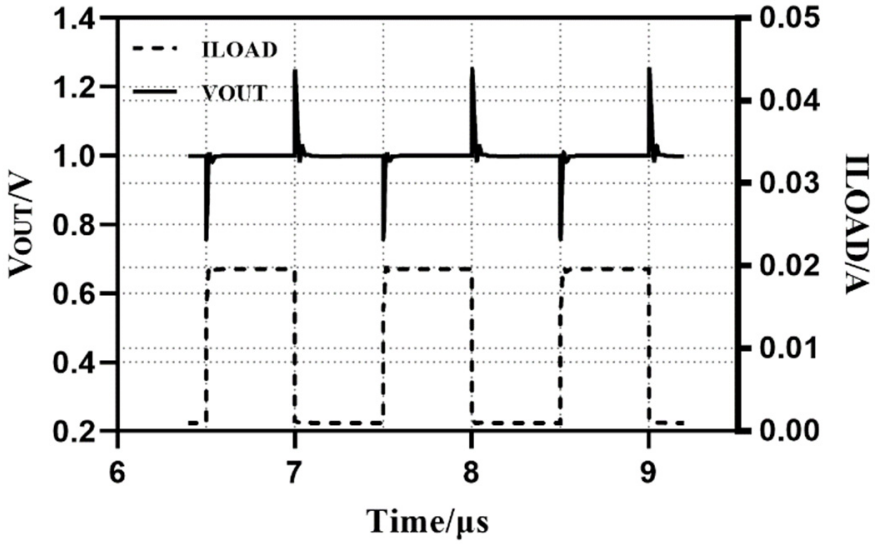


Figure 10. Quiescent current for different temperatures and process corners.

In Figure 11, the transient response simulation results of the LDO without and with the proposed dynamic bias circuit are shown. The load current changes from 0.1 mA to 20 mA with a rise/fall time of 1 ps.



(**a**)



(**b**)

Figure 11. Transient response: (**a**) Without dynamic bias circuit; (**b**) With dynamic bias circuit.

T_{settle} is the recovery time when V_{OUT} settles back to 1% accuracy [33]. As shown in Figure 11, the undershoot, overshoot and recovery time of the LDO without the proposed dynamic bias circuit were about 248 mV, 260 mV and 177 ns, respectively, while those of the LDO with the proposed circuit were about 242 mV, 250 mV and 52 ns only, respectively. The transient benefitted from the dynamic bias current and large bias current.

Figure 12 shows the simulated recovery time versus process corners and temperature variations. As can be seen, across all process corners at −40 °C, 27 °C and 85 °C, the max recovery time was 59 ns at 85 °C in the SS corner, while the min recovery time was 45 ns at −40 °C in the FF corner.

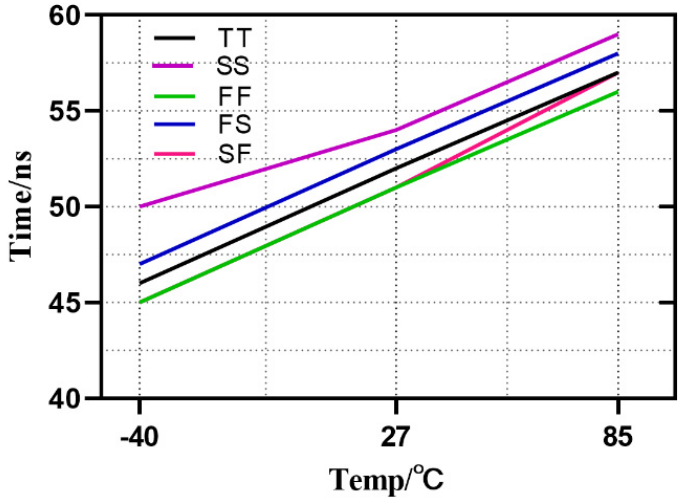


Figure 12. Recovery time versus process corners and temperature variations.

Figures 13 and 14 present the simulated overshoot and undershoot against process corners and temperature variations (−40 °C, 27 °C and 85 °C). The max overshoot was 283 mV at 85 °C in the SS corner, while the min overshoot was 217 mV at −40 °C in the FS corner. The max undershoot was 280 mV at 85 °C in the SS corner, and the min undershoot was 206 mV at −40 °C in the SS corner.

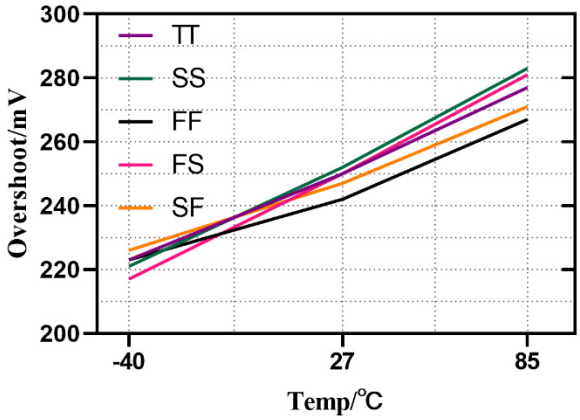


Figure 13. Overshoot against process corners and temperature variations.

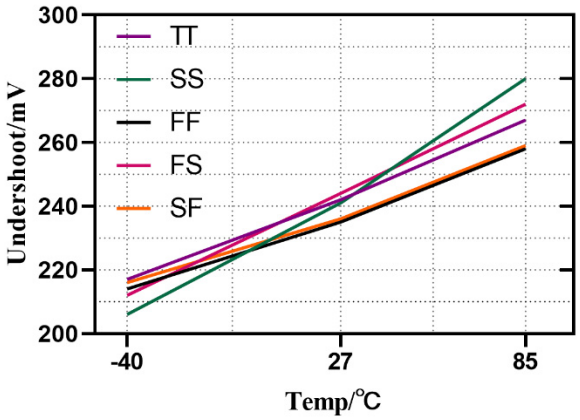


Figure 14. Undershoot against process corners and temperature variations.

For the layout of the design, we used a 0.18 µm standard CMOS process. Figure 15 shows the layout of this design, with an active area of approximately 0.0235 mm^2 (156.8 µm × 149.8 µm).

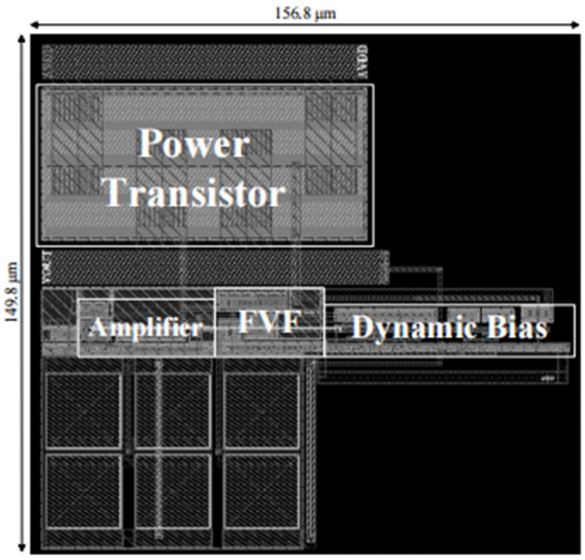


Figure 15. Layout of the proposed LDO.

Table 1 summarizes the performance of the proposed LDO circuit and compares it with the prior state of the art in terms of quiescent current, on-chip capacitor, recovery time spike voltage, load regulation (LDR), line regulation (LNR) and power-supply rejection ratio (PSRR). Compared with the prior designs in Table 1, this paper achieves the shortest response time.

Table 1. Performance summary and comparison with the prior state of the art.

Parameter	[13]	[19]	[25]	[27]	[33]	This Work
Process (nm)	65	65	180	65	130	180
V_{OUT}	1	0.98	1.2	1	1.2	1
IQ (µA)	23.7	385	34.5	13.2	100	92
Imax (mA)	50	20	20	50	20	20
Con-chip (pF)	9	9	5	10	1.4	2.8
TEdg (ns)	100	N/A	0.1	500	10	0.001
K	100,000	N/A	10	500,000	10,000	1
ΔV_{OUT} (mV)	40	N/A	270	341.63	95	250
T_{settle} (ns)	1650	N/A	N/A	925	150	52
PSRR (dB) at 1 kHz	−52	−92.65	N/A	N/A	−60	−60.85
LDR (mV/mA)	0.034	2.3	N/A	0.133	N/A	0.088
LNR (mV/V)	8.89	50	N/A	0.217	N/A	0.948
FOM_1	45,095	N/A	4.65	1896	4773	1.16
FOM_2	782	N/A	N/A	244	750	239

In Table 1, FOM1 is defined as in [26,34]; it can be expressed as

$$FOM_1 = K\left(\frac{\Delta V_{OUT} \cdot I_Q}{\Delta I_{OUT}}\right) \quad (13)$$

In Equation (13), K is the edge-time ratio, which is defined by

$$K = \frac{\Delta t \text{ used in the measurement}}{\text{the smallest } \Delta t \text{ among the designs for comparison}} \quad (14)$$

In Equation (14), Δt is the edge time taken for the change in the output current.

FOM_2 [35] can be expressed as

$$FOM_2 = \frac{T_{settle} \cdot I_Q}{I_{Load,\max}} \quad (15)$$

5. Conclusions

This paper proposed a new dynamic bias technique applied in FVF OCL-LDO circuits. The output current of the power MOS is changed quickly due to the discharge/charge current of the gate of the power MOS increasing during the load current transition; thus, the output voltage returns to the steady state quickly. It achieves a fast transient response by only changing the bias currents during load transition, without increasing the quiescent current.

The proposed LDO was realized by a 0.18 μm CMOS process. The result shows that V_{OUT} recovered to 1% in 52 ns when the load current changed from 0.1 mA to 20 mA, or back, with an edge time of 1 ps. The quiescent current was 92 μA under light and heavy load. The total on-chip capacitance was 2.8 pF, and the undershoot and overshoot were 242 mV and 250 mV, respectively. The proposed LDO is satisfactory for digital circuits and fully integrated body sensor chips.

Author Contributions: Conceptualization, Y.L. and M.C.; methodology, Y.L. and K.W.; software, Y.L. and Y.Y.; writing—original draft preparation, Y.L. and H.W.; writing—review and editing, Y.L. and H.W. All authors have read and agreed to the published version of the manuscript.

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Data Availability Statement: No new data were created or analyzed in this study. Data sharing is not applicable to this paper.

Conflicts of Interest: The authors declare no conflict of interest.

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