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An Interleaved Two Switch Soft-Switching Forward PWM Power Converter with Current Doubler Rectifier

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Abstract: Forward converters have been broadly used in the power supply industry due to their simplicity, worthy efficiency, and low cost. A novel prototype soft-switched zero-voltage and zero-current ZVZC PWM DC-DC power converter with low voltage/current stresses is introduced for telecommunication power feeding in this paper. A new two-switch interleaved forward converter circuit is introduced to minimalize current circulation with no supplementary auxiliary snubber circuits. This converter circuit includes some outstanding benefits such as reduced components, improved efficiency, high power density and economic circuit configurations for high power conditioning applications. The simple operation principle is demonstrated on the basis of steady-state analysis. Furthermore, the effective feasibility of the proposed circuit topology is evaluated and verified practically for a 500 W–100 kHz prototype breadboard. The operation principle and steady-state characteristics are demonstrated from a theoretical point of view. To verify the practical effectiveness of the proposed power converter, a 500 W–100 kHz prototype converter using ultrafast IGBTs is implemented for a distributed telecommunication energy plant. The studied soft-switching converter is evaluated in comparison with the previously-proposed PWM converters in terms of voltage, current stresses, and operating efficiency.

Keywords: DC-DC power converter; modified forward converter; high-frequency link; soft-switching PWM interleaved converter; ultrafast IGBT; telecommunication applications

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1. Introduction

There is an increasing need to achieve higher power densities and efficiencies for power converters. This has increased the use of soft-switched converters due to the benefits of primary switch zero-voltage switching (ZVS) turn-on and zero-current switching (ZCS) turn-off [1]. In particular, half-bridge or full-bridge-based LLC technology [2,3], which is more suitable for medium to high power applications, is broadly used in practical designs. Energy efficiency and power density are very important features of today's consumer electronics and industrial applications. In addition, high efficiency over a wide range of output power and the ability to operate over a wide input voltage range are important future prospects for DC-DC converters. To achieve high efficiency, it is necessary to reduce switching loss, especially in high frequency power converters. In addition, for light loads where switching loss and gate drive loss dominate [4,5], reducing switching loss is effective in achieving high efficiency. On the other hand, for relatively low power applications such as for PV systems with low power or auxiliary power in electric vehicles, a forward converter is usually recommended due to the simplicity of the design [4]. According to this, some studies on forward type resonant converters were carried out [4–8].

Operation at hard switching of the flyback and forward converters imposes high voltage and current spikes on their switches, due to presence of transformer leakage inductance. Furthermore, switching losses result in low conversion efficiency. A passive

clamp circuit can be added to dissipate the energy stored in the leakage inductance [9] and reduce the voltage stress on the switch. However, the power conversion efficiency of the circuit has not improved significantly. In recent years, active clamping techniques have been proposed for both converters to absorb the energy stored in the leakage inductance and suppress transients across the switch. In addition, the forward converter energy reset process has been completed [10–14]. The active-clamping converters have higher efficiency than conventional forward and flyback converters because of the zero-voltage-switching (ZVS) operation of the main switch fulfilled with the help of the auxiliary switch.

Numerous types of soft-switching DC-DC power converters have been proposed. One of the most popular isolated power converters is the forward converter that has been widely implemented in low to medium power supply demands due to its simplicity, high reliability, and high efficiency [12]. The HF transformer in forward and flyback converter is used for isolating the electric power signal and storing the magnetic energy. The HF transformer in the forward converter is implemented to achieve galvanic isolation and energy transformation. Resetting the HF transformer is a special feature for the forward DC-DC converter. Therefore, several forward topologies have been suggested with diverse transformer reset arrangements [13–17].

Among these transformer resetting topologies, the two-switch forward DC-DC converter can realize the lowest voltage stresses on the primary-side active switches [17–25]. Moreover, the magnetizing and leakage energy can be recovered for attaining higher efficiency. Generally, the forward DC-DC converter is a promising choice in applications with high-output current requirements. The primary-side of these converters produces symmetrical AC waveforms across the primary-winding of the HF transformer. Therefore, the core flux is bi-directionally excited, resulting in a better utilization of magnetic core and results in increased power rating. Forward converters offer the advantage of better transformer utilization. Energy is transferred instantly through the transformer and not depending on energy storage [26,27]. The lower peak currents produced in the two windings implies lower copper losses as compared with fly-back converter. With considerably higher magnetizing inductance and no air gap, the transformer can be made more ideal. Hence secondary ripple current is dramatically reduced due to the existence of an output inductor and freewheeling diode that keep the output current completely constant. Accordingly, the output voltage ripples are deceased radically due to higher magnetizing inductance and lower active switches peak current. The two-switch method has the lowest voltage stress, and the double-forward method has the highest efficiency [27–30]. In [31], an interleaved series input parallel output (ISIPO) forward converter was proposed. The ISIPO forward converter share many of the same features, including: 1) The voltage stress of each switch is clamped to the input voltage, which is the lowest voltage stress of all the forward topologies mentioned above. No additional magnetization reset circuit is required. Moreover, high efficiency is realized by realizing the inherent degaussing by using an auxiliary diode and reusing both the leakage and the magnetization energies of the transformer. Ref. [32] introduces an interleaved twin double-ended ahead converter. Double-ended ahead converter is the extensively used topology for diverse applications. An interleaved twin double-ended ahead converter consists of double-ended ahead converters. They are operated at 180° out of phase.

Another category of soft-switching schemes is quasi-resonant converters (QRC) and switched-capacitor resonant converters that depend on frequency control [30]. Thus, magnetic components and the output filter passive devices are not optimal. Once the ZVS QRC converter is designed to achieve ZVS condition at light loads [29], the voltage stress on switches is extremely high at full load operating conditions. Likewise, for ZCS type QRC converters [31–36], the switch has a high capacitive turn-on loss due to the ZCS turn-on. Generally, voltage and current rms values are relatively high in resonant-based converters due to the sinusoidal voltage and current of the main components. In such converters, resonance occurs just before the switching time, providing PWM control for the converter. These converters provide smooth load-independent switching and

operate at constant frequencies [37–39]. Ref. [40] has introduced a zero-voltage junction (ZVT) forward converter that provides soft-switching states and resonant core resets. However, this converter uses a number of auxiliary components such as diodes, inductors, capacitors, and additional forward transformers in auxiliary circuits. In addition, the voltage load on the auxiliary switch in this circuit is the same as the voltage load on the main switch, resulting in higher capacitive turn-on loss. In [41], a zero current zero voltage transition (ZCZVT) forward converter is proposed. Like the converter in [7], this circuit has a complex topology with many components. More importantly, this converter has an additional diode in the mains path, which results in high conduction losses. This converter uses an additional resonant inductor and a series diode with an auxiliary switch, which increases the conduction loss of the converter. In addition, the auxiliary switch has a high capacitive turn-on loss. For the ZVT forward converter, the auxiliary switch is loaded with a low voltage. However, there are numerous components, including an additional resonant inductor and two diodes, increasing the complexity of the converter, and increasing the conduction loss of the auxiliary circuit [42]. This circuit is useful when using IGBTs. In addition, with this converter, in addition to the capacitive turn-on loss of the switch, the main switch is subject to high voltage fluctuations during turn-off. Resonant forward DC-DC converters have been proposed previously to minimize switching losses on semiconductor switches [21–24]. Generally, in high-voltage or high-current applications, the voltage or current stresses in resonant converters are extremely high. High-voltage or high-current power switches have higher cost and high conduction losses. Active-clamping techniques have been proposed with constant frequency switching to absorb the stored energy in the leakage inductor [25–28]. Semiconductor devices are turned on during the transition interval at the zero-voltage switching (ZVS) utilizing the transformer leakage inductance and output capacitance of switches. Usually, the high power density and high power rating are essential in various practical applications such as power supply units in telecommunication power supplies and computer servers. One way to increase output power is to connect two or more converter cells in parallel. Thus, the current stresses and power losses can be distributed into each converter cell. Interleaved pulse-width modulation (PWM) controller can control several converter cells with phase-shifted PWM technique to realise the load current sharing and ripple current cancellation. The parallel forward converters with soft switching techniques have been presented in [29–33] to realise ZVS operation and achieve conversion efficiency improvement. However, the control scheme is more difficult to implement, and many switches are used in the circuits.

This paper describes a new interleaved two switch forward soft-switching transition PWM power converter topology, which can diminish the circulating and idling currents with no extra auxiliary snubber circuits. The DC-DC power converter topology treated here takes advantage of fewer components, better power conversion efficiency, higher power density and cost-effective system configuration for high power conditioning applications. The basic block diagram of the proposed converter is illustrated in Figure 1. The basic building blocks of a the studied telecommunication power supply are as follows: a rectifier/pfc stage, DC-link capacitor, interleaved two-switch forward converter, high-frequency transformer, coupled inductor-current doubler, filter and telecommunication load. The control circuit is composed of controller, voltage and current sensors and gate drive circuit.

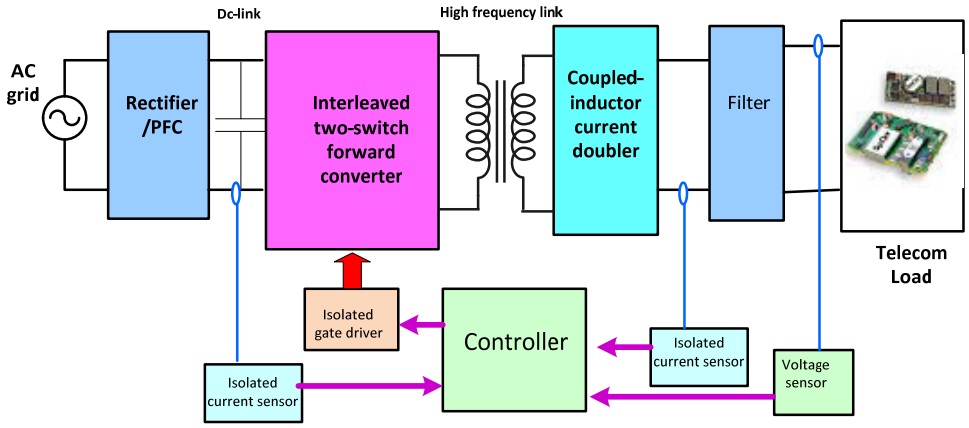


Figure 1. Basic building blocks of the proposed converter.

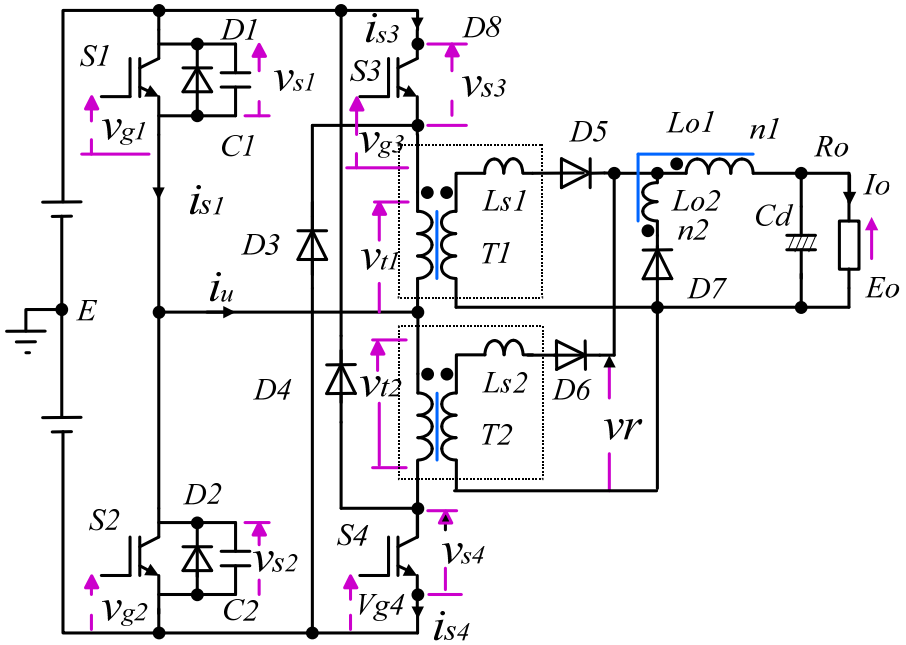
2. Principle of Operation

Figure 2 shows a basic circuit configuration of the proposed DC-DC power converter using the ultrafast IGBTs, which can work as a two-switch interleaving forward power converter with high frequency link. This circuit is a modified version of the two switch interleaved forward converter shown in Figure 2b. One of the forward-type power conversion stages composed of active power switches S_1, S_4, high frequency transformer T_2, fast-recovery diodes D_2, D_4, and diode rectifier D_6. The other bridge leg consists of active power switches S_2, S_3, high frequency transformer T_1, fast recovery diodes D_1, D_3, and rectifier diode D_5. Ls_1 and Ls_2 are low value leakage inductances of T_1 and T_2, correspondingly. A tapped inductor is used in the output stage as a low-pass filter. The gate pulse sequences and ideal waveforms of the power converter are demonstrated in Figure 3. The switching pulse sequences are different from those of the conventional interleaved two switch forward type power converter. Active power switch S_4 (S_3) is turned off after active power S_1 (S_2) is turned off with a short delay time t_δ. Moreover, active power switches S_1 and S_2 are to be driven complementary with a short blanking interval t_d. The output voltage can be regulated by varying a controllable interval t_α as PWM with a constant switching frequency. Figure 3 schematically shows the gate-pulse control signals of the S_1, S_2, S_3 and S_4 main switches of the proposed converter (Figure 2a). The well-known interleaving clocking method is illustrated in Figure 3. To interleave N parallel-connected (or series-connected) converter cells, active switches are switched at the same frequency as the switching operation, but pulses are phase-shifted by $2\pi/N$ radians [21].

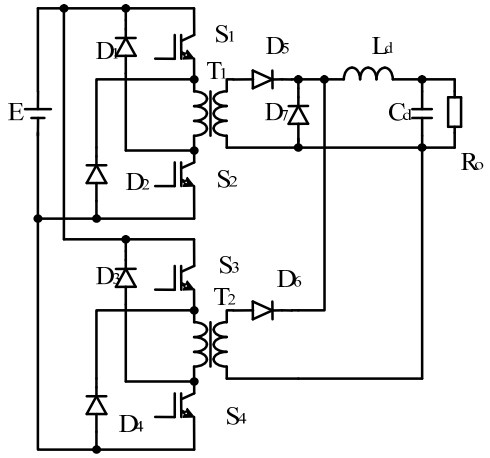
The basic theory of operation under steady-state operating condition is described with the subsequent beliefs.

- All the active power switches and passive power components are ideal.
- High frequency transformers T_1 and T_2 are matching, so that every magnetizing and leakage inductances are characterized as $Lp_1 = Lp_2 = Lp$, $Ls_1 = Ls_2 = Ls$, respectively.
- Capacitors C_1 and C_2 are identical: $C_1 = C_2 = C$.
- Inductor L_{o1} and L_{o2} are coupled compactly and its coupling coefficient $k \approx 1$.

Figure 4 shows the operating current and voltage waveforms at each circuit components. Figure 5 depicts the topological equivalent circuits for one half-cycle interval in continuous conduction mode operation. Before time t_0, active power switches S_1, S_4 and fast recovery rectifier diode D_6 are conducting. Switching states equivalent circuits are done using the state of each switch and diode during one switching period. This method involves defining the set of states that the circuit enters in one period of operation. This method elaborates on the converter operation during one period, and corresponding equivalent circuits are given.



(**a**)



(**b**)

Figure 2. (**a**) Basic circuit configuration of the studied converter. (**b**) Two-switch interleaved hard-switched forward DC-DC converter.

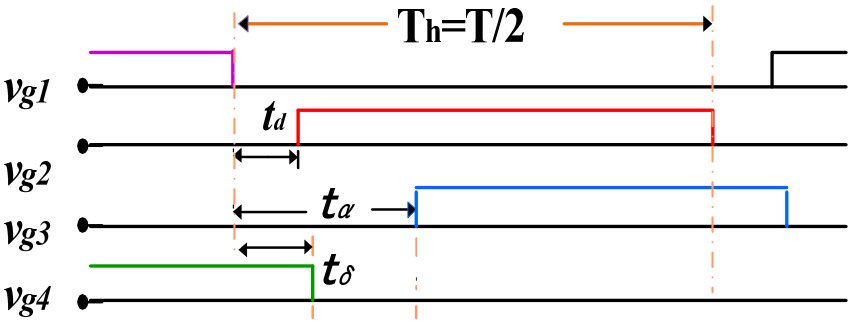


Figure 3. Gate voltage pulse sequences.

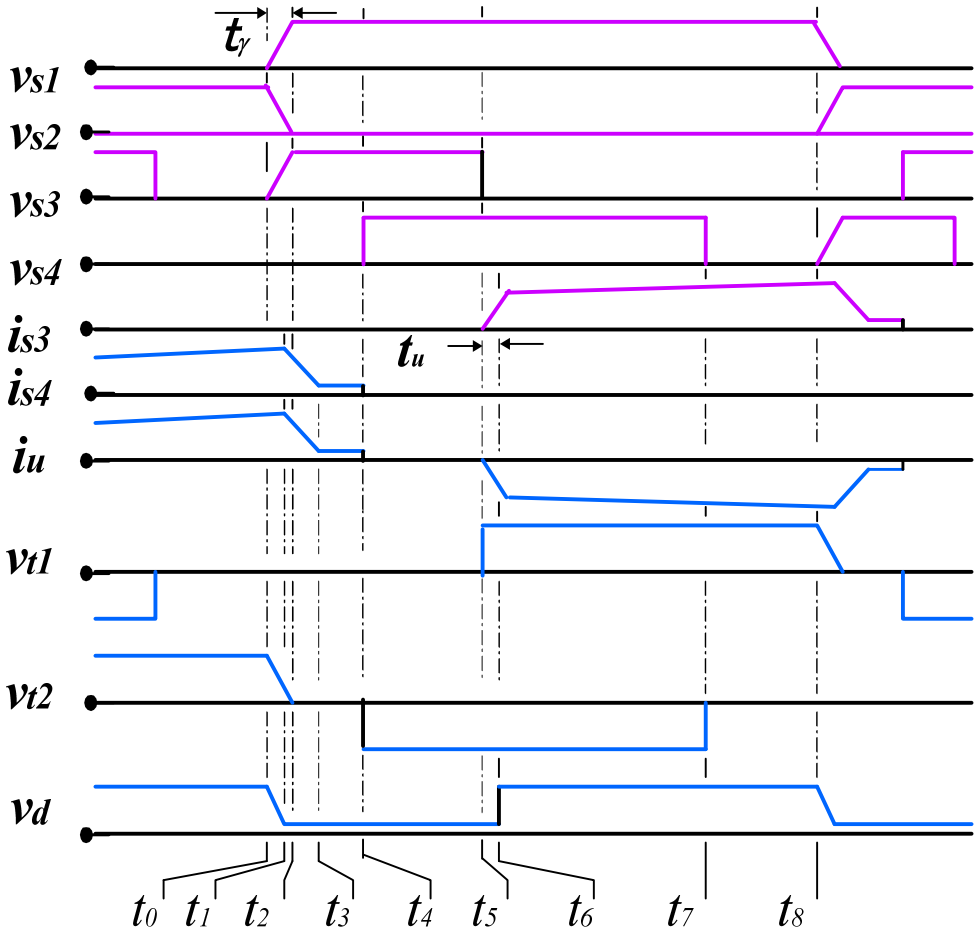


Figure 4. Typical operating waveforms of studied DC-DC power converter.

(a) Mode Interval 1 (t_0–t_1): At time t_0, active power switch S_1 is turned off under zero voltage soft switching (ZVS) transition with the aid of lossless capacitive snubbers C_1 and C_2. Since inductances L_p and L_{d1} are both large, magnetizing current i_{p2} and rectifier current i_{d6} are to be assumed to be constant during this interval. Capacitor voltage v_{c1} increases, and rectified voltage v_r decreases as:

$$v_r = (E - v_{c1})/N_T \tag{1}$$

where N_T is the turns ratio of the high-frequency transformer ($N_T = N_p/N_s$). Because L_{o1} and L_{o2} are coupled to each other compactly, freewheeling diode D_7 starts conduction when v_r reaches $N_L\ E_o$. On the other hand, N_L is the tapped-inductor turns ratio of the and is defined as $N_L = n_2/(n_1 + n_2)$, n_1 and n_2 are the number of turns of L_{o1} and L_{d2}, respectively.

(b) Mode Interval 2 (t_1–t_2): The output current flows through D_7, L_{o2} and L_{o1}. Therefore, the output current reproduced to the primary side of the transformer drops. This interval ends when voltage v_{c2} goes down to zero.

(c) Interval 3 (t_2–t_3): Diode D_2 starts to conduct. The output current reflected to the transformer primary side continues to decrease. The current in capacitors C_1 and C_2 stops. Switch S_4 is still conducting. The energy stored in L_{p2} is transferring to the secondary side of HFT. However, this interval finishes when the current in diode rectifier i_{d6} reaches zero.

(d) Interval 4 (t_3–t_4): The whole output current flows through D_7, L_{o2} and L_{o1}. The output current reflected to the transformer primary-side decreases to zero. This means no energy is transferring to the secondary side of HFT. Only a lesser magnetizing current of the transformer T_2 circulates through transistor switch S_4 and diode D_2. This interval ends when the gate signal is removed from power switch S_4. Therefore, S_4 is turned off.

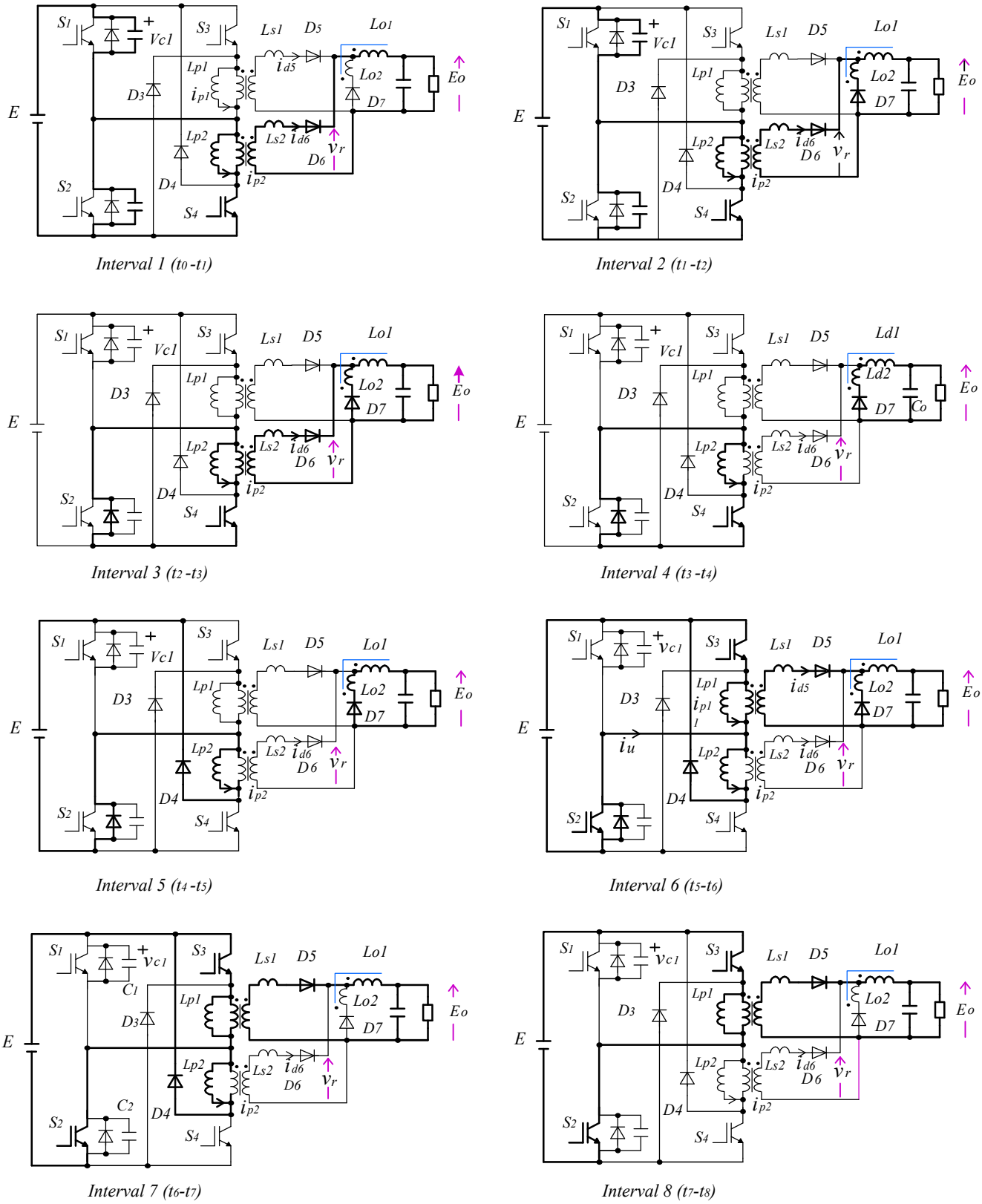


Figure 5. Equivalent circuits of the circuit during half cycle operating intervals.

(e) Interval 5 (t_4–t_5): At time t_4, corresponding to a delay time t_δ, active power switch S_4 is turned off under zero current soft-switching (ZCS). Magnetizing current i_{p2} flows through D_2 and D_4 to the DC voltage supply E as a resetting action of high frequency

transformer T_2. Then i_{p2} start decreasing. On the other hand, the load current still circulates through D_7, L_{o1} and L_{o2}.

(f) Interval 6 (t_5–t_6): At time t_5, depending on duty-ratio of the power converter, S_3 is turning-on under ZCS principle because the leakage inductance L_{s1} make softer di_{s3}/dt during turning-on operation of switch S_3. Active power switch S_2 is also turning-on with hybrid ZCS and ZVS transition when current i_u becomes $i_u < 0$. This is because diode D_2 is conducting. The current in the primary-side of the HFT transformer flows through power switches S_2 and S_3. The current of magnetizing i_{p1} and rectifier current i_{d5} starts circulation through switches S_2 and S_3, and diode D_4. The energy is transferring to the secondary side of HFT through L_{s1} and diode D_5. During this period, the current is increasing in S_3 and D_5. Meanwhile, current i_{L2} through L_{d2} reduces. This operation interval terminates when i_{L2} drops to zero.

(g) Operation interval 7(t_6–t_7): At time t_6, the diode D_7 turns off. Therefore, the total output current streams through D_5 and L_{d1} while the magnetizing current i_{p2} continues decreasing with a constant slope -E/Lp.

(h) Interval 8 (t_7–t_8): This interval starts at t_7, the HFT magnetizing current i_{p2} drops to zero ($t = t_7$), diode D_4 as a passive switch turns off. The electrical energy is delivered to the load through S_3, S_2, T_1 and D_5. The half cycle operating intervals finish at time t_8. The steady-state operation of the next half-cycle is similar to that of the discussed half-cycle. As mentioned above, S_1 and S_2 are turned-on and turned-off at ZVS soft-switching, while switches S_3 and S_4 behave with ZCS soft-switching at both turn-on and turn-off operation. The circulating and idling currents in both sides of high-frequency transformer HFT are considerably low with no supplementary auxiliary snubber circuits.

3. Steady State Operational Characteristics

The output voltage characteristics and current stress on the active power switches are analytically estimated in continuous conduction mode in this section. Figure 6 depicts applicable waveforms of rectified voltage v_r and the current through inductor i_{L1}.

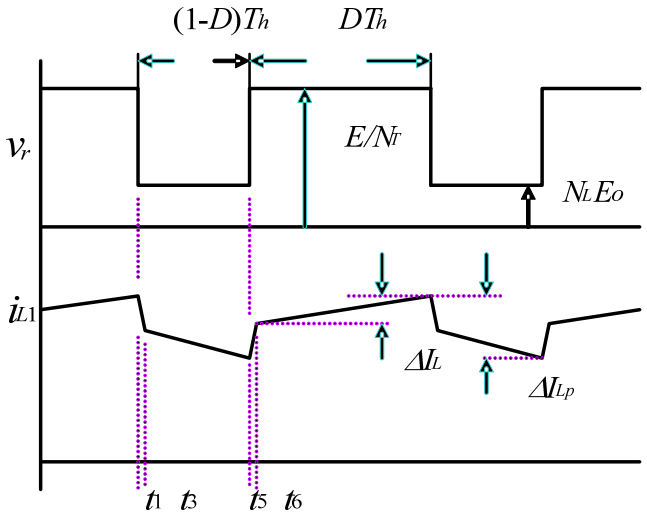


Figure 6. Rectified voltage v_r and inductor current i_{L1} operational waveforms.

The output voltage is controlled by adjusting the duty cycle D when v_r is high the current i_{L1} is increasing, when v_r is low the current i_{L1} is decreasing until a new cycle comes. There are two filter inductors in series with the diode when current is delivered to the load to reduce the ripples in output currents. The output capacitor has to smooth out large pulsating output currents since it is supplied only during the switch OFF period.

This arrangement permits more favorable trapezoidal current waveforms and lower output current and voltage ripple, which consequently gives reduced noise and decreased stress on semiconductors and capacitors. Due to the non-pulsating characteristic of

its output current, the forward converter is well suited for applications involving high output currents.

The peak current stress I_{sp} for power switches S_1–S_4 is given by

$$I_{sp} = i_{p2}(t_1) + \{i_{d6}(t_1)/N_T\} \tag{2}$$

and $i_{p2}(t_1)$ is estimated as

$$i_{p2}(t_1) = DET_h/L_p \tag{3}$$

where T_h ($T_h = T/2$) is the half-switching interval of the power converter, and D is the duty ratio of the power converter represented by $D = (T_h - T\alpha)/T_h$.

Since inductance L_s is significantly low, operational intervals from t_1 to t_3 and from t_5 to t_6 are small and negligible as depicted in Figure 6. Therefore, current i_{L1} through L_{o1} can be represented as,

$$\begin{cases} n_1 i_{L1}(t_1) = (n_1 + n_2) i_{L1}(t_3) \\ (n_1 + n_2) i_{L1}(t_5) = n_1 i_{L1}(t_6) \end{cases}. \tag{4}$$

Then, the current in diode $i_{d6}(t_1)$ and ΔI_{Lp} can be derived as

$$i_{d6}(t_1) = i_{L1}(t_1) = \frac{I_o}{1-(1-D)N_L} + \frac{\Delta I_L}{2} \tag{5}$$

$$\Delta I_{Lp} = \frac{N_L I_o}{1-(1-D)N_L} + (1 - \frac{N_L}{2})\Delta I_L \tag{6}$$

where, I_o is the output current and can be estimated by

$$I_o = \frac{1}{T_h}\int_0^{T_h} i_{L1}(t)dt, \tag{7}$$

and $\Delta I_L = (1-D)(1-N_L)E_o T_h/L_{d1}$.

Therefore, I_{sp} is estimated by

$$I_{sp} = \frac{DET_h}{L_p} + \frac{1}{N_T}\left\{\frac{I_o}{1-(1-D)N_L} + \frac{\Delta I_L}{2}\right\}. \tag{8}$$

The rectified voltage v_r during a half cycle period can be represented as

$$\begin{cases} v_r = N_L E_o \ for\ t_1 < t \le t_6 \\ v_r = E \quad\ for\ t_6 < t \le t_8 \end{cases}. \tag{9}$$

From Equation (9), the output voltage E_o can be derived as

$$\begin{aligned} E_o &= \tfrac{1}{T_h}\textstyle\int_0^{T_h} v_d(t)dt \\ &= \tfrac{DE}{N_T\{1-(1-D)N_L\}} - \tfrac{L_s I_o}{T_h\{1-(1-D)N_L\}^2}. \end{aligned} \tag{10}$$

When leakage inductance L_s is small properly, the output voltage E_o is calculated as

$$E_o \cong \frac{DE}{N_T\{1-(1-D)N_L\}} \tag{11}$$

Realizing Equations (8) and (10), when the HFT turns ratio N_L is very small as $N_L << 1$, both characteristics of output voltage and current stresses I_{sp} are relatively similar to those of conventional hard-switched interleaving two switches DC-DC forward power converter. However, the main advantages of the interleaving scheme in forward DC-DC converters are reduced ripples in output and input capacitor currents. This enables flexible design to use smaller capacitor banks in input and output to satisfy output voltage ripple requirements. However, the peak currents in the converter circuit are reduced by a factor

of two by using two output inductors which in turn decreases the EMI contents for these topologies. The size and cost of these power converters will reduce by reducing the size of filter capacitor banks.

4. Experimental Results and Discussions

This section presents a precise and concise explanation of the obtained experimental results, their analysis, as well as the experimental conclusions that can be presented. A prototype with power rating of 500 W (E_o = 50 V and output current I_o = 10 A in experiment) 100 kHz breadboard using IGBTs is implemented in the laboratory to confirm the operating principle and validate the analytical steady state characteristics. The design specifications and the circuit parameters of this converter are designed as given in Table 1.

Table 1. Circuit parameters of prototype converter.

S_1–S_4	IRG4PC40W
Vces = 600 V, Ic = 20 A(Tc = 100 °C),	
Coes = 140 pF (at Vcc = 30 V)	
D_1–D_4:*SF8L60*, *VRRM* = 600 V, *IF* = 8 A	
D_5–D_7:	ESAC93M-03, *VRRM* = 300 V, *IF* = 12 A
C_1, C_2	820 pF (parallel connected with S_1 and S_2.)
T_1, T_2:	Np = 23 Turns, Ns = 7 Turns, N_T = 3.3
L_{p1}, L_{p2}:	2.5 mH (HFT Magnetizing inductance)
L_{s1}, L_{s2}:	0.35 µH (HFT Leakage inductance)
L_{o1}, L_{o2}	L_{o1} = 35 µH, L_{o2} = 1.1 µH, N_L = 0.14, k = 0.933
C_o	540 µF

The inductance of magnetization and leakage inductance of the high frequency transformer are utilized for Lp_1, Lp_2 and Ls_1, Ls_2, respectively. The timing signal diagram of the power converter operating by means of a current mode control is illustrated in Figure 7. In order to continue operation with ZVS and ZCS soft-switching, a blanking time t_d and a delay time t_δ are set to 0.5 µs and 0.7 µs, respectively.

The basic timing principle elaborated in the generation of the gating signal is that the pulses generated should be able to turn ON only four semiconductor switches. A pulsed-latch is an ideal sequencing element for high-performance gate signals. The timing signal diagram of the power converter operating by means of a current mode control is implemented practically using the control circuit in Figure 8. The blanking time td and a delay time td are adjusted to continue operation with ZVS and ZCS soft-switching. The circuit composed of two op-amp comparators, latch, oscillator, S-R and T-flip-flops and delay.

Figure 9 shows the voltage current characteristics of the new interleaved two-switches forward converter at Uin = 130 V. The duty cycle of the converter circuit is 0.3, 0.5 and 0.7. It can be seen that all the observed waveforms fit the theoretical analysis well. The experimental wave forms under reduced load with output current of 2 A are shown in Figure 10. The figure shows the switch voltage and current at the mentioned operating conditions. Figures 9 and 10 depict observed voltages and currents waveforms under the specified conditions of E = 260 V, E_o = 50 V, I_o = 10 A and E = 260 V, E_o = 50 V, I_o = 2 A. In both cases, active semiconductor devices S_1 and S_2 operate achieving ZVS soft-switching, and active power switches S_3 and S_4 operate achieving ZCS soft-switching at turn-on and turn-off by realizing low idling and circulation currents.

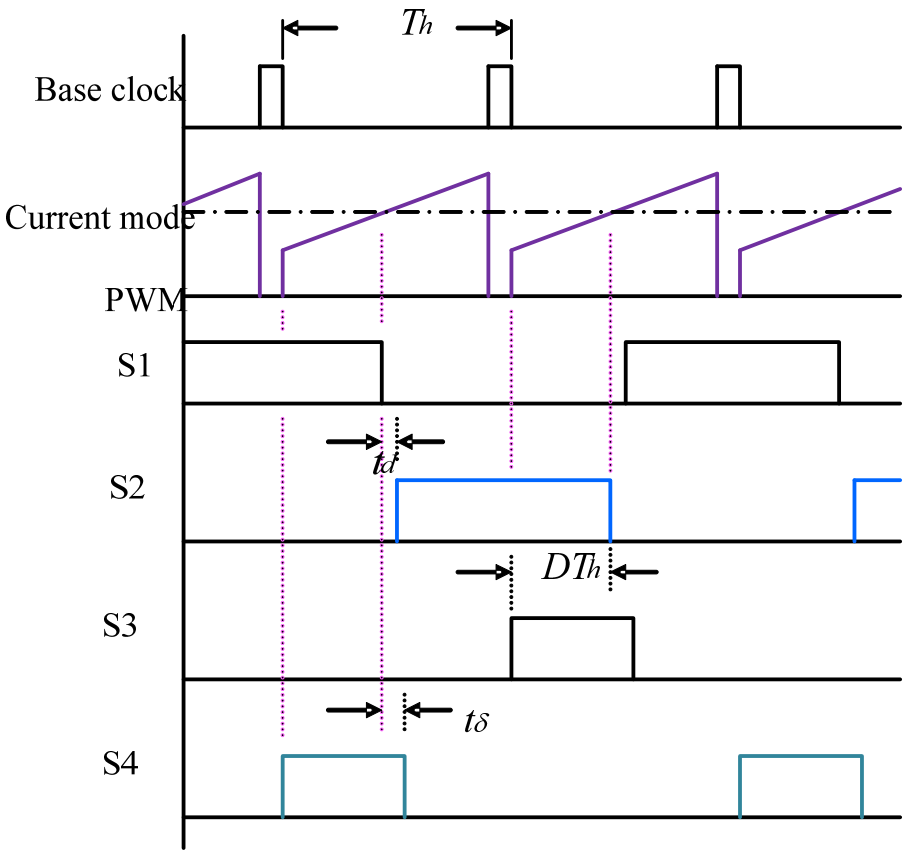


Figure 7. Timing diagram of the controller.

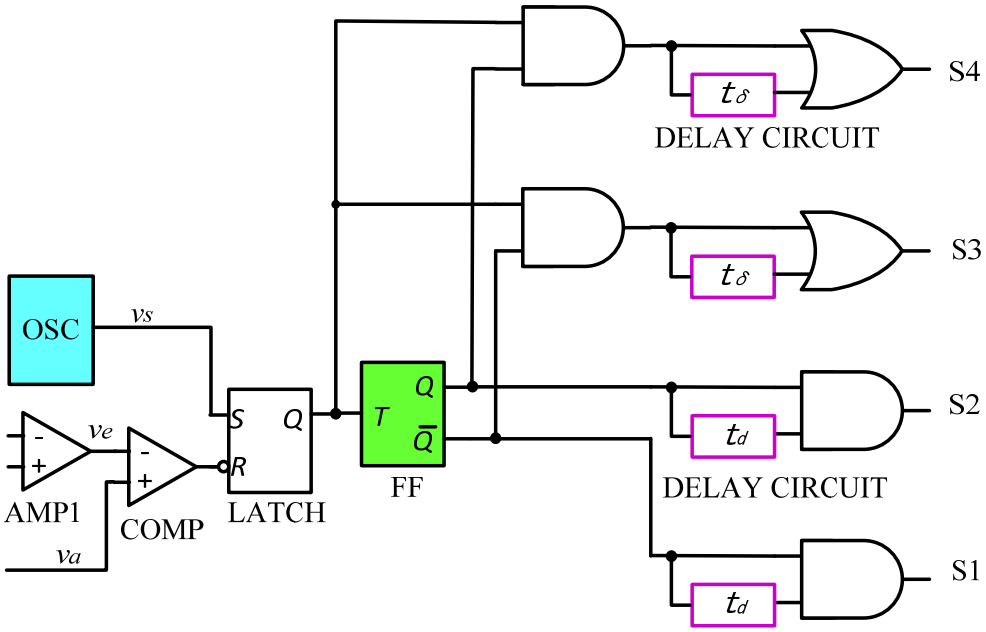
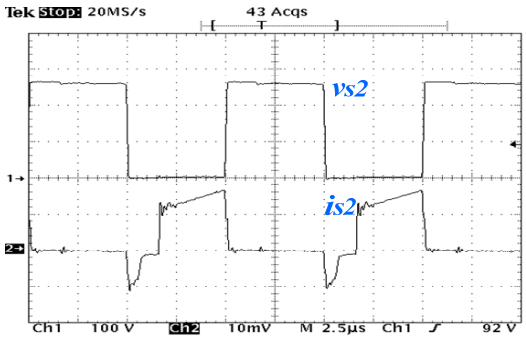
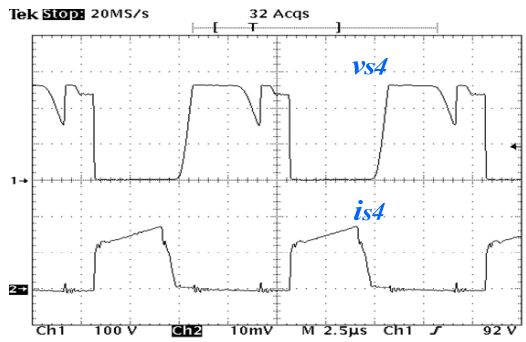


Figure 8. Generation of gate signal for power switches.

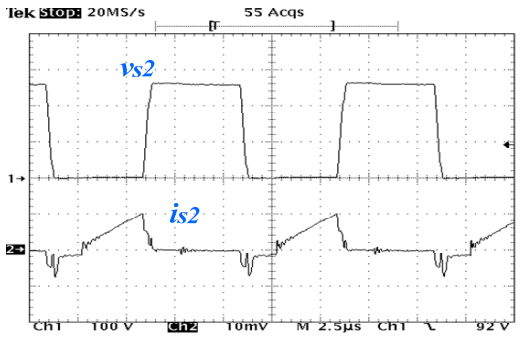


(a)

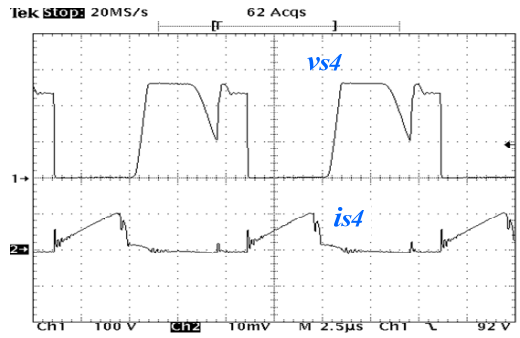


(b)

Figure 9. Experiment waveforms of the prototype at E = 260 V, E_o = 50 V, I_o = 10 A. (v_s.: 100 V/div., i_s: 2 A/div., time scale: 2.5 µs/div). (**a**) Switch S_2 current and voltage (**b**) Switch S_4 current and voltage.



(a)



(b)

Figure 10. Experiment waveforms of the prototype at E = 260 V, E_o = 50 V, I_o = 2 A. (v_s.: 100 V/div., i_s: 2 A/div., time scale: 2.5 µs/div). (**a**) Switch S_2 current and voltage (**b**) Switch S_4 current and voltage.

The output voltage is calculated by Equation (10). The measured and calculated output voltages are plotted versus output current characteristics and shown in Figure 11. The duty cycle is taken as a parameter under using open loop control scheme. One can observe that the reduction of the converter output voltage produced by the existence of leakage inductance *Ls* is noticeably low. The actual measured efficiency is shown in Figure 12 as a function of the output load current in case of constant output voltage equal to 50 V. The achieved power conversion efficiency is equal to 93.5% during full-load operating condition.

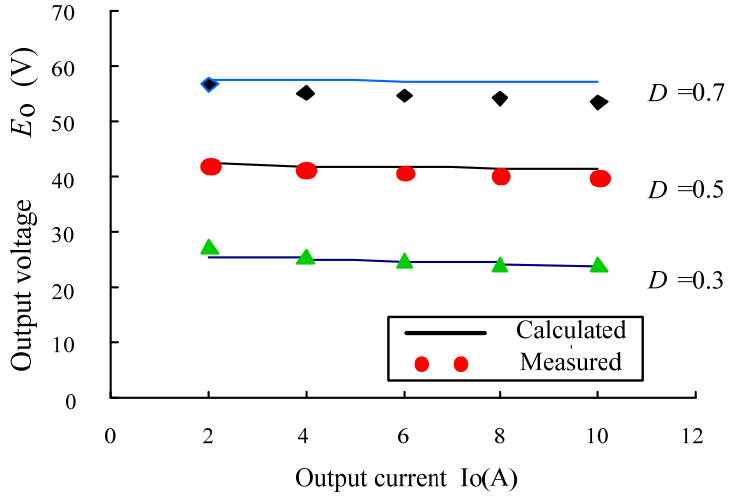


Figure 11. Calculated and measured output voltages versus load current.

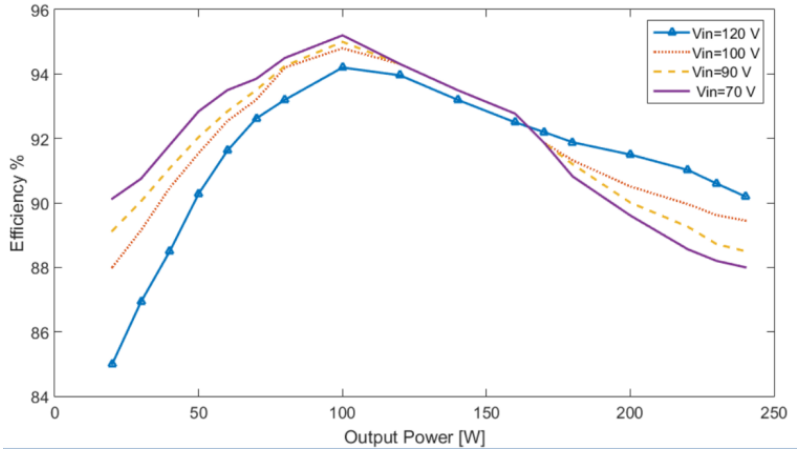


Figure 12. Measured output power at different input voltages.

5. Discussion

In this section, the results are discussed and how they can be interpreted from the perspective of previous studies and of the working hypotheses. The efficiency variation with the output power at different voltages is shown in Figure 12. The measured efficiencies of the proposed converter are evaluated at different input voltages (70 V, 90 V, 110 V and 130 V). The tested results indicate the benefits of the unique architecture. High energy efficiency over wide input voltage range is achieved. Table 2 shows the calculated voltage and current stresses appear during operation for each power converter. A comparative evaluation is made for voltage and current stresses of the implemented converter from a practical point of view. However, the output voltage reduction caused by the forward voltage dropping on the active power switches and diodes, and the effective duty cycle decrease due to the leakage inductances of the high-frequency transformer HFT

are approximately assessed totally as 3 V. Although the current ripple of output inductor in the studied DC-DC power converter is pretty considerable, the RMS current stresses on the inductor and the active power switches are nearly the same as compared with those of the hard-switching DC-DC power converter. The experimental results take conduction power losses of the implemented soft-switched DC-DC power converter as low as those of the hard-switched DC-DC power converter.

Table 2. Comparison of voltage and current stresses of the proposed and conventional converter.

	Conventional Hard-Switching Converter		**Proposed Soft-Switching Converter**	
Input parameters.	$E_{\min} = 220$ V, $E = 260$ V, $E_o = 53$ V, $I_o = 10$ A, $f_s = 100$ kHz, $D_{\max} = 0.8$, $L_d = 35$ μH.		$E_{\min} = 220$ V, $E = 260$ V, $E_o = 53$ V, $I_o = 10$ A, $f_s = 100$ kHz, $D_{\max} = 0.8$, $L_{d1} = 35$ μH, $N_L = 0.14$.	
Turns ratio of the HFT transformer.	$N_T = \frac{D_{\max} E_{\min}}{E_o}$	3.32	$N_T = \frac{D_{\max} E_{\min}}{\{1-(1-D_{\max})N_L\}E_o}$	3.42
Duty cycle under rated voltage operation E.	$D = \frac{N_T E_o}{E}$	0.677	$D = \frac{(1-N_L)N_T E_o}{E-N_T N_L E_o}$	0.664
Current ripple in the output inductor (peak-to-peak ripple).	$\Delta I_{LP} = \frac{(1-D)E_o T_h}{L_{d1}}$	2.45 A	$\Delta I_{LP} = \frac{N_L I_o}{1-(1-D)N_L} + (1 - \frac{N_L}{2})\Delta I_L$	3.51 A
Output inductor RMS current.	$I_{Lrms} = I_o$	10.0 A	$I_{L1rms} = \frac{I_o\sqrt{D+(1-D)(1-N_L)^2}}{1-(1-D)N_L}$	10.0 A
Peak current through active power switches.	$I_{SP} = \frac{1}{N_T}\left\{I_o + \frac{\Delta I_{Lp}}{2}\right\}$	3.38 A	$I_{SP} = \frac{1}{N_T}\left\{\frac{I_o}{1-(1-D)N_L} + \frac{\Delta I_L}{2}\right\}$	3.39 A
Average current through the active power switches.	$I_{SAV} = \frac{DI_o}{2N_T}$	1.02 A	$I_{SAV} = \frac{1}{2N_T}\left\{\frac{DI_o}{1-(1-D)N_L}\right\}$	1.02 A
RMS current through active power switches.	$I_S = \frac{\sqrt{D}I_o}{\sqrt{2}N_T}$	1.75 A	$I_S = \frac{1}{\sqrt{2}N_T}\left\{\frac{\sqrt{D}I_o}{1-(1-D)N_L}\right\}$	1.77 A
Peak voltage on the active power switches.	$V_{SP} = E$	260 V	$V_{SP} = E$	260 V

Figure 13 shows efficiency comparison for the new and conventional interleaved forward power converter in case of 130 V input voltage. It seems that the higher the output power, the lower the efficiency. It is because the conduction losses are the major parts of total losses. All the parameters and devices of the two forward converters are the same except that the resistors RC1 and RC2 in the conventional forward converter are 510 Ω. It is obvious that the new converter can achieve higher conversion efficiency compared with the conventional one, because most of the magnetizing and leakage energy of the transformer is recycled.

References [21–24] proposed a series of schemes to improve the performance of two-switch forward converter. Among them, references [40–42] have the functions of improving duty cycle and soft switching. However, all of them used auxiliary switches, which will increase the complexity of the topology. In addition, these topologies generally have high voltage stress problem in switches.

Table 3 gives a comparison between the proposed and previous circuits in terms of rating and voltage stresses on switches.

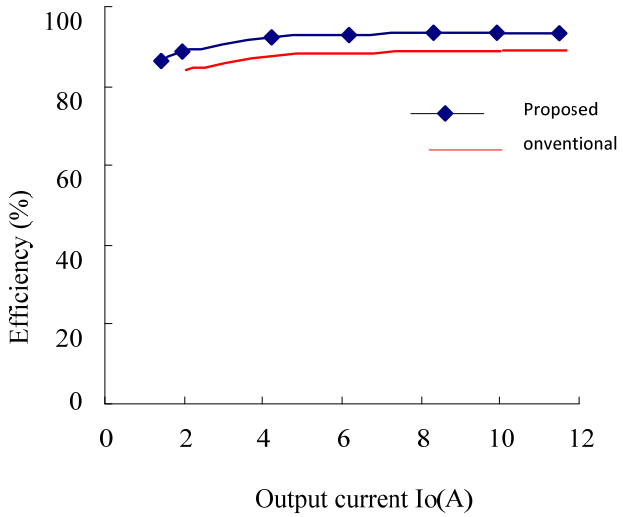


Figure 13. Efficiency comparison between the conventional and developed converter.

Table 3. Comparison between the proposed and previous.

	Paper [24]	**Paper [21]**	**[42]**	**[6]**	**Proposed**
Input voltage *E*	260	250–400	320–400	260	220–260
Output voltage *Vo*	50	54	48	50	53
Output current	10 A	5 A	10 A	10 A	10 A
Switching frequency fs	100 kHz	100	100 kHz	100 kHz	100 kHz
N_T Turns ratio	3.5:1	50:20	60:10	23:7:3.3	23:7:7
Voltage stress S_1–S_4 D_5–D_6	E E/NT-Vo	E 2E/NT	E 2E/NT	E 2E/NT	E E/NT-Vo

6. Conclusions

A soft-switched two switch interleaved forward PWM DC-DC power converter using ultrafast IGBTs has been presented as a new generation converter topology in this paper for telecommunication plants. Its operating principle of this converter has been verified with steady-state analysis and experimentally tested by 500 W–100 kHz breadboard using ultrafast IGBTs. The proposed soft-switched PWM-DC-DC converter circuit is characterized by the following exceptional characteristics:

- The switching losses are low through a wide-ranging of load variation.
- Circulating currents are low, resulting in a low amount of conduction losses.
- No need for using additional auxiliary snubber circuits.
- No existence of flux imbalance in the two high frequency transformer windings because of the existence of forward configuration of the converter.

Compared with the bridge converter, the two-switch forward converter has many advantages, such as simple structure, high stability, and simple magnetic reset method. Thus, it is very suitable for high reliability applications. The transformer in the forward converter can only excite in one direction, which means its core volume is larger than that of the bridge converter. However, in a high frequency working environment, it is the thermal stress produced by core loss, rather than the saturated flux density, that plays a major role in constraining the flux swing. Therefore, in a high frequency environment, the problem of the forward converter core size increasing is eliminated.

In the future, the transient analysis of this converter should be assessed from an experimental point of view.

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