electronics

MDPI

Article

Fault Diagnosis and Tolerant Control for Three-Level T-Type Inverters

Kuei-Hsiang Chao *, Long-Yi Chang and Chien-Chun Hung

Department of Electrical Engineering, National Chin-Yi University of Technology, Taichung 41170, Taiwan
* Correspondence: chaokh@ncut.edu.tw; Tel.: +886-4-2392-4505 (ext. 7272); Fax: +886-4-2392-2156

Abstract: This paper proposes a fault diagnosis system for inverters based on a cerebellar model articulation controller (CMAC). First, a three-level T-type inverter was implemented and used to create a three-level T-type inverter test environment for measuring the output voltage waveforms of faulty power transistors on the main inverter circuit under different output frequencies. The measured waveforms were processed using a fast Fourier transform (FFT) algorithm to create frequency spectrum diagrams and extract the characteristic spectra of corresponding faulty switches. Then, the associations of the spectra were determined and applied as training data for the CMAC to detect the positions of the faulty power transistors. The test results demonstrated that the proposed induction motor fault diagnosis system is capable of fast algorithm, requires less data to train, and has excellent accuracy of identification, with an error margin of ±5%. The detection results were then processed using a fault-tolerant controller (FTC) to enhance the reliability of the proposed system. Finally, some simulations and experimental results were conducted and analyzed to validate the feasibility of the proposed FTC system.

Keywords: cerebellar model articulation controller; T-type inverter; characteristic spectrum; fault diagnosis; fault-tolerant control

Citation: Chao, K.-H.; Chang, L.-Y.; Hung, C.-C. Fault Diagnosis and Tolerant Control for Three-Level T-Type Inverters. *Electronics* **2022**, *11*, 2496. https://doi.org/10.3390/electronics11162496

Academic Editor: Lucia Frosini

Received: 31 May 2022
Accepted: 28 July 2022
Published: 10 August 2022

1. Introduction

Compared with two-level inverters, multi-level inverters [1–5] demonstrate reduced voltage stress on the switches and change in output voltage (dv/dt). They are suitable for high-power applications, and their cascaded arrangement of power transistors facilitate the formation of step-shaped wavelets in the output line-to-neutral point voltage waveform, creating trapezoidal voltage waveforms (similar to sine waveforms) that reduce harmonic content. Multi-level inverters can be categorized into diode-clamped, T-type, cascaded h-bridge (CHB), and flying capacitor inverters. Among these categories, the three-level, diode-clamped inverter is a widely applied inverter that is simple and easy to control [6]. This type of inverter is equipped with a capacitor that evenly divides the voltage from the direct current (DC) side into three voltage levels ($+V_{dc}/2$, 0, and $-V_{dc}/2$). Therefore, the output voltage comprises three states and requires diodes and switches to clamp the output voltage of the inverter to the neutral-point voltage of the DC side. The three-level T-type inverter proposed by Schweizer and Kolar [7], which is an inverter that does not require diode clamping, was examined in this paper. This inverter adopts common emitter-cascaded power transistors to achieve neutral-point voltage clamping rather than the use of additional diodes by diode-clamped inverters. The three-level T-type inverter effectively enhances the reliability and reduces the cost of the system. However, factors such as extended overcurrent (high temperature) operations, component aging, and drive circuit malfunction may damage the switches and hinder normal operations. To resolve these issues, multi-level inverter designs must take into account fault detection mechanisms and fault-tolerant control (FTC) capabilities to ensure that the inverter can maintain normal operations when a fault occurs [8–10].

Number or waveforms were directly used to represent the fault diagnosis information produced by early measuring instruments for the motor drive system. Fault points can be detected quickly and easily using these results. However, experienced personnel must be present to interpret the diagnostic information, detect the fault type, and engage in the maintenance or replacement of relevant components. This traditional fault diagnosis method has often led to detection error and waste of time and manpower for unnecessary maintenance and replacement [11–13]. Therefore, developing new techniques to diagnose system faults has been a longstanding focus of research. A number of scholars in Taiwan and other countries have centered their efforts on developing new diagnostic techniques [14–17]. Extant fault detection and diagnosis methods can be characterized into three major types, specifically, model-based techniques, expert system, and artificial intelligence (AI) algorithms. Model-based techniques are effective diagnostic methods. However, assumptions and limitations are unavoidable in model-based techniques due to the difficulty of building inverter models (including snubber capacitance and balance resistors) and the parasitic nature of inverters. Expert systems are often used in large systems. They effectively adjust systems but require experts to construct the entire system, which can be extremely costly. By comparison, AI algorithms require neither models nor expert knowledge [18–21]. Rather, they rely on the initial training data of normal and abnormal conditions, making them extremely versatile. A variety of AI algorithms is available, including the fuzzy method [22,23] and the neuro-fuzzy method [24]. These methods can be used to establish a fault diagnosis system solely based on the associations between input and output. However, the accuracy of algorithms increases over time. They are also limited to diagnosing single datasets at a given time and rely on expert experience. To overcome these limitations, this paper proposes a CMAC-based fault diagnosis method that adopts fast-learning and highly responsive AI algorithms.

A three-level T-type inverter was used to test the performance of the proposed system in detecting the positions of faulty power transistors. Subsequently, an FTC was used to maintain the operation reliability of the inverter. The CMAC-based fault diagnosis system for inverters architecture is illustrated in Figure 1.

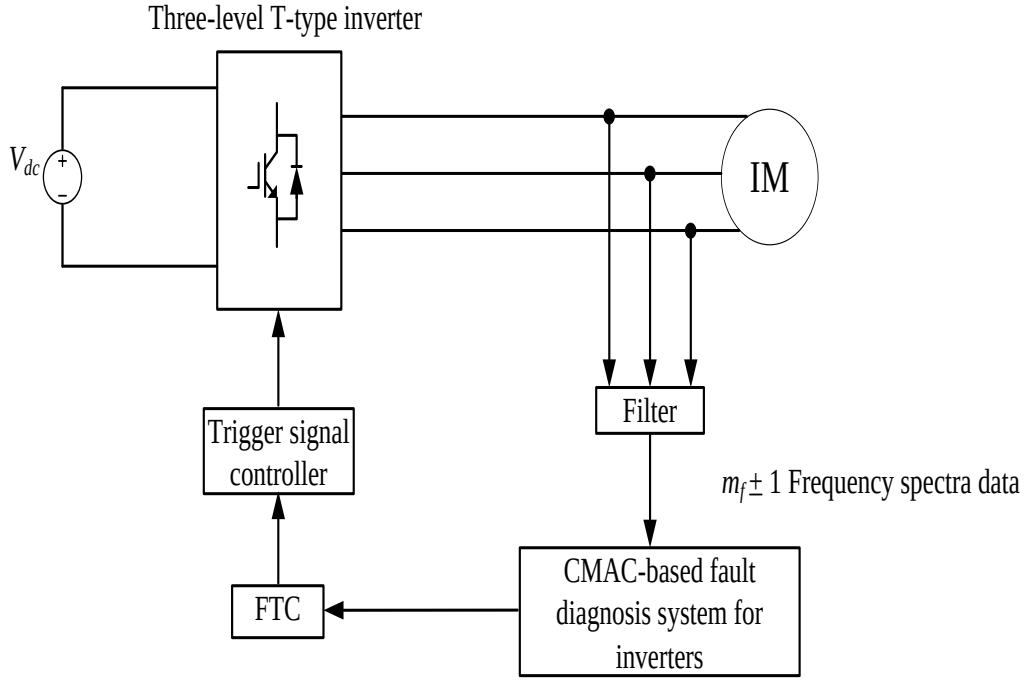


Figure 1. The CMAC-based fault diagnosis system for inverter architecture.

2. Fault Characteristics of Three-Level Inverters

The three-level T-type inverter circuit illustrated in Figure 2 was used to analyze the fault diagnosis system. The time command pulse width modulation (PWM) scheme of switches is generated using the comparison between the three-phase balanced sinusoidal waves ($v_{\sin\_a}$, $v_{\sin\_b}$, and $v_{\sin\_c}$) and triangular waves (v_{tri_1} and v_{tri_2}) as shown in Figure 3. In addition, the $S_{X1}{}^{+}$ and $S_{X1}{}^{-}$, and $S_{X2}{}^{+}$ and $S_{X2}{}^{-}$ must be controlled into a complementary state. Take a-phase as an example: when $v_{\sin\_a} > v_{tri\_1}$, let the power transistors $S_{a1}{}^{+}$ and $S_{a2}{}^{+}$ be turned on and $S_{a1}{}^{-}$ and $S_{a2}{}^{-}$ be turned off. If $v_{tri\_1} > v_{\sin\_a} > v_{tri\_2}$, let the power transistors $S_{a2}{}^{+}$ and $S_{a1}{}^{-}$ be turned on and $S_{a1}{}^{+}$ and $S_{a2}{}^{-}$ be turned off. However, if $v_{\sin\_a} < v_{tri\_2}$, then let the power transistors $S_{a1}{}^{-}$ and $S_{a2}{}^{-}$ be turned on and $S_{a1}{}^{+}$ and $S_{a2}{}^{+}$ be turned off. The power transistors of *b*-phase and *c*-phase can be controlled with the same control strategy. Generally, inverter faults can largely be categorized into three types, namely, short-circuit fault, open-circuit fault, and trigger signal mistransmission. Short-circuit faults occur when an excessive electrical voltage travels through a switch without resistance. Open-circuit faults occur when power transistors fail to transmit trigger signals to the appropriate channels. Trigger signal mistransmission occurred when switches received erroneous trigger commands.

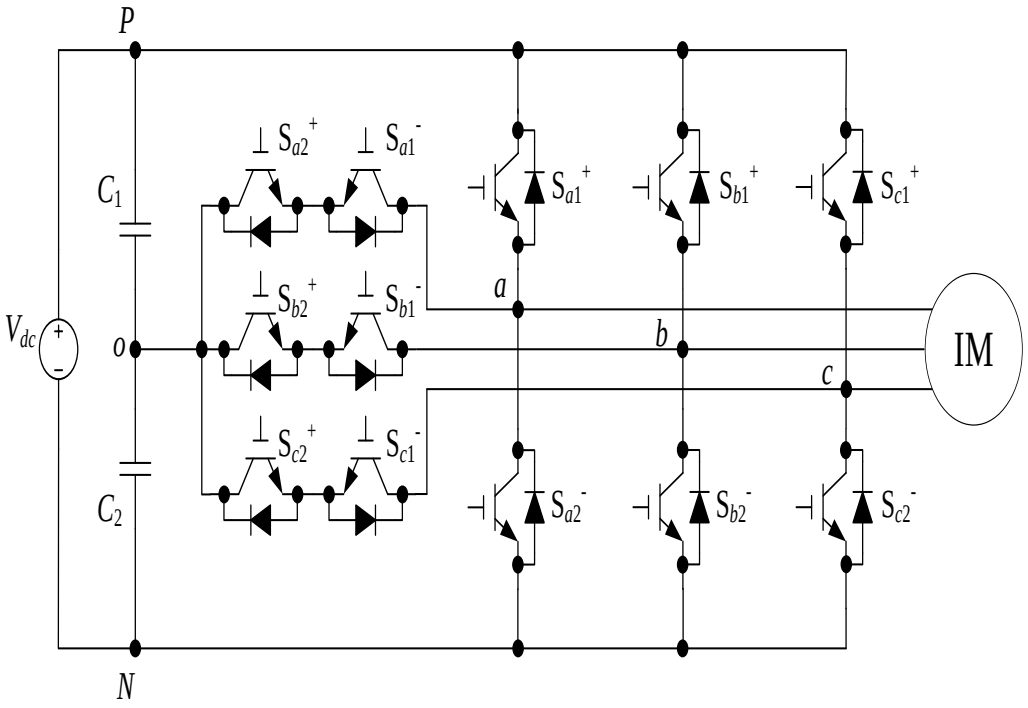


Figure 2. The three-level T-type inverter architecture.

A practical three-level T-type inverter was implemented and used to create a test environment. A switch fault at a random point in time was tested. Measured outcomes indicated that the waveforms produced by the inverter achieved three-phase balance during normal operation. When the inverter operated at a working frequency of 60 Hz without faulty power transistors, the inverter produced output waveforms and frequency spectra similar to those illustrated in Figures 4 and 5. Figure 4 shows that the size and shape of the various phase voltage waveforms were similar with a mutual phase difference of 120°. These are typical three-phase balance characteristics. When a fault occurs in any of the switches in the inverter, the characteristics in Figure 4 would change. For example, when a fault occurred in switch $S_{a1}{}^{+}$, the waveform of the *a*-phase output voltage (v_{ao}) distorted (Figure 6). Figure 7 illustrates the waveform of the *b*-phase voltage (v_{bo}) when a fault occurred in switch $S_{b2}{}^{-}$. The figure clearly shows a significant difference between the waveform of the voltage (v_{bo}) during normal and faulty conditions. Figure 8 illustrates

the waveform of the *c*-phase voltage (v_{co}) when a fault occurred in switch ${S_{c1}}^+$. The figure clearly shows waveform distortion in the output phase voltage of the *c* arm (v_{co}). The waveform of the *a*-phase output voltage (v_{ao}) of the inverter with a fault in switch ${S_{a1}}^+$ shown in Figure 6 is same as the waveform of the *c*-phase output voltage (v_{co}) of the inverter with a fault in switch ${S_{c1}}^+$ shown in Figure 8, but the phase difference is 120°.

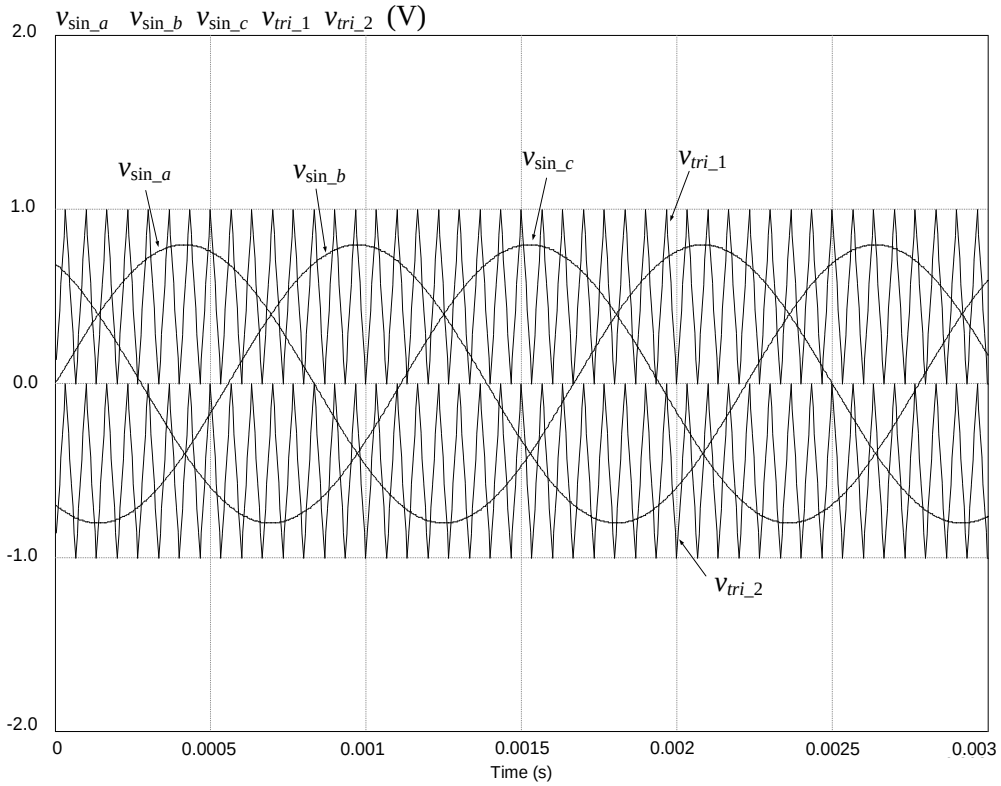
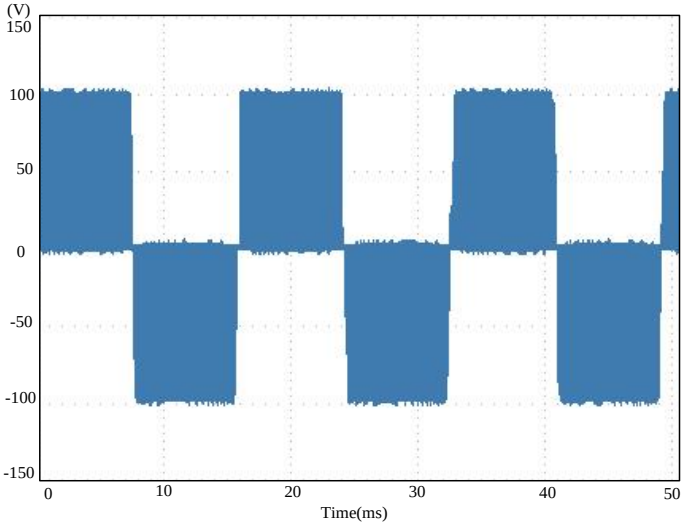


Figure 3. The time command PWM generation scheme of switches for a three−level T−type inverter.

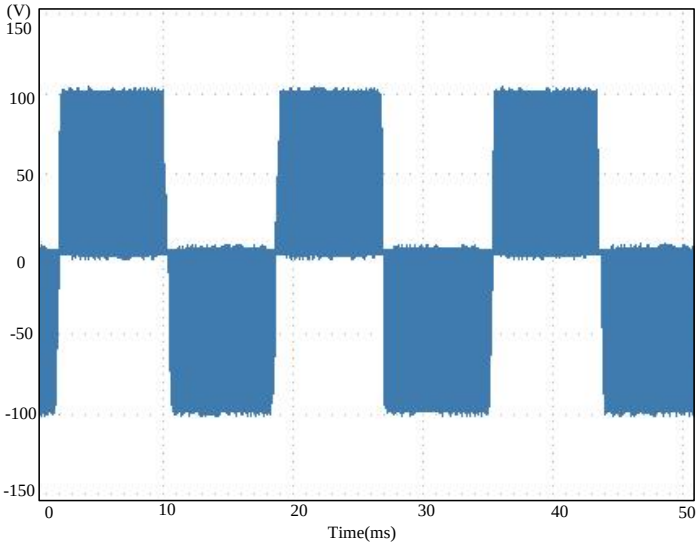
The preceding analysis confirmed the presence of abnormalities in the voltage frequency spectra of the inverter during the occurrence of a fault. Figure 9 illustrates the frequency spectra of the various phase voltages when a fault occurs in switch ${S_{c1}}^+$ at a working frequency of 60 Hz. A comparison between the frequency spectra of Figure 9 and those of the inverter during normal operation (Figure 5) revealed increased variance at $(m_f - 1)th$ and $(m_f + 1)th$ order of the frequency spectra for phase voltage v_{co}. Therefore, the spectral values at a working frequency of 60 Hz were adopted as the characteristic spectra for faults. Subsequently, m_f was defined as the frequency modulation index. The index can be expressed as follows:

$$m_f \triangleq \frac{f_{carrier}}{f_{reference}} = \frac{f_{tri}}{f_{sin}} \tag{1}$$

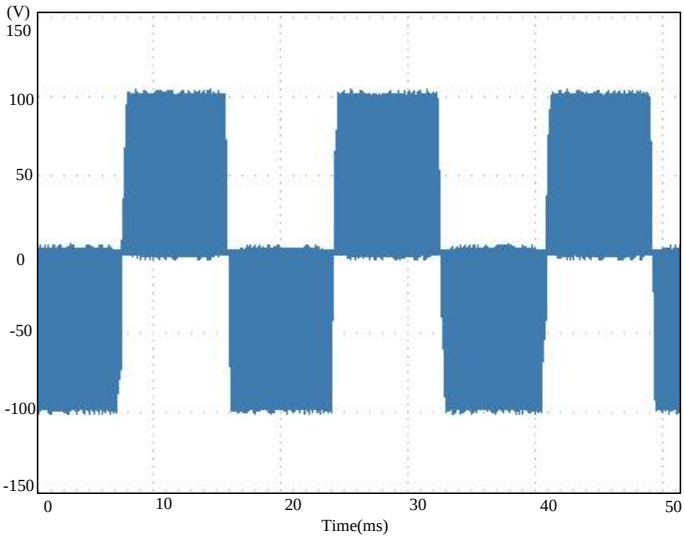
where, f_{tri} represents the frequency of the triangular carrier wave (or the switching frequency of the inverter), and f_{sin} represents the frequency of the sine wave (or the working frequency of the inverter). Parameter data concerning power transistor faults can be retrieved from the measured and analysis results. A CMAC was used to create a fault diagnosis system for inverters to detect faults in the main three-level T-type inverter circuit during switching.



(**a**)



(**b**)



(**c**)

Figure 4. Output voltage waveforms of the inverter at a working frequency of 60 Hz with no switch faults: (**a**) phase voltage v_{ao}; (**b**) phase voltage v_{bo}; (**c**) phase voltage v_{co}.

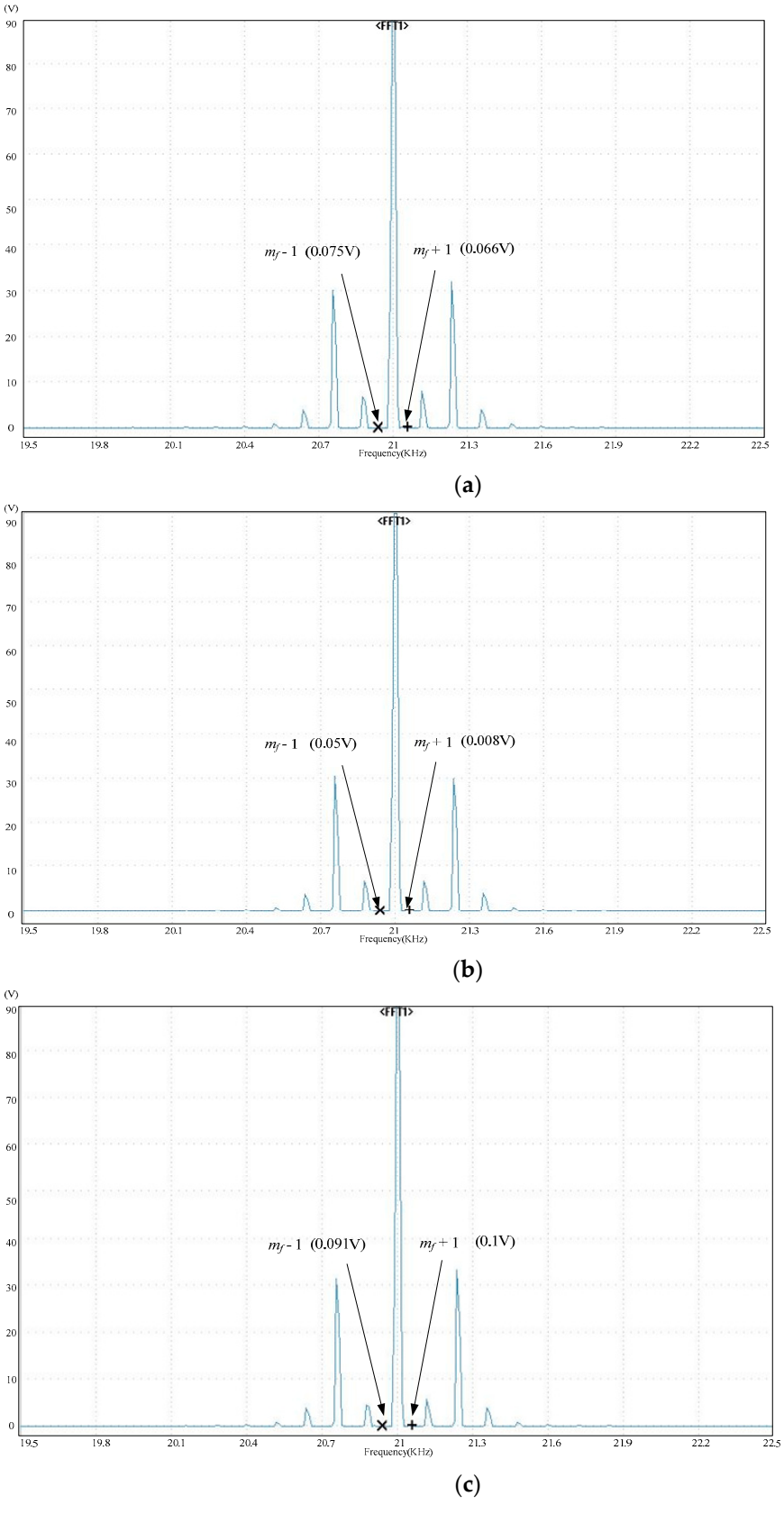


Figure 5. The frequency spectra of the various phase voltages of the inverter at a working frequency of 60 Hz with no switch faults: (**a**) phase voltage v_{ao}; (**b**) phase voltage v_{bo}; (**c**) phase voltage v_{co}.

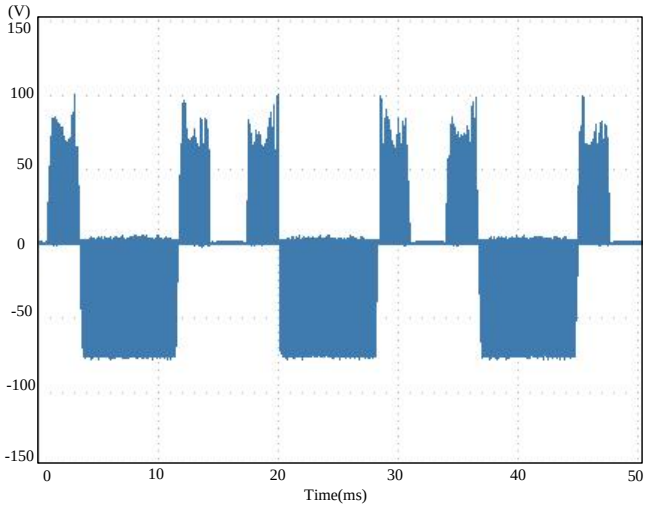


Figure 6. Waveform of the *a*-phase output voltage (v_{ao}) of the inverter at a working frequency of 60 Hz with a fault in switch ${S_{a1}}^{+}$.

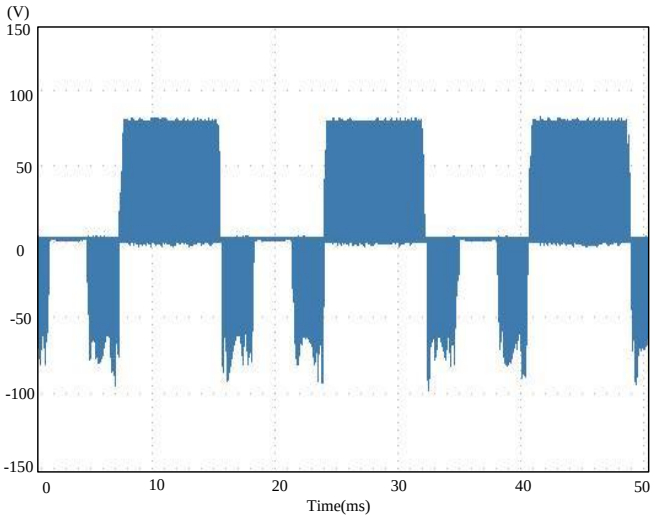


Figure 7. Waveform of the *b*-phase output voltage (v_{bo}) of the inverter at a working frequency of 60 Hz with a fault in switch ${S_{b2}}^{-}$.

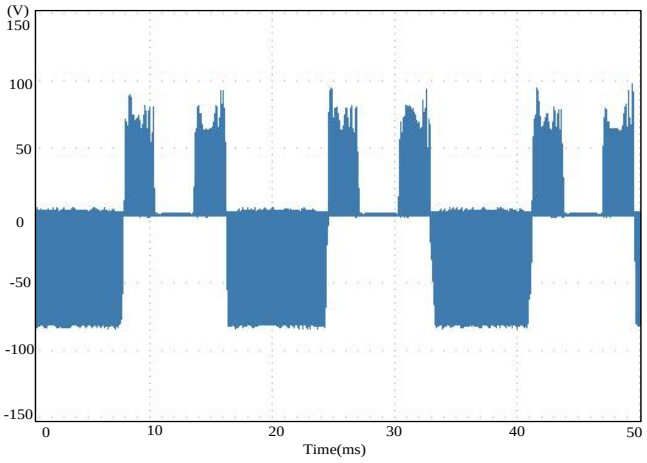
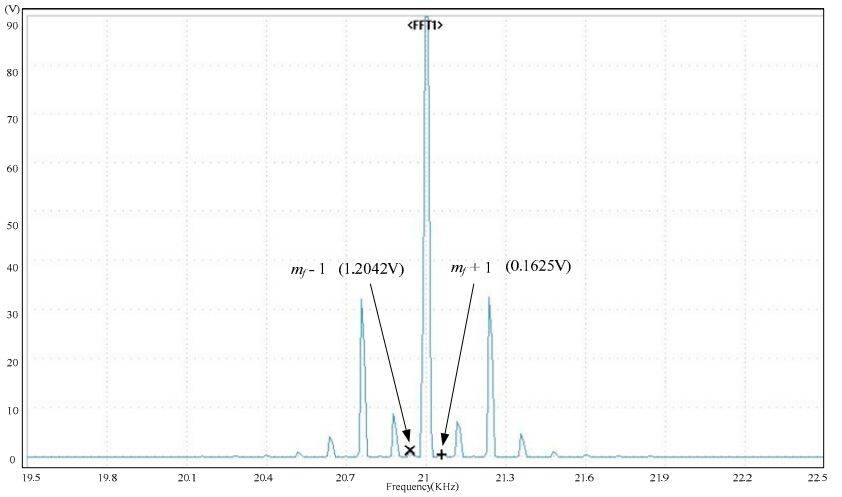
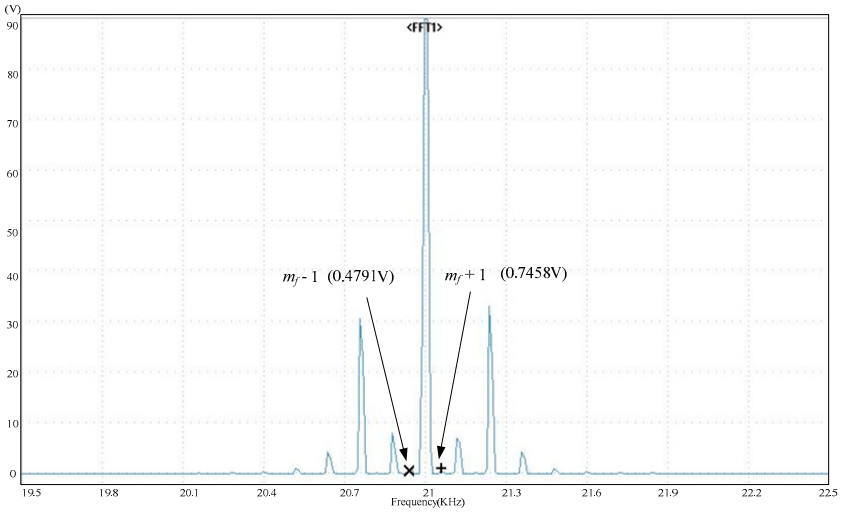


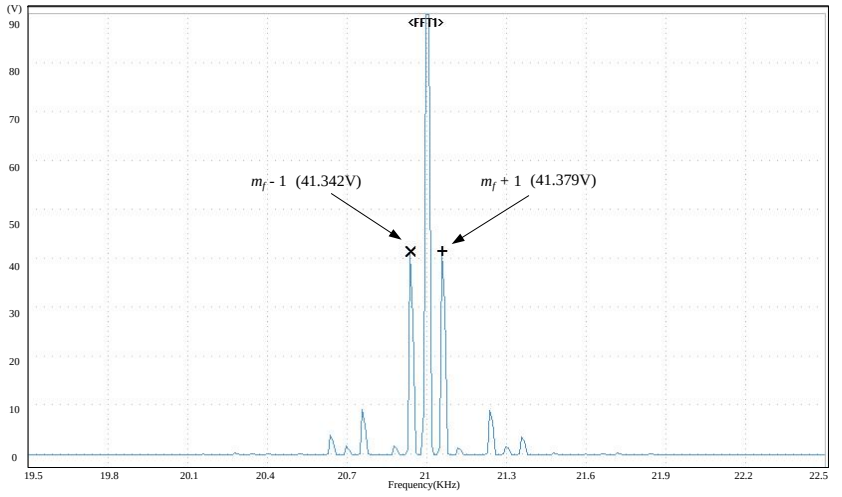
Figure 8. Waveform of the *c*-phase output voltage (v_{co}) of the inverter at a working frequency of 60 Hz with a fault in switch ${S_{c1}}^{+}$.



(**a**)



(**b**)



(**c**)

Figure 9. The frequency spectra of the various phase voltages of the inverter at a working frequency of 60 Hz with a fault in switch $S_{c1}{}^{+}$: (**a**) phase voltage v_{ao}; (**b**) phase voltage v_{bo}; (**c**) phase voltage v_{co}.

3. The Cerebellar Model Articulation Controller

The CMAC was introduced by J. S. Albus in 1970 [25]. The CMAC model mimics the cerebellar neural structure of a human to achieve rapid learning and response characteristics. The CMAC framework is illustrated in Figure 10. The input signals undergo quantization, binary coding, and excitation address coding in the CMAC. The excitation addresses are then summed to generate an output value. The size of the value is analyzed to determine the type of switch fault. Training samples only excite or train their corresponding memory units. For example, the *i*th (i = 1–6) training sample only excites, trains, or tunes the *i*th layer. Therefore, overall training time is drastically reduced [26].

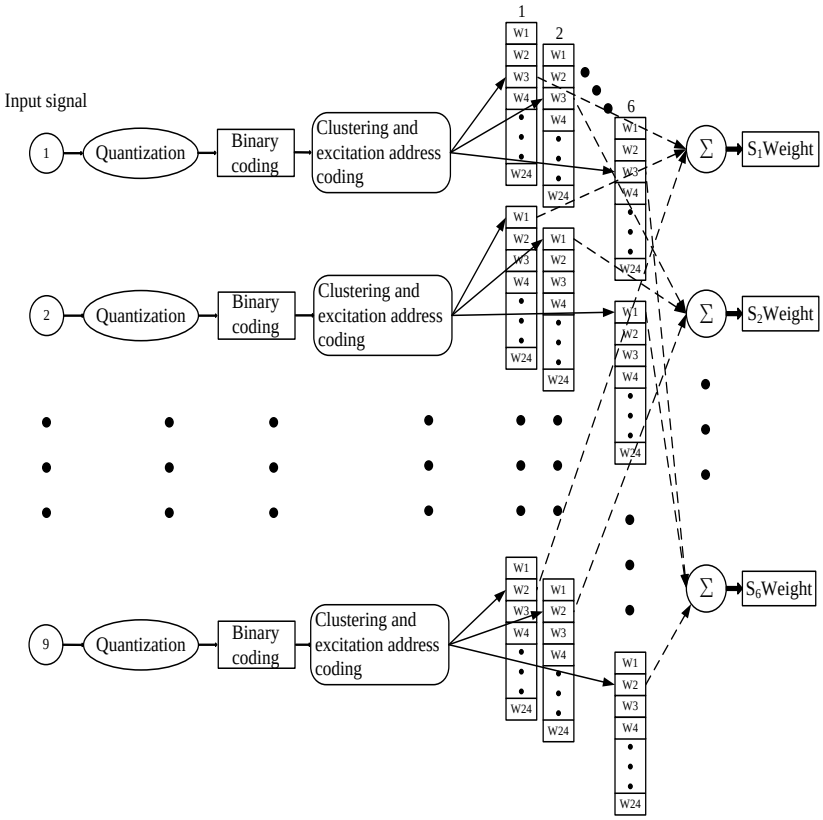


Figure 10. CMAC framework.

3.1. Quantization

A number of equal quantization levels were categorized between the highest and lowest values of the input signals. Quantization levels with higher resolutions are able to produce more detailed quantization codes but demand more free memory. In this paper, the input signals were divided into 255 levels. Levels higher than the maximum value were allocated a quantization value of 255. Levels lower than the minimum value were allocated a value of 0. A corresponding quantization value was allocated to the quantization levels between the maximum and minimum values.

3.2. Excitation Address Coding and CMAC Output Calculation

According to the corresponding quantization levels of the input signals, the values were converted into binary codes. The coded values were then combined and re-coded. Finally, the clusters were provided with a cluster code and an excitation address. For example, the input signals are the voltages at $(m_f - 1)th$ and $(m_f + 1)th$ orders in the three-phase frequency spectrum. Nine difference values are present between the two voltages. Assuming that the levels after quantization were 209, 200, 10, 5, 3, 10, 5, 6, and 5, they are first converted into binary codes (11010001b, 11001000b, 00001010b, 00000101b, 00000011b, 00001010b, 00000101b, 00000110b, and 00000101b) and then combined and re-

coded (110100011100100000001010000001010000001100001010000001010000011000000101b) to obtain a 72-bit code. If the code is clustered every three bits, a total of 24 clusters would be obtained. The excitation addresses for the 24 clusters from the least significant bit (LSB) to the most significant bit (MSB) are n_1 = 101b = 5, n_2 = 000b = 0, n_3 = 000b = 0, n_4 = 011b = 3, n_5 = 000b = 0, n_6 = 010b = 2, n_7 = 001b = 1, n_8 = 000b = 0, n_9 = 010b = 2, n_{10} = 001b = 1, n_{11} = 100b = 4, n_{12} = 001b = 1, n_{13} = 000b = 0, n_{14} = 010b = 2, n_{15} = 001b = 1, n_{16} = 000b = 0, n_{17} = 010b = 2, n_{18} = 001b = 1, n_{19} = 000b = 0, n_{20} = 100b = 4, n_{21} = 100b = 4, n_{22} = 011b = 3, n_{23} = 100b = 4, and n_{24} = 110b = 6. Assuming that the initial weighting of the memory units was 0, then the sum of w_1^5, w_2^0, w_3^0, w_4^3, w_5^0, w_6^2, w_7^1, w_8^0, w_9^2, w_{10}^1, w_{11}^4, w_{12}^1, w_{13}^0, w_{14}^2, w_{15}^1, w_{16}^0, w_{17}^2, w_{18}^1, w_{19}^0, w_{20}^4, w_{21}^4, w_{22}^3, w_{23}^4, and w_{24}^6 would be 0. Hence, the CMAC output can be expressed as follows:

$$y = \sum_{i=1}^{N^*} w_i^{n_i} \tag{2}$$

where y is the actual output value, N^* is the number of excitation addresses, $w_i^{n_i}$ is the weight of the excitation memory, and n_i is the address of the excited memory.

3.3. Memory Weight Tuning

The output target for the CMAC was set as 1.0 in this paper. A supervised learning approach can be used for clear output targets. Subsequently, the steepest descent method was adopted to tune the various weights [27], which can be expressed as follows:

$$w_{i(new)}^{n_i} = w_{i(old)}^{n_i} + \beta \frac{y_d - y}{N^*} \; i = 1, 2, \ldots, N^* \tag{3}$$

where $w_{i(new)}^{n_i}$ is the new weight after tuning the excitation memory, $w_{i(old)}^{n_i}$ is the old weight before tuning the excitation memory, β is the learning gain ($0 < \beta \leq 1$), and y_d is the target value.

3.4. Fault Tolerance

The proposed fault diagnosis method demonstrates excellent interference resistance. Using the 72-bit code characterized in Section 3.2, the original code was changed to 110100011100100000001010000001010000001100001010000001010000011001000101b. After coding the excitation addresses (n_1, n_2, n_3, n_4, n_5, n_6, n_7, n_8, n_9, n_{10}, n_{11}, n_{12}, n_{13}, n_{14}, n_{15}, n_{16}, n_{17}, n_{18}, n_{19}, n_{20}, n_{21}, n_{22}, n_{23}, and n_{24}) changed from 5, 0, 0, 3, 0, 2, 1, 0, 2, 1, 4, 1, 0, 2, 1, 0, 2, 1, 0, 4, 4, 3, 4, and 6 to 5, 0, 1, 3, 0, 2, 1, 0, 2, 1, 4, 1, 0, 2, 1, 0, 2, 1, 0, 4, 4, 3, 4, and 6. A fault occurred only n_3. All other excitation addresses achieved a normal output, suggesting that the method demonstrated excellent fault tolerance. By expanding the number of clusters, the address can be dispersed and stored in more locations, reducing the effects of fault detection in the neighboring bit on output and enhancing accuracy.

3.5. CMAC Training

The training process for the CMAC-based fault diagnosis system for inverters is illustrated in Figure 11. The input training samples first underwent quantization, combined coding, cluster coding, and memory address excitation. The weights of the excitation addresses were then summed to produce an output. Equation (3) was used to tune the memory weights. Once all the samples were trained, the sample weights were analyzed to determine whether the target value was achieved. The training program can be terminated once the target value is achieved. Otherwise, the training program can be terminated once the predetermined number of training sessions has been reached.

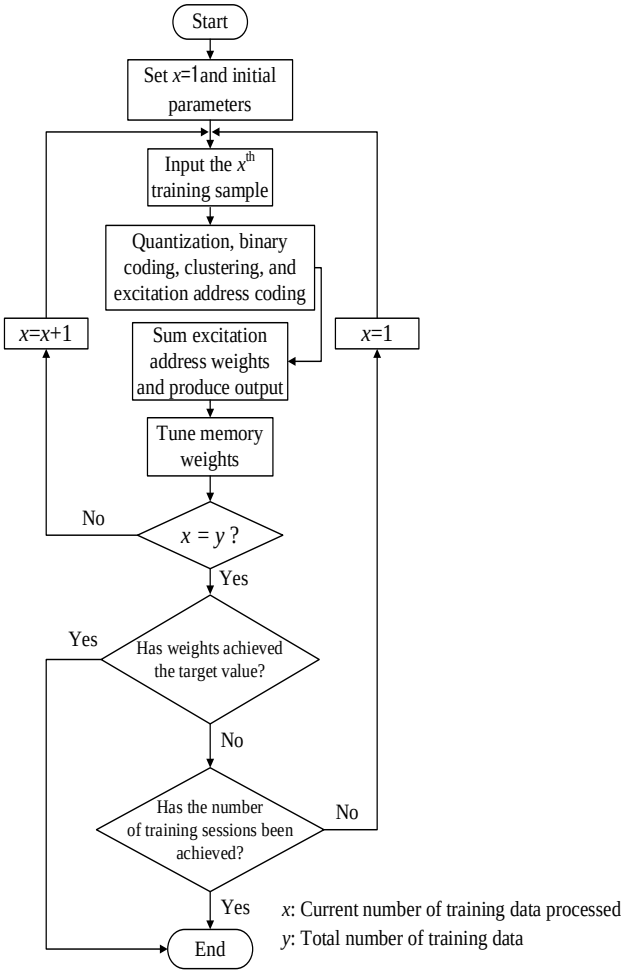


Figure 11. Training flowchart for the CMAC-based fault diagnosis system for inverters.

4. CMAC-Based Fault Diagnosis for Inverters

Extended overcurrent (high-temperature) operations or component aging can cause faults in inverters. The three-level T-type inverter structure illustrated in Figure 2 was used to test switch faults. The proposed CMAC-based system was then employed to detect the positions of faulty power transistors.

First, the measured waveforms of the three-phase voltage in the inverter were processed using a fast Fourier transform algorithm to obtain the voltage spectra at $(m_f - 1)th$ and $(m_f + 1)th$ orders and the difference between them. These values served as the input signals of the CMAC. Switches $S_{a1}{}^{+}$, $S_{a2}{}^{-}$, $S_{b1}{}^{+}$, $S_{b2}{}^{-}$, $S_{c1}{}^{+}$, and $S_{c2}{}^{-}$ served as the different fault types. Moreover, 648 sets of data were collected concerning the faults of the six switches in the inverter at a working frequency between 20 and 90 Hz. The datasets were divided into 432 training data sets and 216 test datasets. The training data sets were processed using the CMAC training model characterized in Section 3.5 to obtain the weights of the different faulty switches. The parameter settings for the CMAC training program are as follows: (1) quantization levels: 255 levels; (2) bits per cluster: 3 bits; (3) cluster quantity: 24 clusters; (4) learning constants (β): 1 constant; and (5) training sessions: 25 times.

Fault detection and diagnosis can commence once the CMAC has been trained. The diagnosis procedures are as follows:

Step 1. Access the weights of the trained CMAC.
Step 2. Access the test data samples.
Step 3. Proceed in the quantization, combined coding, clustering, and excitation address coding of the data.
Step 4. Sum the weights of the excitation addresses to produce an output.

Step 5. Determine the weight of the output (weight value closer to 1 denotes an increased likeliness of fault).
Step 6. Generate fault diagnostic results.

5. Test Results

To detect faulty power transistors, the fault categories were divided into the fault of six switches, specifically, $S_{a1}{}^{+}$, $S_{a2}{}^{-}$, $S_{b1}{}^{+}$, $S_{b2}{}^{-}$, $S_{c1}{}^{+}$, and $S_{c2}{}^{-}$ (Table 1).

Table 1. Fault categories.

Fault Conditions	Category
Fault occurs in $S_{a1}{}^{+}$	F_1
Fault occurs in $S_{a2}{}^{-}$	F_2
Fault occurs in $S_{b1}{}^{+}$	F_3
Fault occurs in $S_{b2}{}^{-}$	F_4
Fault occurs in $S_{c1}{}^{+}$	F_5
Fault occurs in $S_{c2}{}^{-}$	F_6

The characteristic spectral data of the various phase voltages of the inverter operating at 52 Hz, 85 Hz, and 120 Hz with a fault in each of the switches are tabulated in Tables 2–4, respectively. The test data in Tables 2–4 were incorporated into the proposed fault diagnosis system.

Table 2. Characteristic spectral data of the inverter at 52 Hz with different fault categories.

Fault Category	*a*-Phase Characteristic Spectra			*b*-Phase Characteristic Spectra			*c*-Phase Characteristic Spectra		
	$m_f - 1$	$m_f + 1$	Difference	$m_f - 1$	$m_f + 1$	Difference	$m_f - 1$	$m_f + 1$	Difference
F_1	119.613	121.643	2.030	5.313	4.388	0.925	4.758	5.824	1.066
F_2	114.776	124.832	10.056	5.321	5.855	0.534	5.230	5.144	0.086
F_3	5.747	5.700	0.047	120.198	120.783	0.585	5.726	6.377	0.651
F_4	5.991	5.839	0.152	116.877	124.288	7.411	4.527	4.709	0.182
F_5	5.067	5.678	0.611	5.630	4.802	0.828	114.667	125.159	10.492
F_6	6.368	6.210	0.158	4.728	5.491	0.763	122.676	119.228	3.448

Table 3. Characteristic spectral data of the inverter at 85 Hz with different fault categories.

Fault Category	*a*-Phase Characteristic Spectra			*b*-Phase Characteristic Spectra			*c*-Phase Characteristic Spectra		
	$m_f - 1$	$m_f + 1$	Difference	$m_f - 1$	$m_f + 1$	Difference	$m_f - 1$	$m_f + 1$	Difference
F_1	103.875	104.962	1.087	3.451	2.456	0.995	3.154	3.693	0.539
F_2	100.778	106.730	5.952	3.270	3.914	0.644	3.110	2.930	0.180
F_3	3.270	3.141	0.129	103.991	104.641	0.650	3.971	3.995	0.024
F_4	4.109	4.218	0.109	102.684	106.825	4.141	2.568	2.519	0.049
F_5	2.722	3.698	0.976	3.619	2.994	0.625	100.973	107.094	6.121
F_6	3.976	3.638	0.338	2.600	3.613	1.013	105.701	103.733	1.968

Table 4. Characteristic spectral data of the inverter at 120 Hz with different fault categories.

Fault Category	*a*-Phase Characteristic Spectra			*b*-Phase Characteristic Spectra			*c*-Phase Characteristic Spectra		
	$m_f - 1$	$m_f + 1$	Difference	$m_f - 1$	$m_f + 1$	Difference	$m_f - 1$	$m_f + 1$	Difference
F_1	90.164	91.107	0.944	2.995	2.132	0.863	2.738	3.206	0.468
F_2	87.475	92.642	5.166	2.838	3.397	0.559	2.699	2.543	0.156
F_3	2.838	2.726	0.112	90.264	90.828	0.564	3.447	3.468	0.021
F_4	3.567	3.661	0.095	89.130	92.724	3.594	2.229	2.186	0.043
F_5	2.363	3.210	0.847	3.141	2.599	0.542	87.645	92.958	5.313
F_6	3.451	3.158	0.293	2.257	3.136	0.879	91.748	90.040	1.708

The detection outcomes are tabulated in Tables 5–7. The tables show that the system accurately detected the fault data. For example, the detection outcomes in Table 5 generated an output weight of 0.6999 for the test data of F_2 faults in Table 2, which was the highest of all the fault data points, suggesting that the fault was category F_2. To validate the interference resistance of the proposed system, the samples for three working frequencies were tested with an error margin of ±5%. The detection outcomes are tabulated in Tables 8–10. The outcomes show that the proposed system can accurately detect fault categories with or without the presence of error.

Table 5. Detection outcomes of the inverter at 52 Hz with different fault categories.

Fault Category	Output Weight						Detection Outcome
	F_1	F_2	F_3	F_4	F_5	F_6	
F_1	0.7066	0.5039	0.2158	0.1147	0.5605	0.4640	F_1
F_2	0.5594	0.6999	0.1957	0.1363	0.4814	0.4542	F_2
F_3	0.2930	0.2163	0.7419	0.6132	0.5812	0.5308	F_3
F_4	0.2375	0.1476	0.5404	0.6918	0.4793	0.5279	F_4
F_5	0.5462	0.4348	0.5371	0.4375	0.8931	0.7285	F_5
F_6	0.4886	0.4583	0.5007	0.4262	0.7563	0.8933	F_6

Table 6. Detection outcomes of the inverter at 85 Hz with different fault categories.

Fault Category	Output Weight						Detection Outcome
	F_1	F_2	F_3	F_4	F_5	F_6	
F_1	0.7440	0.5517	0.2297	0.2480	0.5754	0.4923	F_1
F_2	0.5552	0.6683	0.2333	0.1660	0.5146	0.5312	F_2
F_3	0.2803	0.2050	0.7136	0.4682	0.5912	0.5467	F_3
F_4	0.2019	0.1526	0.5619	0.5859	0.5076	0.4151	F_4
F_5	0.4780	0.4384	0.4806	0.4135	0.8566	0.6552	F_5
F_6	0.4745	0.4783	0.4386	0.3918	0.7345	0.8697	F_6

Table 7. Detection outcomes of the inverter at 120 Hz with different fault categories.

Fault Category	Output Weight						Detection Outcome
	F_1	F_2	F_3	F_4	F_5	F_6	
F_1	0.7291	0.5406	0.2251	0.2431	0.5639	0.4825	F_1
F_2	0.5441	0.6549	0.2286	0.1627	0.5043	0.5206	F_2
F_3	0.2433	0.2009	0.6993	0.4588	0.5794	0.5358	F_3
F_4	0.1979	0.1495	0.5507	0.5742	0.4974	0.4068	F_4
F_5	0.4684	0.4296	0.4710	0.4052	0.8395	0.6421	F_5
F_6	0.4651	0.4687	0.4298	0.3839	0.7198	0.8523	F_6

In the half-bridge and full-bridge circuits, where two transistors are connected in series in one converter leg, it is important to provide a blanking time so that the turn-on control input to one transistor is delayed with respect to turn-off control input of the other transistor in the inverter leg. This blanking time should be chosen conservatively to be greater than the worst-case maximum storage time of the transistors being used to avoid cross condition. Under normal operation, such a conservatively chosen blanking time ensures that both the transistors in the inverter leg are off. This dead time introduces an unwanted nonlinearity in the converter transfer characteristic. This dead time can be minimized by the use of design enhancements to drive circuits, which minimize turn-on and turn-off delay time in power semiconductor devices being used as the power switches. There are usually only a few us for a power device IGBT. Therefore, its influence on fault diagnosis can be ignored.

Table 8. Detection outcomes of the inverter at 52 Hz with a ±5% error margin.

Fault Category	Error Rate	Output Weight						Detection Outcome
		F_1	F_2	F_3	F_4	F_5	F_6	
F_1	+5%	0.6706	0.5592	0.2090	0.1431	0.5708	0.5251	F_1
	−5%	0.6457	0.4993	0.2439	0.1454	0.5136	0.4768	
F_2	+5%	0.4525	0.7206	0.1111	0.1148	0.4693	0.3698	F_2
	−5%	0.4726	0.6165	0.1711	0.1386	0.4906	0.4526	
F_3	+5%	0.2310	0.2145	0.6713	0.5192	0.5900	0.5044	F_3
	−5%	0.3332	0.2504	0.6910	0.5634	0.5757	0.5640	
F_4	+5%	0.2518	0.0922	0.5670	0.6080	0.4840	0.4681	F_4
	−5%	0.2470	0.1257	0.5595	0.7397	0.5096	0.5351	
F_5	+5%	0.4445	0.4228	0.5517	0.4030	0.9062	0.7037	F_5
	−5%	0.5444	0.4758	0.4715	0.4586	0.8274	0.7609	
F_6	+5%	0.5538	0.4585	0.4769	0.4255	0.7682	0.8771	F_6
	−5%	0.4258	0.4217	0.4987	0.4038	0.7699	0.8961	

Table 9. Detection outcomes of the inverter at 85 Hz with a ±5% error margin.

Fault Category	Error Rate	Output Weight						Detection Outcome
		F_1	F_2	F_3	F_4	F_5	F_6	
F_1	+5%	0.7012	0.4889	0.2386	0.2282	0.5687	0.5251	F_1
	−5%	0.6974	0.5512	0.2385	0.1924	0.5192	0.5309	
F_2	+5%	0.5301	0.6586	0.1823	0.1373	0.5600	0.4343	F_2
	−5%	0.5175	0.6687	0.1922	0.1605	0.5172	0.4643	
F_3	+5%	0.2800	0.2232	0.6873	0.5318	0.5848	0.5731	F_3
	−5%	0.2104	0.1871	0.7173	0.4320	0.6328	0.4432	
F_4	+5%	0.2057	0.1313	0.4782	0.5397	0.4936	0.4091	F_4
	−5%	0.1315	0.1625	0.5224	0.5717	0.5107	0.3889	
F_5	+5%	0.4780	0.4384	0.4806	0.4135	0.8566	0.6552	F_5
	−5%	0.5003	0.4220	0.4237	0.3800	0.7992	0.6669	
F_6	+5%	0.4479	0.4731	0.4328	0.4021	0.7341	0.8639	F_6
	−5%	0.5313	0.4555	0.4687	0.4098	0.6987	0.9409	

Table 10. Detection outcomes of the inverter at 120 Hz with a ±5% error margin.

Fault Category	Error Rate	Output Weight						Detection Outcome
		F_1	F_2	F_3	F_4	F_5	F_6	
F_1	+5%	0.6872	0.4791	0.2338	0.2236	0.5573	0.5146	F_1
	−5%	0.6835	0.5402	0.2337	0.1886	0.5088	0.5203	
F_2	+5%	0.5195	0.6454	0.1787	0.1346	0.5488	0.4256	F_2
	−5%	0.5072	0.6553	0.1884	0.1573	0.5069	0.4550	
F_3	+5%	0.2744	0.2187	0.6736	0.5212	0.5731	0.5616	F_3
	−5%	0.2062	0.1834	0.7030	0.4234	0.6201	0.4343	
F_4	+5%	0.2016	0.1287	0.4686	0.5289	0.4837	0.4009	F_4
	−5%	0.1289	0.1593	0.5120	0.5603	0.5005	0.3811	
F_5	+5%	0.4684	0.4296	0.4710	0.4052	0.8395	0.6421	F_5
	−5%	0.4903	0.4136	0.4152	0.3724	0.7832	0.6536	
F_6	+5%	0.4389	0.4636	0.4241	0.3941	0.7194	0.8466	F_6
	−5%	0.5207	0.4464	0.4593	0.4016	0.6847	0.9221	

6. Fault Tolerance of Three-Level T-Type Inverter

Figure 2 presents the structural diagram of the three-level T-type inverter, revealing that the occurrence of an open-circuit fault in any of the inverter switches ($S_{a1}{}^{+}$, $S_{a2}{}^{-}$, $S_{b1}{}^{+}$, $S_{b2}{}^{-}$, $S_{c1}{}^{+}$, and $S_{c2}{}^{-}$) would cause an abnormal output voltage in the phase and thus result in a three-phase imbalance. The imbalance would change the voltage level of the dc bus, engendering a voltage imbalance in the upper and lower capacitors. This situation would further induce repeated three-phase imbalances in the output voltage. Therefore, to maintain inverter operation in the event of switch failure, the switching state of the inverter and the phase angle of the reference voltage must be adjusted simultaneously to maintain the three-phase balance in the output voltage.

6.1. Fault-Tolerant Control Analysis

Figure 12 shows the phasor diagram of a balanced three-phase voltage of a switch without fault. When the switch $S_{a1}{}^{+}$ or $S_{a2}{}^{-}$ incurs an open-circuit fault, the *a*-phase h-bridge switches ($S_{a1}{}^{+}$ and $S_{a2}{}^{-}$) must be deactivated to activate the neutral-point switches ($S_{a1}{}^{-}$ and $S_{a2}{}^{+}$); specifically, point *a* is connected to the neutral point, and *b* and *c*-phases are still switched normally. The FTC for the occurrence of an open-circuit fault in $S_{a1}{}^{+}$ is shown in Figure 13. The voltage phasor diagram corresponding to this situation is illustrated in Figure 14a. As illustrated in this figure, the phasor positions of the line voltages Vab and Vca in Figure 12 become those of Vab1 and Vca1, with the voltage magnitude decreasing by 0.577 times relative to the original line voltage. The line voltage Vbc1 remains unchanged. However, because the voltage v_{ao} is 0, the phase angle of the *b*-phase voltage should be simultaneously adjusted to be 150° behind that of the *a*-phase voltage, and the phase angle of the *c*-phase voltage should be 150° ahead of that of the *a*-phase voltage. After the occurrence of a fault, the three-phase voltage can still maintain the operation of the balanced three-phase system; the corresponding voltage phasor diagram of the system is shown in Figure 14b. The phasor positions of the line voltages Vab1 and Vca1 presented in Figure 14a shift to those of Vab2 and Vca2, with the magnitude of the line voltage Vbc2 decreasing by 0.577 times relative to that of the original line voltage Vbc1. If an open-circuit fault occurs in the switch $S_{b1}{}^{+}$ or $S_{b2}{}^{-}$, the *b*-phase h-bridge switches ($S_{b1}{}^{+}$ and $S_{b2}{}^{-}$) are deactivated, and the neutral-point switches ($S_{b1}{}^{-}$ and $S_{b2}{}^{+}$) are activated; specifically, point *b* is connected to the neutral point, and the *a*- and *c*-phase switches continue to operate normally. The FTC for the occurrence of an open-circuit fault in $S_{b2}{}^{-}$ is shown in Figure 15. The voltage phasor diagram corresponding to this situation is shown in Figure 16a. The phasor positions of the line voltages Vab and Vbc in Figure 12 shift to those of Vab1 and Vbc1, with the voltage magnitude decreasing by 0.577 times relative to the magnitude of the original line voltage; by contrast, the magnitude of the line voltage Vca1 remains unchanged. However, because the voltage v_{bo} is 0, the phase angle of the *a*-phase voltage should be simultaneously adjusted such that it is 30° ahead of that of the *a*-phase voltage, and the phase angle of the *c*-phase voltage should be 90° ahead of that of the *a*-phase voltage. Figure 16b presents the voltage phasor diagram derived after these adjustments. The phasor positions of the line voltages Vab1 and Vbc1 presented in Figure 16a shift to those of Vab2 and Vbc2, with the magnitude of the line voltage Vca2 decreasing by 0.577 times relative to that of the original line voltage Vca1. Similarly, if an open-circuit fault occurs in the switch $S_{c1}{}^{+}$ or $S_{c2}{}^{-}$, the *c*-phase h-bridge switches ($S_{c1}{}^{+}$ and $S_{c2}{}^{-}$) are deactivated, and the neutral-point switches ($S_{c1}{}^{-}$ and $S_{c2}{}^{+}$) are activated. Point *c* is connected to the neutral point, and the *a*- and *b*-phase switches continue to operate normally. The FTC for the occurrence of an open-circuit fault in $S_{c1}{}^{+}$ is shown in Figure 17. Figure 18a shows the voltage phasor diagram corresponding to this situation. The phasor positions of the line voltages Vbc and Vca shown in Figure 12 switch to those of Vbc1 and Vca1, with the voltage magnitude decreasing by 0.577 times relative to the magnitude of the original line voltage; by contrast, the magnitude of the line voltage Vab1 remains unchanged. However, because the voltage v_{co} is 0, the phase angle of the *a*-phase voltage should be simultaneously adjusted such that it is 30° behind the original *a*-phase voltage, and the phase angle of the *b*-phase voltage

should be 90° behind the original *a*-phase voltage. Figure 18b illustrates the voltage phasor diagram derived after the adjustments. The phasor positions of the line voltages Vbc1 and Vca1 presented in Figure 18a switch to the positions of Vbc2 and Vca2, with the magnitude of Vab2 decreasing by 0.577 times relative to that of the original line voltage Vab1.

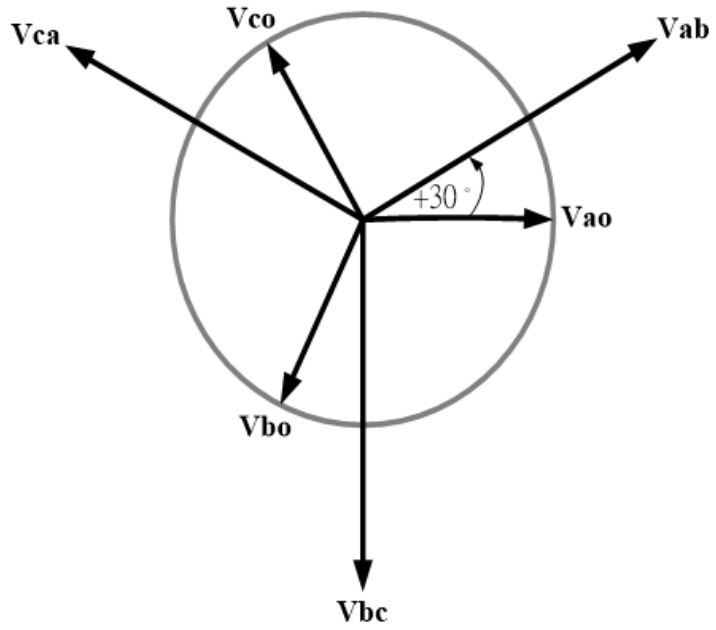


Figure 12. Balanced three-phase voltage phasor diagram of a switch without fault.

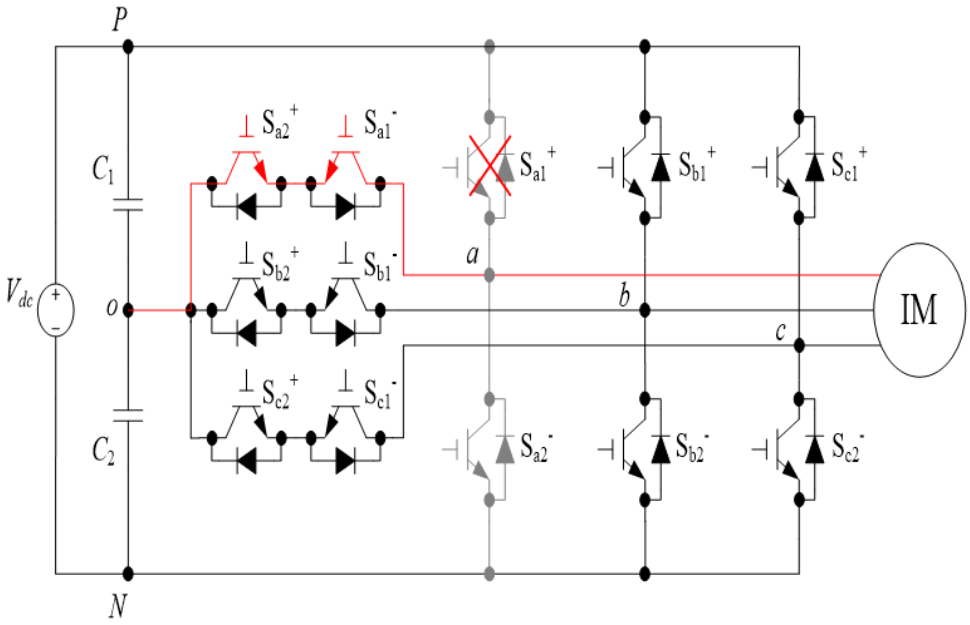


Figure 13. FTC for the occurrence of an open-circuit fault in $S_{a1}{}^{+}$.

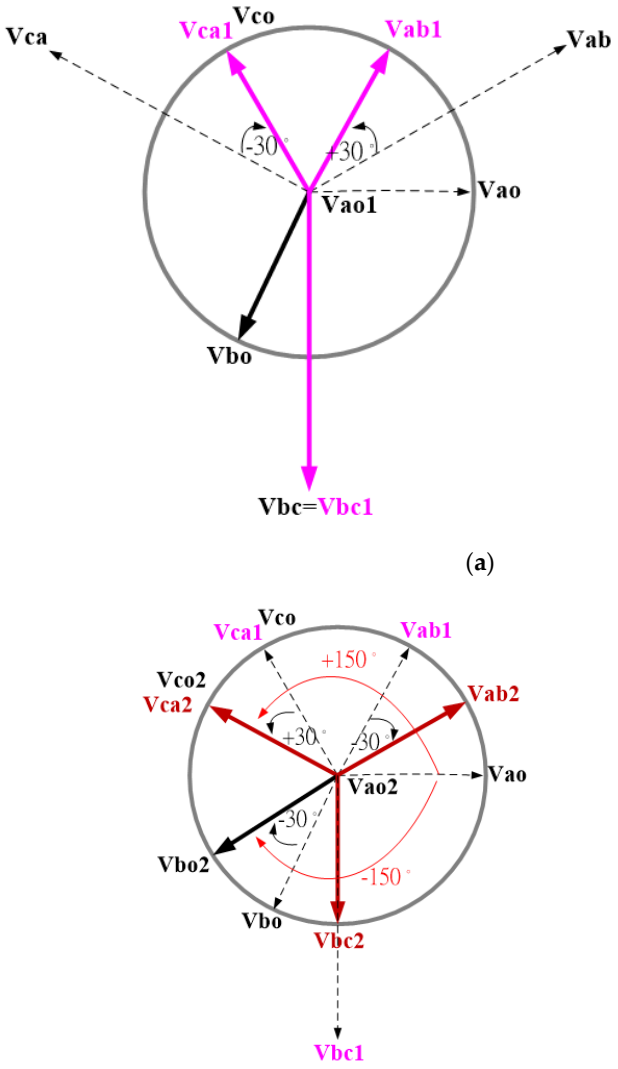


Figure 14. Voltage phasor diagram of fault-tolerant control when a fault occurs in the switch $S_{a1}{}^{+}$ or $S_{a2}{}^{-}$; (**a**) unadjusted voltage phase angle; (**b**) adjusted phase angle of the *b*-phase voltage such that it is 150° behind that of the *a*-phase voltage; adjusted phase angle of the *c*-phase voltage such that it is 150° ahead of that of the *a*-phase voltage.

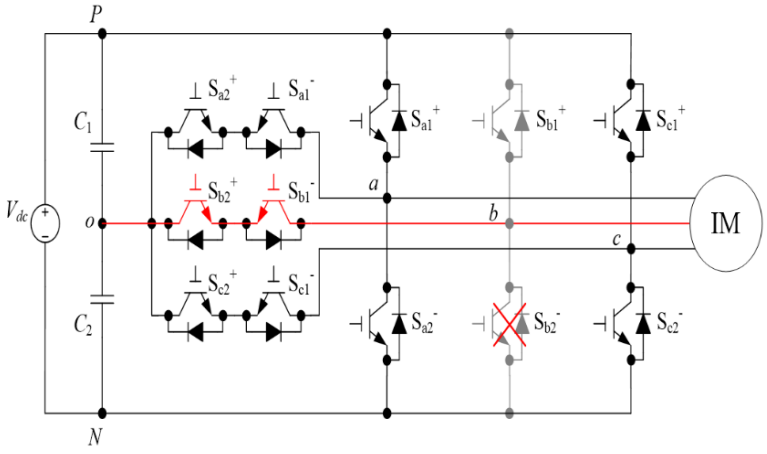
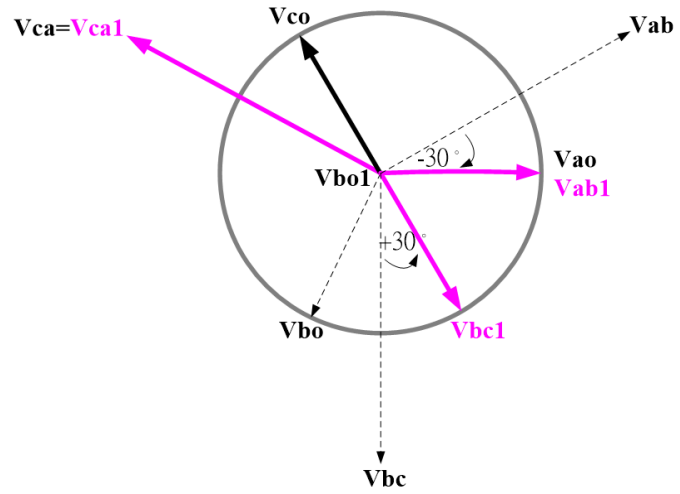
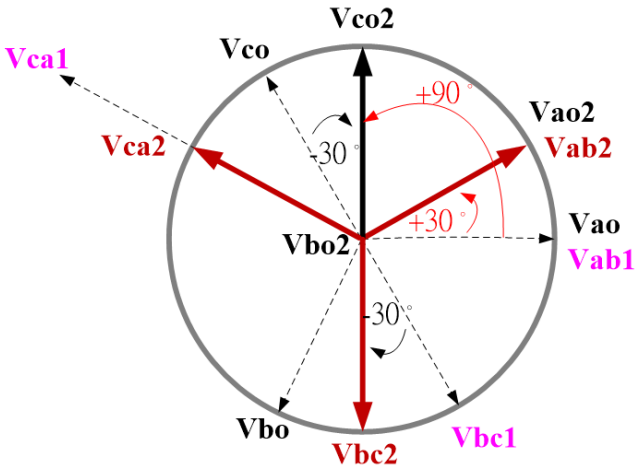


Figure 15. FTC for the occurrence of an open-circuit fault in $S_{b2}{}^{-}$.



(**a**)



(**b**)

Figure 16. Voltage phasor diagram of fault-tolerant control when a fault occurs in the switch $S_{b1}{}^{+}$ or $S_{b2}{}^{-}$; (**a**) unadjusted voltage phase angle; (**b**) adjusted phase angle of the *a*-phase voltage such that it is 30° ahead of the original phase angle of the *a*-phase voltage; adjusted phase angle of the *c*-phase voltage such that it is 90° ahead of the original phase angle of the *a*-phase voltage.

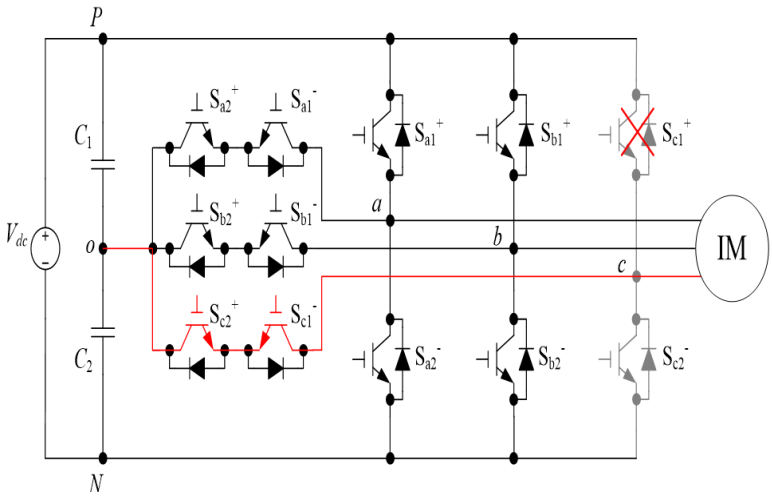


Figure 17. FTC for the occurrence of an open-circuit fault in $S_{c1}{}^{+}$.

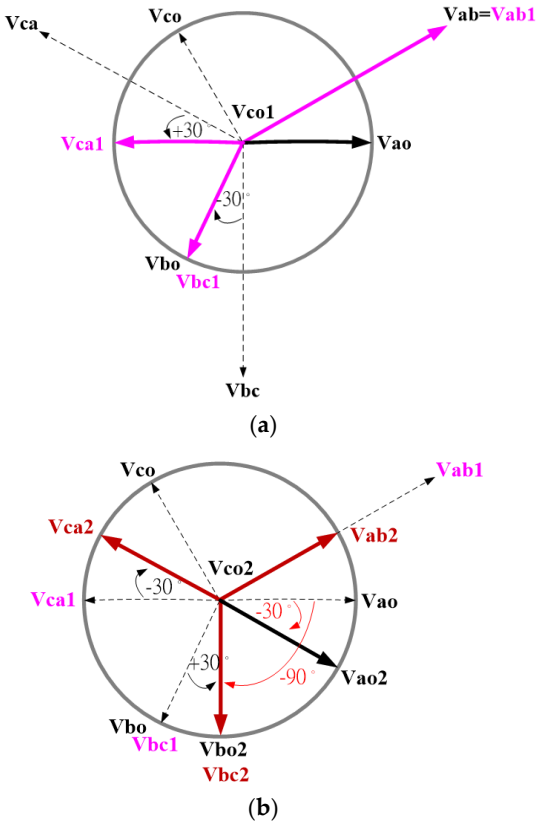


Figure 18. Voltage phasor diagram of the fault-tolerant control when a fault occurs in the switch $S_{c1}{}^{+}$ or $S_{c2}{}^{-}$; (**a**) unadjusted voltage phase angle; (**b**) adjusted phase angle of the *a*-phase voltage such that it is 30° behind that of the original phase angle of the *a*-phase voltage; adjusted phase angle of the *b*-phase voltage such that it is 150° behind the original phase angle of the *a*-phase voltage.

6.2. FTC Simulation Results

The FTC operations for the occurrence of an open-circuit fault in $S_{a1}{}^{+}$, $S_{b2}{}^{-}$, and $S_{c1}{}^{+}$ were simulated. The simulation results are illustrated in Figures 19–21. Distortion was exhibited in the three-phase output line voltage 0.06 s following the occurrence of an open-circuit fault, particularly in the faulty phase. The FTC was activated at 0.12 s. The figures show that once the FTC was activated, the five-level three-phase output line voltage was reduced to three levels and the output line voltage maintained three-phase balance after the occurrence of a fault.

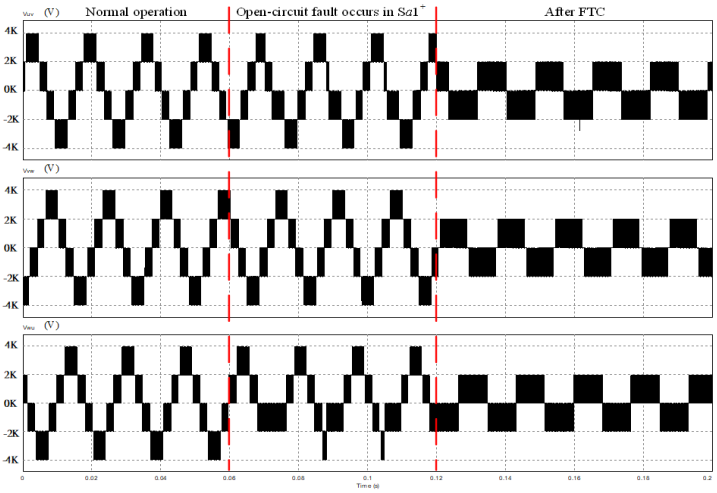


Figure 19. Output voltage with an open-circuit fault in $S_{a1}{}^{+}$ after FTC.

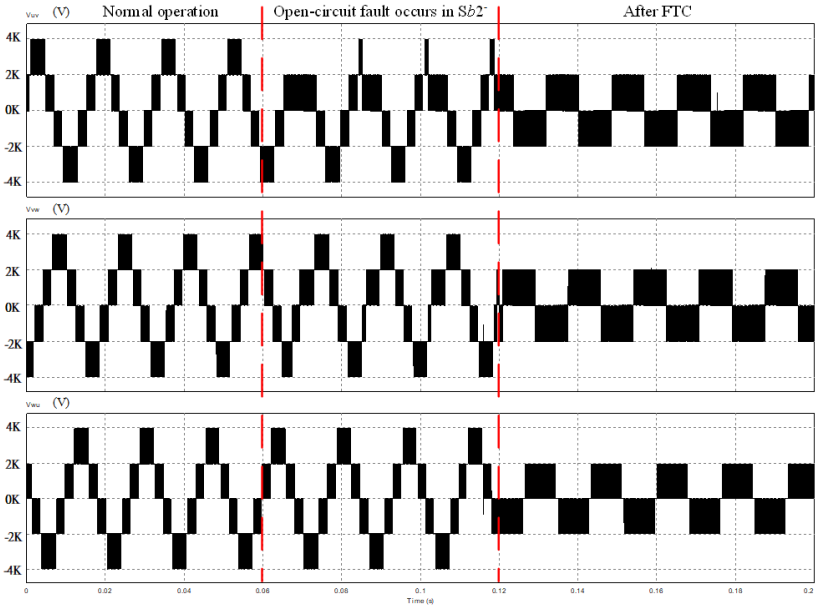


Figure 20. Output voltage with an open-circuit fault in $S_{b2}{}^{-}$ after FTC.

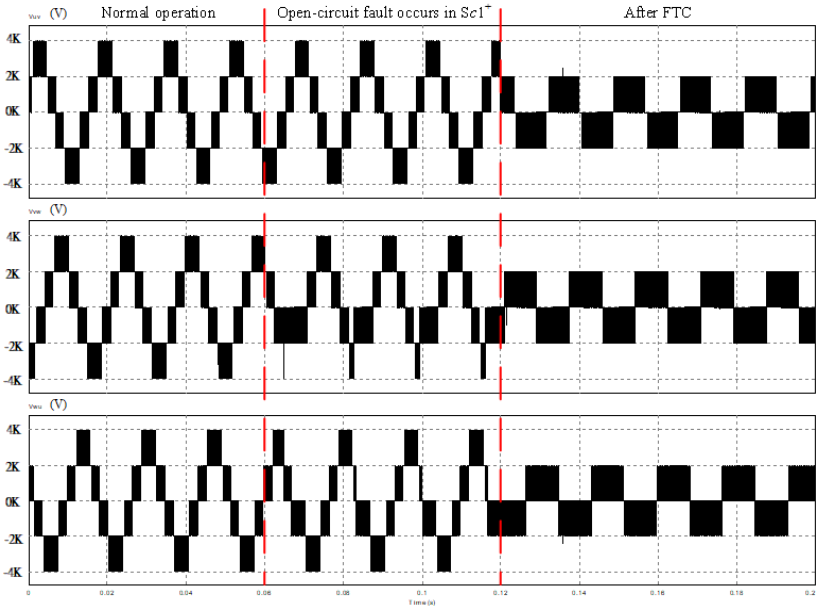


Figure 21. Output voltage with an open-circuit fault in $S_{c1}{}^{+}$ after FTC.

6.3. FTC Experimental Results

To verify the simulation results, this study uses the digital signal processor TMS320F28335 as the control core and considers the occurrence of open-circuit faults in the switches $S_{a1}{}^{+}$, $S_{b2}{}^{-}$, and $S_{c1}{}^{+}$ to test the fault-tolerant control strategy. Regarding the parameter setting of the motor drive, a 300-Vdc inverter with a switching frequency of 21 kHz is connected to an induction motor. The parameters of the induction motor are listed in Table 11.

Table 11. Parameters of the three-phase induction motor.

Horsepower (Hp)	Rotor Resistance (Ω)	Rotor Leakage Inductance (H)	Stator Resistance (Ω)	Stator Leakage Inductance (H)	Magnetization Inductance (H)	Moment of Inertia (kg-m^2)
1	10.4	0.04	11.6	0.04	0.557	0.004

Figure 22 shows that the occurrence of an open-circuit fault in the switch $S_{a1}{}^{+}$ would distort the three-phase output line voltage. The fault is particularly severe in the v_{ab} and v_{ca} phases, and the fault-tolerant control strategy can be launched 0.03 s after the occurrence of the fault. In this situation, the *a*-phase h-bridge switches ($S_{a1}{}^{+}$ and $S_{a2}{}^{-}$) are deactivated, and the neutra-point switches ($S_{a1}{}^{-}$ and $S_{a2}{}^{+}$) are thus activated. The *b* and *c*-phase switches still operate normally; the phase angle of the *b*-phase voltage is simultaneously adjusted such that it is 150° behind the phase angle of the *a*-phase reference voltage, and the phase angle of the *c*-phase reference voltage is adjusted such that it is 150° ahead of that of the *a*-phase voltage. After the execution of the fault-tolerant control strategy, the three-phase output line voltage is reduced from five to three levels (Figure 22). However, after the occurrence of the fault, the output line voltage still maintains the operation of the balanced three-phase system. Therefore, the motor can still operate normally under reduced load.

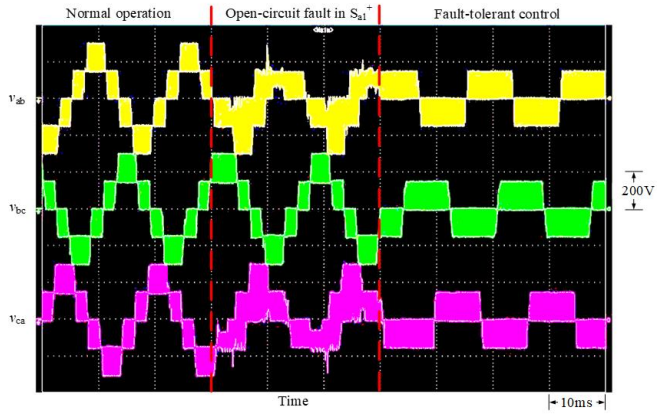


Figure 22. Measured waveform of the output voltage generated by the fault-tolerant control strategy when an open-circuit fault occurs in the switch $S_{a1}{}^{+}$.

If an open-circuit fault occurs in the switch $S_{b2}{}^{-}$, the fault would distort the three-phase output line voltage, as illustrated in Figure 23. The fault is particularly severe in the v_{ab} and v_{bc} phases. In this situation, if the fault-tolerant control strategy is launched, the *b*-phase h-bridge switches ($S_{b1}{}^{+}$ and $S_{b2}{}^{-}$) are deactivated and the neutral-point switches ($S_{b1}{}^{-}$ and $S_{b2}{}^{+}$) are thus activated; the *a*- and *c*-phase switches still operate normally. However, the phase angle of the new *a*-phase reference voltage is adjusted such that it is 30° ahead of that of the original *a*-phase reference voltage, and the phase angle of the *c*-phase reference voltage is adjusted such that it is 90° ahead of that of the original *a*-phase voltage. Figure 23 indicates that after the execution of the fault-tolerant control strategy, the three-phase output line voltage is reduced from five to three levels; however, after the occurrence of the fault, the output line voltage can maintain the operation of the balanced three-phase system. Therefore, the motor can continue to operate appropriately under reduced load.

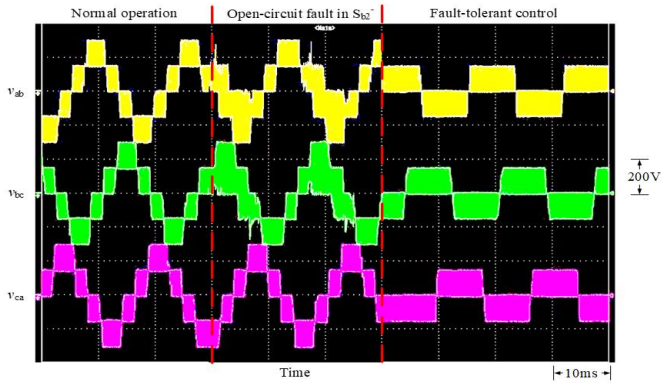


Figure 23. Measured waveform of the output voltage generated by the fault-tolerant control strategy when an open-circuit fault occurs in the switch $S_{b2}{}^{-}$.

If an open-circuit fault occurs in the switch $S_{c1}{}^{+}$, the fault would distort the three-phase output line voltage, as presented in Figure 24. The fault is particularly severe in the v_{bc} and v_{ca} phases. If the fault-tolerant control is launched 0.03 s after the occurrence of the fault, the *c*-phase h-bridge switches ($S_{c1}{}^{+}$ and $S_{c2}{}^{-}$) are deactivated and the neutral-point switches ($S_{c1}{}^{-}$ and $S_{c2}{}^{+}$) are activated; the *a*- and *b*-phase switches still operate normally. The phase angle of the *a*-phase reference voltage is adjusted such that it is 30° behind that of the original *a*-phase reference voltage, and the phase angle of the *b*-phase reference voltage is adjusted such that it is 90° behind that of the original *a*-phase reference voltage. Figure 24 reveals that after the execution of the fault-tolerant control strategy, the three-phase output line voltage is also reduced from five to three levels. However, after the occurrence of the fault, the output line voltage can maintain the operation of the balanced three-phase system. Therefore, the motor can continue to operate appropriately under reduced load.

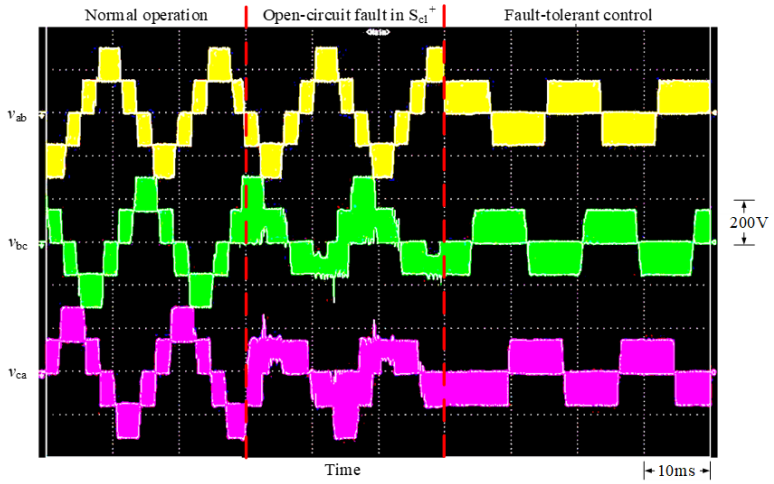


Figure 24. Measured waveform of the output voltage generated by the fault-tolerant control strategy when an open-circuit fault occurs in the switch $S_{c1}{}^{+}$.

If the capacitor at the DC link is not large enough, and the switching of FTC is not fast enough, the voltage of DC link will vary. In this paper, because the capacitor used in the DC link is quite large, and the switching time of FTC switch is very short, there is almost no voltage variation in the DC link before fault and after clearing the fault.

7. Conclusions

This paper proposed a CMAC-based fault diagnosis system for inverters capable of detecting the positions of faulty power transistors in three-level T-type inverters. The application of a CMAC reduces training time. It also possesses capabilities to reduce the effects of interference signals. The FTC strategy enabled the system to engage in FTC immediately following the occurrence of a fault to maintain the normal supply power of the inverter, thereby greatly enhancing the power reliability of three-level T-type inverters. Finally, the experimental results verify that the proposed system can accurately detect fault categories, even with the presence of interference. Moreover, the FTC strategy enables the system to maintain the three-phase balance of the output line voltage upon the occurrence of a switch fault, confirming the feasibility of the proposed system.

Author Contributions: K.-H.C. planned the project and did the writing, editing, and review. He also did the analysis and optimized the cerebellar model articulation controller. L.-Y.C. developed the three-level T-type inverter and used to create a three-level T-type inverter test environment. C.-C.H. was responsible for data curation, software and experimental corroboration for the T-type inverter and fault-tolerant controller. K.-H.C. administered the project. All authors have read and agreed to the published version of the manuscript.

Funding: The authors gratefully acknowledge the support and funding of this paper by the Ministry of Science and Technology, Taiwan, under the Grant Number MOST 109-2221-E-167-016-MY2.

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Rodriguez, J.I.; Leeb, S.B. A Multilevel inverter topology for inductively coupled power transfer. *IEEE Trans. Power Electron.* **2006**, *21*, 1607–1617. [CrossRef]
2. Escalante, M.F.; Vannier, J.C.; Arzande, A. Flying capacitor multilevel inverters and DTC motor drive applications. *IEEE Trans. Ind. Electron.* **2002**, *49*, 809–815. [CrossRef]
3. Tourkhani, F.; Viarouge, P.; Meynard, T.A. Optimal design and experimental results of a multilevel inverter for an UPS application. In Proceedings of the Second International Conference on Power Electronics and Drive Systems, Singapore, 26–29 May 1997; pp. 340–343.
4. Daher, S.; Schmid, J.; Antunes, F.L.M. Multilevel inverter topologies for stand-alone PV systems. *IEEE Trans. Ind. Electron.* **2008**, *55*, 2703–2712. [CrossRef]
5. Naik, R.L.; Udaya, K.R.Y. A novel technique for control of cascaded multilevel inverter for photovoltaic power supplies. In Proceedings of the 2005 European Conference on Power Electronics and Applications, Dresden, Germany, 11–14 September 2005; pp. 1–9.
6. Nabae, A.; Takahashi, I.; Akagi, H. A new neutral-point clamped PWM inverter. *IEEE Trans. Ind. Appl.* **1981**, *17*, 518–523. [CrossRef]
7. Schweizer, M.; Kolar, J.W. Design and implementation of a highly efficient three-level T-type converter for low-voltage applications. *IEEE Trans. Power Electron.* **2013**, *28*, 899–907. [CrossRef]
8. Chen, A.; Hu, L.; Chen, L.; Deng, Y.; Yao, G.; He, X. A multilevel converter topology with fault-tolerant ability. *IEEE Trans. Power Electron.* **2005**, *20*, 405–415. [CrossRef]
9. Khomfoi, S.; Tolbert, L.M. Fault diagnostic system for a multilevel inverter using a neural network. *IEEE Trans. Power Electron.* **2007**, *22*, 1062–1069. [CrossRef]
10. Choi, U.; Lee, K.; Blaabjerg, F. Diagnosis and tolerant strategy of an open-switch fault for T-type three-level inverter systems. *IEEE Trans. Ind. Appl.* **2014**, *50*, 495–508. [CrossRef]
11. Chao, A.M. Motor Fault Diagnosis by Using Fuzzy Neural Network. Master's Thesis, Chung Yuan Christian University, Taoyuan, Taiwan, 2004.
12. Ahmadi, S.; Poure, P.; Saadate, S.; Khaburi, D.A. Fault tolerance analysis of five-level neutral-point-clamped inverters under clamping diode open-circuit failure. *Electronics* **2022**, *11*, 1461. [CrossRef]
13. Chao, K.H.; Ke, C.H. Fault diagnosis and tolerant control of three-level neutral-point clamped inverters in motor drives. *Energies* **2020**, *13*, 6302. [CrossRef]
14. Han, T.; Yang, B.S.; Lee, J.M. A new condition monitoring and fault diagnosis system of induction motors using artificial intelligence algorithms. In Proceedings of the IEEE International Conference on Electrical Machines and Drives, San Antonio, TX, USA, 15 May 2005; pp. 1967–1974.
15. Chen, T.; Pan, Y.; Xiong, Z. A hybrid system model-based open-circuit fault diagnosis method of three-phase voltage-source inverters for PMSM drive systems. *Electronics* **2020**, *9*, 1251. [CrossRef]
16. Lehtoranta, J.; Koivo, H.N. Fault diagnosis of induction motors with dynamical neural networks. In Proceedings of the IEEE International Conference on System, Man and Cybernetics, Waikoloa, HI, USA, 12 October 2005; pp. 2979–2984.
17. He, Q.; Du, D.M. Fault diagnosis of induction motor using neural networks. In Proceedings of the International Conference on Machine Learning and Cybernetics, Hong Kong, China, 19–22 August 2007; pp. 1090–1095.
18. Murphey, Y.L.; Masrur, M.A.; Chen, Z.H.; Zhang, B. Model-based fault diagnosis in electric drives using machine learning. *IEEE/ASME Trans. Mechatron.* **2006**, *11*, 290–303. [CrossRef]
19. Zidani, F.; Benbouzid, M.E.H.; Diallo, D.; Nait-Said, M.S. Induction motor stator faults diagnosis by a current concordia pattern based fuzzy decision system. *IEEE Trans. Energy Convers.* **2003**, *18*, 469–475. [CrossRef]
20. Nejjari, H.; Benbouzid, M.E.H. Monitoring and diagnosis of induction motors electrical faults using a current Park's vector pattern learning approach. *IEEE Trans. Ind. Appl.* **2000**, *36*, 730–735. [CrossRef]
21. Diallo, D.; Benbouzid, M.E.H.; Hamad, D.; Pierre, X. Fault detection and diagnosis in an induction machine drive: A pattern recognition approach based on concordia stator mean current vector. *IEEE Trans. Energy. Convers.* **2005**, *20*, 512–519. [CrossRef]
22. Zidani, F.; Diallo, D.; Benbouzid, M.E.H.; Nait-Said, R. A Fuzzy-based approach for the diagnosis of fault modes in a voltage-fed PWM inverter induction motor drive. *IEEE Trans. Ind. Electron.* **2008**, *55*, 586–593. [CrossRef]
23. Zhang, K.; Jiang, B.; Staroswiecki, M. Dynamic output feedback fault tolerant controller design for Takagi-Sugeno fuzzy systems with actuator faults. *IEEE Trans. Fuzzy Syst.* **2010**, *18*, 194–201. [CrossRef]
24. Awadallah, M.A.; Morcos, M.M. Diagnosis of switch open-circuit fault in PM brushless DC motor drives. In Proceedings of the Power Engineering Conference on Large Engineering System, Montreal, QC, Canada, 7–9 May 2003; pp. 69–73.
25. Albus, J.S. A new approach to manipulator control: The cerebellar model articulation controller. *Trans. ASME J. Dynam. Syst. Meas. Contr.* **1975**, *97*, 220–227. [CrossRef]

26. Hung, C.P.; Chao, K.H. CMAC neural network application on lead-acid batteries residual capacity estimation. In Proceedings of the 3th International Conference on Intelligent Computing, Qingdao, China, 21–24 August 2007; pp. 961–970.
27. Handeiman, D.A.; Lane, S.H.; Gelfand, J.J. Integrating neural networks and knowledge-based systems for intelligent robotic control. *IEEE Contr. Syst. Mag.* **1990**, *10*, 77–87. [CrossRef]