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Influence of Substrate and Gate Insulator on the Thermal Characteristics of β-Ga_2O_3 Field-Effect Transistors: A Simulation Study

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Abstract: β-Ga_2O_3 suffers from extremely poor thermal conductivity, resulting in a severe self-heating effect. Integrating β-Ga_2O_3 with high-thermal-conductivity foreign substrates is one of the promising solutions to improve the thermal performance of β-Ga_2O_3 devices. However, the gate insulator also plays an important role in the device's thermal characteristics. In this work, we analyze the influence of the thermal conductivity of the substrate and gate insulator and the associated thermal boundary conductance (TBC) on the channel peak temperature (T_{MAX}) investigated by the coupled 3-D thermal simulation. It reveals that AlN and SiC substrate could be sufficient compared to the expensive diamond substrate for substrate integration thermal management scheme. And the reduced T_{MAX} becomes more prominent with the high thermal conductivity gate insulator (e.g., *h*-BN) than with the conventional Al_2O_3 gate insulator. Furthermore, the T_{MAX} of the device maintains a very high temperature as the TBC is very low (10 $MWm^{-2}K^{-1}$), indicating the importance of optimizing TBC. Our results provide useful insights into the thermal management of β-Ga_2O_3 devices.

Keywords: β-Ga_2O_3; thermal management; device simulation

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1. Introduction

Beta-gallium oxide (β-Ga_2O_3) is a promising candidate for power and RF devices in the future due to its attractive properties, such as an ultra-wide bandgap of 4.8 eV and a high theoretical electrical breakdown field of 8 MV/cm [1]. The electrical breakdown field of 3.8 MV/cm has been achieved [2], which surpasses the theoretical maximum of GaN and SiC. In addition, β-Ga_2O_3 has big advantages in terms of low cost and mass production using melt growth techniques.

Recently, β-Ga_2O_3-based field-effect transistors (FETs) have been extensively studied. Mun et al. fabricated lateral β-Ga_2O_3 metal-oxide-semiconductor field-effect transistors (MOSFETs) with the source-connected field plate. They realized a high breakdown voltage of over 2 kV for the first time [3]. Tadjer et al. prepared β-Ga_2O_3 MOSFETs with a high-*k* HfO_2 gate insulator, and a positive threshold voltage for a Ga_2O_3-based transistor was displayed [4]. Further, Xia et al. developed a δ-doped β-Ga_2O_3 FET with the cutoff frequency of 27 GHz, where a maximum transconductance of 44 mS/mm and a maximum current density of 0.26 A/mm was also obtained [5]. However, the thermal conductivity of β-Ga_2O_3 (10–30 $Wm^{-1}K^{-1}$) is significantly lower than that of GaN (230 $Wm^{-1}K^{-1}$) and 4H-SiC (490 $Wm^{-1}K^{-1}$). The heat generated in the β-Ga_2O_3 channel cannot be removed effectively. Thus, the channel temperature rises, and the carrier mobility decreases, eventually leading to the degradation of device performance or even device failure. To mitigate the self-heating effect, various foreign substrates with high thermal conductivity have been examined using experimental and simulation approaches. The β-Ga_2O_3-based devices on AlN [6], SiC [7], and diamond [8] substrates all exhibit better thermal characteristics. Meanwhile, Chatterjee et al. used electro-thermal simulation to propose that the flip-chip heterointegration can effectively improve both the steady-state and transient thermal properties of Ga_2O_3 devices [9]. Yuan et al. also showed that double-side cooling combined with a heat spreader employed in the active region of the device could reduce the device's thermal resistance [10]. However, most studies have focused on substrates and heat spreaders rather than gate insulators.

In this work, a 2-D electro-thermal model of β-Ga_2O_3 MOSFETs was constructed using commercial Silvaco TCAD software. The simulation models were verified using the experimental data. Then a 3-D thermal model with the Joule heat power map extracted from the 2-D simulation was created in the commercial COMSOL software to simulate the exact temperature distribution. Based on the above models, the effect of the thermal conductivity of the substrate and gate insulator and the associated thermal boundary conductance (TBC) on the channel peak temperature (T_{MAX}) were investigated.

2. Simulation Setup

A typical β-Ga_2O_3 MOSFET structure, as schematically shown in Figure 1, was used for 2-D simulation in this work. In this device, the thickness of the β-Ga_2O_3 channel and its doping concentration was chosen to be 100 nm and 2.0×10^{18} cm^{-3}, respectively. The thickness of Al_2O_3 was set to 20 nm. The gate length, the source and drain contacts length, the source to gate distance, and the drain to gate distance were 0.8 μm, 1 μm, 0.7 μm, and 1 μm, respectively.

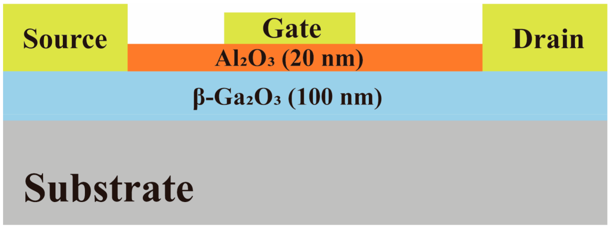

Figure 1. Cross-sectional schematic diagram of the simulated β-Ga_2O_3 MOSFET.

The 2-D simulation was performed by the Silvaco TCAD with the drift-diffusion transport model. The default low field mobility model in Blaze and the high field negative differential mobility model [11] were considered for β-Ga_2O_3. The substrate was used as a heat sink. The temperature-dependent thermal conductivity of Al_2O_3 was referred from the literature [12], and the thermal conductivity of AlN and Si was calculated by ATLAS using the Boltzmann transport equation. For β-Ga_2O_3, the key parameters in the simulation are summarized in Table 1. In the simulation, the bottom of the substrate was set to ambient temperature, while the rest of the boundaries were adiabatic boundaries.

Table 1. β-Ga_2O_3 simulation parameters.

Parameter	Value
Bandgap (eV)	4.8
Relative dielectric constant	10
Electron effective mass	0.28 m_0
Electron affinity (eV)	4.0
Conduction band density (cm^{-3})	3.6×10^{18}
Valence band density (cm^{-3})	2.86×10^{20}
Saturated electron velocity (cm/s)	1.0×10^{7}
Thermal conductivity	Anisotropy [13]

Then, a coupled 3-D finite element thermal simulation was adopted to predict the device temperature profile more accurately. Figure 2 presents the 3-D thermal model of the simulated β-Ga_2O_3 MOSFET. The Joule heat power map was extracted from the 2-D simulation and imported into the 3-D model as a heat source. The substrate thickness and channel width were 500 µm and 1 µm, respectively. The gate electrode, source, and drain electrodes were Ni/Au (20/100 nm) and Ti/Al/Ni/Au (20/100/60/80 nm), respectively. The size of the electrode pad was 10 × 10 μm^2. The rest of the parameters were consistent with the 2-D simulation. Similar to the 2-D simulation, the bottom of the substrate was also set to ambient temperature. At the same time, the rest of the boundaries were set to natural convection with the convection coefficient of 5 $Wm^{-2}K^{-1}$.

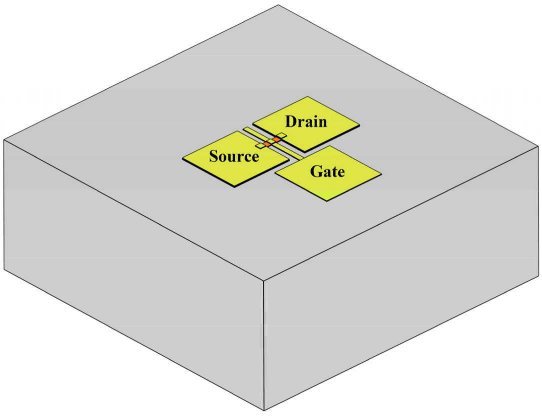

Figure 2. 3-D thermal model of the simulated β-Ga_2O_3 MOSFET. (not drawn to scale).

For lateral transistor devices, the heat generated in the channel is mainly dissipated through the device surface and the substrate. Figure 3 offers a simple model of heat transport in our simulated device, where the red rectangle is the regions of heat generation and the red arrows represent the heat transport paths. In the vertical direction, the heat transport can be described by a 1-D model, which considers Joule heat generation, dissipation, and diffusion, as given by [14].

$$d^2\Delta T(x)/dx^2 - a(x)^2\Delta T(x) = -bJ^2 \quad (1)$$

$$\Delta T(x) = T(x) - T_0$$

where T_0 is ambient temperature, J is the current density, and $b = 1/\kappa\sigma$, where κ is the thermal conductivity and σ is the electrical conductivity. $a(x)$ is a dissipation factor, which includes the effect of gate insulator and substrate.

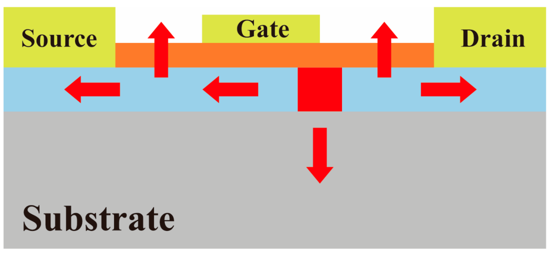

Figure 3. Heat transport model of the simulated β-Ga_2O_3 MOSFET.

Therefore, we investigated the effect of the relevant device parameters on T_{MAX}, including substrate thermal conductivity (K_{Sub}), gate insulator thermal conductivity, the thermal boundary conductance between the β-Ga_2O_3 channel and the substrate (TBC-Sub), and the thermal boundary conductance between the β-Ga_2O_3 channel and the gate insulator (TBC-Gate). The feasible range of the above parameters is summarized in Table 2.

Table 2. Feasible range of parameters in the 3-D thermal simulation.

Parameter	Range
K_{Sub} ($Wm^{-1}K^{-1}$)	10–3000
Gate Insulator Thermal Conductivity	Al_2O_3 or *h*-BN
TBC-Sub ($MWm^{-2}K^{-1}$)	10–300
TBC-Gate (($MWm^{-2}K^{-1}$))	10–300

3. Results and Discussion

First, we adjusted the electron mobility and interface charges in the simulation for calibration against the experimental data [6]. The substrate is set to AlN/Si (230 nm/10 µm). Figure 4 presents a comparison between experimental and simulated output performance. A good agreement is substantially obtained for the drain current density.

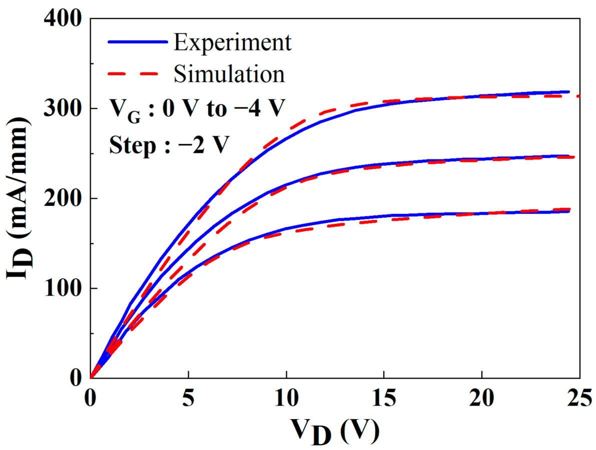

Figure 4. The experimental and simulated output performance of the β-Ga_2O_3 MOSFET.

Figure 5 shows the simulated Joule heat power map in the device at the gate-to-source bias of 0 V and drain-to-source bias of 25 V. It is seen that most of the heat is generated at the edge of the gate on the drain side. For simplicity, only the Joule heat power distribution in the white dashed box in the figure is considered with the cross-sectional area of 1.0×0.1 µm^2. The location and size of the heat source are assumed to be independent of dissipated power density.

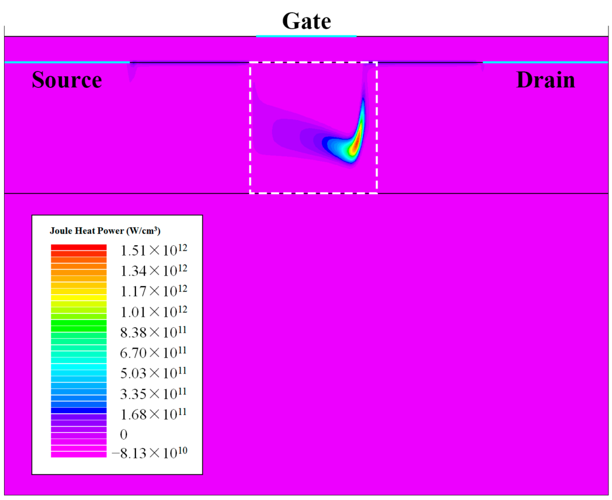

Figure 5. Joule heat power profile in the device at the gate-to-source bias of 0 V and drain-to-source bias of 25 V.

Figure 6 plots T_{MAX} as a function of K_{Sub} at a power density of 10 W/mm when both the TBC-Sub and TBC-Gate are kept at 10 $MWm^{-2}K^{-1}$. The Al_2O_3 and *h*-BN are selected as typical representatives of the gate insulator. The thermal conductivity of *h*-BN is greater than that of Al_2O_3 [15], which is about 100 $Wm^{-1}K^{-1}$. The thermal conductivity of common substrate materials is also marked in the figure. The figure shows that T_{MAX} decreases with the increase of K_{Sub} for both Al_2O_3 and *h*-BN, but the decrease is negligible when K_{Sub} exceeds 300 $Wm^{-1}K^{-1}$. When K_{Sub} increases from 300 $Wm^{-1}K^{-1}$ to 2000 $Wm^{-1}K^{-1}$, T_{MAX} decreases by only about 3 K. The above results show that for substrate integration thermal management scheme, AlN and SiC substrate could be sufficient compared to the expensive diamond substrate.

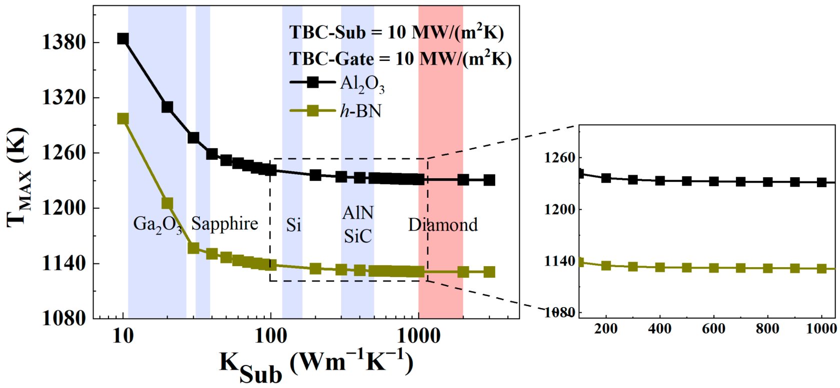

Figure 6. The dependence of T_{MAX} on K_{Sub} as both the TBC-Sub and TBC-Gate are kept at 10 $MWm^{-2}K^{-1}$.

It is observed from Figure 6 that the β-Ga_2O_3 device based on the diamond substrate (2000 $Wm^{-1}K^{-1}$) still suffers from an unacceptable T_{MAX} of over 1100 K, indicating the importance of optimizing the thermal boundary conductance. Figure 7a,b depicts the effect of TBC-Sub and TBC-Gate on T_{MAX} for different substrate thermal conductivities (10 $Wm^{-1}K^{-1}$ and 2000 $Wm^{-1}K^{-1}$) for the gate insulator of Al_2O_3 and *h*-BN, respectively. T_{MAX} reduces with increasing TBC-Sub or TBC-Gate when K_{Sub} is a constant. However, TBC-Gate has significantly less impact on T_{MAX} due to the small thermal conductivity of the Al_2O_3 gate insulator. At K_{Sub} of 2000 $Wm^{-1}K^{-1}$, T_{MAX} reduces by 54% when TBC-Sub increases from 10 $MWm^{-2}K^{-1}$ to 100 $MWm^{-2}K^{-1}$. And T_{MAX} reduces by only 28% when TBC-Gate increases from 10 $MWm^{-2}K^{-1}$ to 100 $MWm^{-2}K^{-1}$. While for the *h*-BN gate insulator, T_{MAX} reduces by 51% when TBC-Sub increases from 10 $MWm^{-2}K^{-1}$ to 100 $MWm^{-2}K^{-1}$. And T_{MAX} reduces by 37% when TBC-Gate increases from 10 $MWm^{-2}K^{-1}$ to 100 $MWm^{-2}K^{-1}$. The *h*-BN shows better heat dissipation capability due to its higher thermal conductivity. The comparison of the effect of TBC-Gate on T_{MAX} for different gate insulators is further depicted in Figure 8.

Finally, the effect of TBC-Gate on T_{MAX} was analyzed for different TBC-Sub. Figure 9a,b show T_{MAX} versus TBC-Gate for TBC-Sub of 50 $MWm^{-2}K^{-1}$, 100 $MWm^{-2}K^{-1}$, and 300 $MWm^{-2}K^{-1}$ for the gate insulator of Al_2O_3 and *h*-BN, respectively. Obviously, with the high thermal conductivity gate insulator of *h*-BN, the T_{MAX} reduction is more prominent. Currently, the measured TBC of the Ga_2O_3-diamond interfaces is about 179 $MWm^{-2}K^{-1}$ [16]. For the gate insulator of Al_2O_3, when K_{Sub} and TBC-Gate are 2000 $W/m^{-1}K^{-1}$ and 100 $MWm^{-2}K^{-1}$, the T_{MAX} is 478 K. While for the *h*-BN gate insulator, the T_{MAX} is 458 K, which is below the safe operation of 200 °C [9]. It is believed that with further interface engineering and higher thermal conductivity gate insulator, substrate integration can provide good thermal management for β-Ga_2O_3 devices.

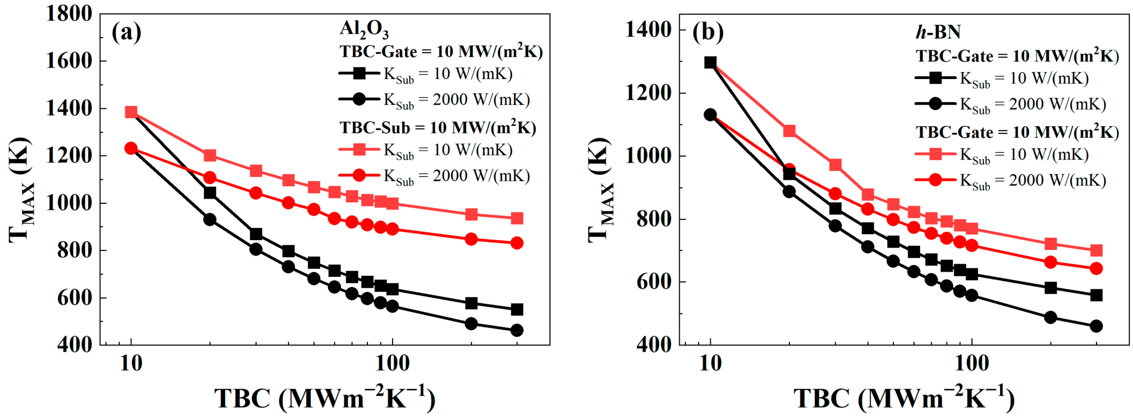

Figure 7. The dependence of T_{MAX} on TBC-Sub and TBC-Gate for different substrate thermal conductivities as the gate insulators are (**a**) Al_2O_3 and (**b**) h-BN.

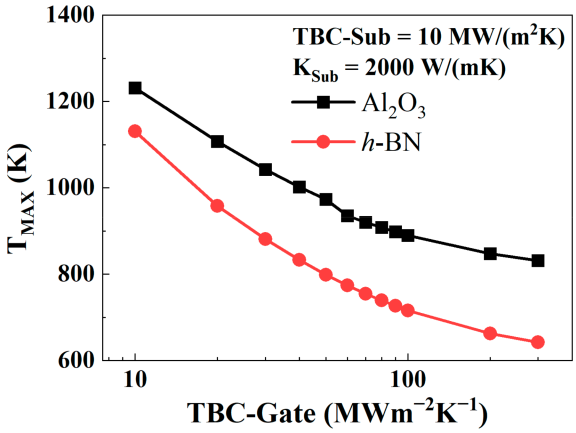

Figure 8. The dependence of T_{MAX} on TBC-Gate for different gate insulators.

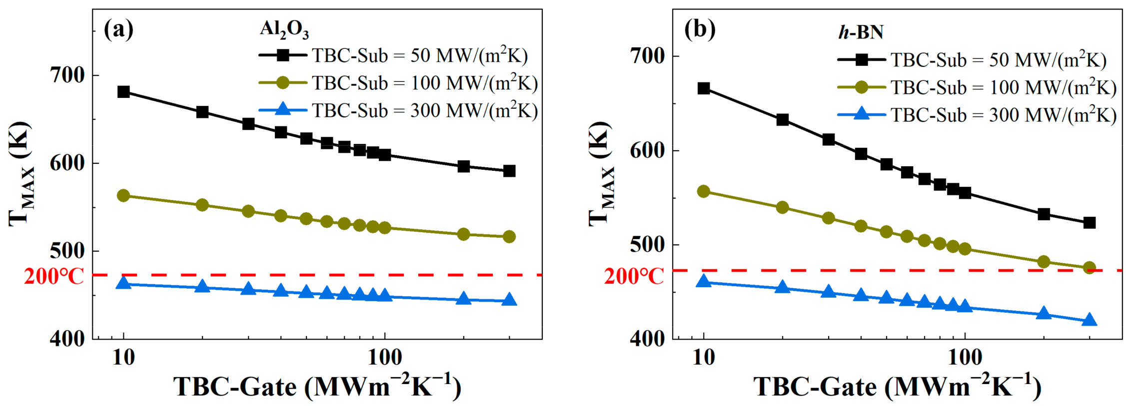

Figure 9. T_{MAX} versus TBC-Gate for TBC-Sub of 50 $MWm^{-2}K^{-1}$, 100 $MWm^{-2}K^{-1}$, and 300 $MWm^{-2}K^{-1}$ as the gate insulators are (**a**) Al_2O_3 and (**b**) *h*-BN.

4. Conclusions

In summary, we studied substrate integration thermal management schemes for β-Ga_2O_3 devices using the coupled 3-D thermal simulation. The results indicate that AlN and SiC substrates may be sufficient compared to the expensive diamond substrate. And compared to the conventional Al_2O_3 gate insulator, the reduced T_{MAX} becomes more prominent using the high thermal conductivity gate insulator (e.g., *h*-BN). Furthermore, the associated TBC also plays an important role in the device's thermal characteristics. The T_{MAX} of the device exceeds 1100 K under a targeted power density of 10 W/mm when the TBC is very low (10 $MWm^{-2}K^{-1}$), indicating the importance of optimizing TBC. Overall, our results provide useful insights into the thermal management of β-Ga_2O_3 devices.

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