electronics

Article

Analysis of a Resonant Converter with Wide Input Voltage

Bor-Ren Lin [1,*], Alexis Phaik Imm Goh [2] and Kai-Wei Wang [1]

1 Department of Electrical Engineering, National Yunlin University of Science and Technology, Yunlin 640, Taiwan; qwe8262878@gmail.com
2 College of Future, National Yunlin University of Science and Technology, Yunlin 640, Taiwan; alexisg@yuntech.edu.tw
* Correspondence: linbr@yuntech.edu.tw

Abstract: A DC-DC converter with a 16:1 ($V_{in,max}$ = 16$V_{in,min}$) wide input voltage operation is presented for auxiliary power supplies on solar power conversion circuits or railway vehicles. The solar cell output voltage is associated with the solar intensity (day or night) and geographical location. Thus, the wide input voltage capability of DC converters is required for photovoltaic power conversion. For low power supplies on railway vehicles, the nominal input voltages are 24 V~110 V for the electric door system, motor drive, solid state lighting systems and braking systems. The presented converter uses buck/boost and resonant circuits to achieve the wide input voltage range operation from 18 V to 288 V. If V_{in} stays on a low input voltage range (18 V~72 V), the buck/boost circuit is operated at a voltage boost characteristic. On the other hand, the buck/boost circuit is operated at a voltage buck characteristic when the input voltage climbs to a high voltage range (72 V~288 V). Thus, the buck/boost circuit can output a constant voltage. Then, the resonant circuit in the second stage is worked at a constant input voltage case so that the frequency variation range is reduced. Finally, to investigate the performance and effectiveness of the studied circuit, experiments with a 500 W prototype were conducted to investigate the performance of the studied circuit.

Keywords: buck/boost converter; resonant converter; wide input voltage variation

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Citation: Lin, B.-R.; Goh, A.P.I.; Wang, K.-W. Analysis of a Resonant Converter with Wide Input Voltage. *Electronics* **2021**, *10*, 1110. https://doi.org/10.3390/electronics10091110

Academic Editor: Khaled Ahmed

Received: 24 April 2021
Accepted: 4 May 2021
Published: 8 May 2021

1. Introduction

Wide voltage range DC-DC converters have been discussed and presented for solar cell power conversion due to the variable output voltage of the photovoltaic panel. The output voltage of a photovoltaic panel depends on the solar intensity of the day and night. Therefore, DC converters with a wide voltage range are developed for solar power conversion and the self-supplying power units are developed for remote control systems. Wide voltage DC-DC converters are also needed on a railway vehicle due to many different nominal DC voltages (24 V~110 V) that are requested for the communication system, lighting system, electric door system and braking system. Thus, pulse-width modulation (PWM) converters with a wide voltage operation are welcomed and demanded on railway power supply units. Multi-stage converters [1,2] have been proposed to actualize the wide voltage capability operation. The buck or boost circuit topology is selected on the front-stage to achieve a buck or boost operation. The flyback, forward or half-bridge circuit topology with pulse-width modulation is adopted on the rear-stage to regulate output voltage. However, these solutions have high switching losses on power devices and the input voltage range is still limited at $V_{in,max} \leq 4V_{in,min}$ or $V_{in,max} \leq 6V_{in,min}$. Series-parallel connection DC converters have been discussed in [3–5]. Unfortunately, the circuit structure is too complicated and more expensive for use in low or medium power supplies. Single-stage DC converters with a PWM operation were discussed in [6–12] to extend the input voltage range. However, the input voltage range in [6–12] is still limited at $V_{in,max} \leq 4V_{in,min}$. In [13], the thermal constraints issue has been discussed for a current-mode monolithic DC-DC converter.

In this paper, we present and investigate a DC-DC converter that has a 16:1 (V_{in} = 288 V~18 V) wide voltage operation and soft switching turn-on operation. To realize a 16:1 wide voltage operation, a buck/boost DC-DC circuit is utilized in the first stage to accomplish either a voltage boost action if the V_{in} is on a low input voltage range ($V_{in,min} < V_{in} < 4V_{in,min}$) or a voltage buck action if the V_{in} is on a high input voltage range ($4V_{in,min} < V_{in} < 16V_{in,min}$). Therefore, the output terminal voltage of the buck/boost converter is controlled at a constant value. An *LLC* converter is used in the rear-stage to control the output voltage while accomplishing zero voltage switching (ZVS) for active devices. Since the input voltage of the *LLC* converter is almost constant due to the buck/boost converter regulation, the variation in switching frequency is limited to a narrow frequency range. Compared to conventional DC-DC converters and multi-stage converters, the main contributions in this paper are (1) the wide voltage range action, (2) the soft switching operation in the second stage circuit, and (3) the simple control scheme. The converter characteristics are confirmed by the experiments using a prototype circuit.

2. Circuit Structure

Figure 1 provides the circuit schematic of the presented PWM converter with the function of a 16:1 voltage range operation for PV panel power converters or the auxiliary power on railway vehicles. The presented circuit is a two-stage DC converter. The front-stage is a buck/boost circuit and the rear-stage is an *LLC* converter. The components of a buck/boost circuit include Q_1, D_1, L_f, Q_2, D_2 and C_{dc}. The *LLC* converter includes L_r, S_1, S_2, T, C_r, D_{o1}, D_{o2} and C_o. The buck/boost circuit can achieve a wide input voltage range operation. When $V_{in} < V_{dc}$, the buck/boost circuit is operated at a voltage boost. On the other hand, the buck/boost circuit is worked at a buck operation if $V_{in} > V_{dc}$. The *LLC* resonant circuit in the rear-stage is operated at a constant input voltage V_{dc} condition. Therefore, the switching frequency of a resonant circuit can be designed at a series resonant frequency to lessen the magnetizing current losses, while, at the same time, having ZVS characteristics for switches S_1 and S_2 and diodes D_{o1} and D_{o2}. According to the input voltage range, the presented converter can be operated at two voltage ranges ($V_{in,min}$~$4V_{in,min}$) and ($4V_{in,min}$~$16V_{in,min}$). When V_{in} is greater than $V_{in,min}$ and less than $4V_{in,min}$, the switch Q_1 is on, diode D_1 is on the reverse biased and Q_2 is controlled with pulse-width modulation. Thus, the buck/boost circuit is worked like a boost converter to achieve a voltage step-up characteristic, as shown in Figure 2a. The DC bus voltage V_{dc} is controlled at the reference voltage $V_{dc,ref}$ and the *LLC* resonant circuit is controlled at a constant input voltage case. When $4V_{in,min} < V_{in} < 16V_{in,min}$, switch Q_2 is off and switch Q_1 is controlled with a pulse-width modulation scheme to control the DC bus voltage $V_{dc} = V_{dc,ref}$. Thus, the buck/boost converter is working as a buck converter to achieve a voltage step-down characteristic, as shown in Figure 2b. According to the adopted control algorithm, the studied converter has a 16:1 ($V_{in,max} = 16V_{in,min}$) voltage range operation for a solar PV panel power conversion and a railway vehicle with low power supplies and applications.

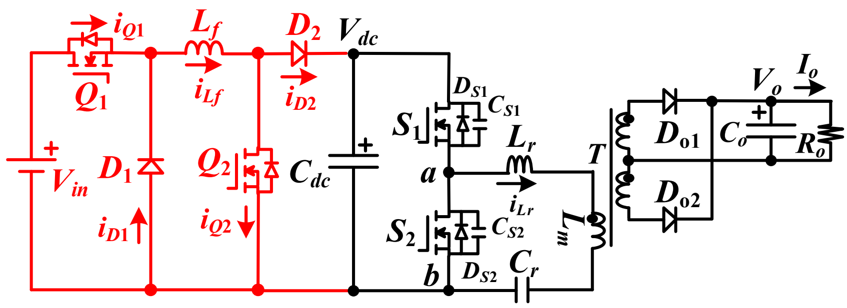

Figure 1. The circuit diagram of the presented converter with 16:1 ($V_{in,max} = 16V_{in,min}$) voltage range operation.

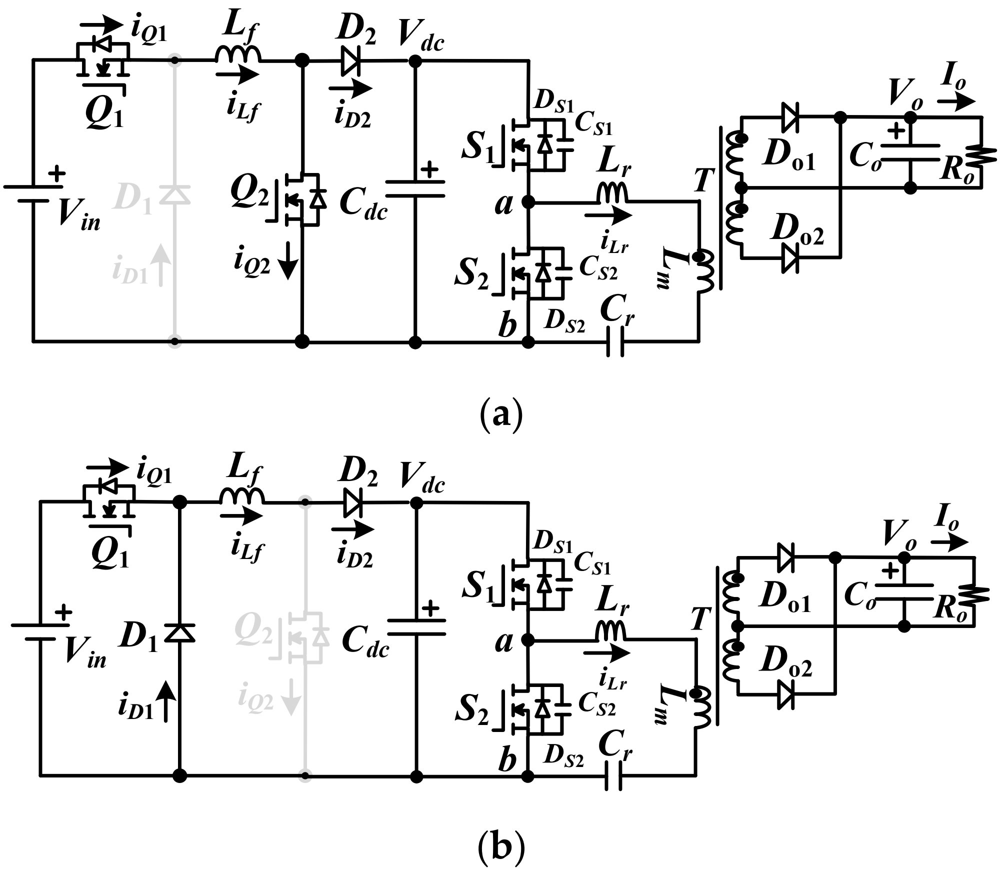

Figure 2. Equivalent circuits for (**a**) low input voltage operation (**b**) high input voltage operation.

3. Operation Principle

The studied converter is a two-stage circuit. The front-stage is a buck/boost converter to achieve either a voltage boost action if V_{in} is on a low input voltage range or a voltage buck action if V_{in} is on a high input voltage range. The buck/boost converter is regulated by a pulse-width modulation. The second stage is an *LLC* resonant converter to accomplish both electric isolation and a ZVS turn-on operation for active devices.

3.1. Circuit Operation of the Buck/Boost Converter

The buck/boost converter can work at a voltage boost operation or buck operation. To accomplish a wide voltage operation, the DC bus voltage of the buck/boost converter is controlled at $V_{dc} = 4V_{in,min}$. When $V_{in,min} \leq V_{in} < 4V_{in,min}$, the buck/boost converter operates at a boost operation (Figure 2a)and Q_1 is on, diode D_1 is off and Q_2 is controlled by a pulse-width modulation to have a voltage boost action. Figure 3a gives the PWM signals of the buck/boost converter for a voltage step-up action. Under a continuous conduction mode operation, two circuit modes are observed (Figure 3b,c). Based on a voltage-second balance on the inductor L_f, the DC bus voltage V_{dc} is obtained as $d_{Q1}V_{in}/(1 - d_{Q2}) = V_{in}/(1 - d_{Q2})$ where d_{Q1} and d_{Q2} are duty cycles of Q_1 and Q_2, respectively, and $d_{Q1} = 1$ under the boost operation.

Mode 1 [t_0~$t_0 + d_{Q2}T_{sw}$]: At $t = t_0$, Q_2 is activated to turn on. Since Q_1 is always on and D_1 is reverse biased for the voltage boost operation, the voltage across on L_f can be obtained as $v_{Lf} = V_{in}$ and v_{D2} is $-V_{DC}$. The inductor current i_{Lf} increases and the diode D_2 is reverse biased. Capacitor C_{dc} is discharged to supply current i_{dc} to the secondstage resonant converter.

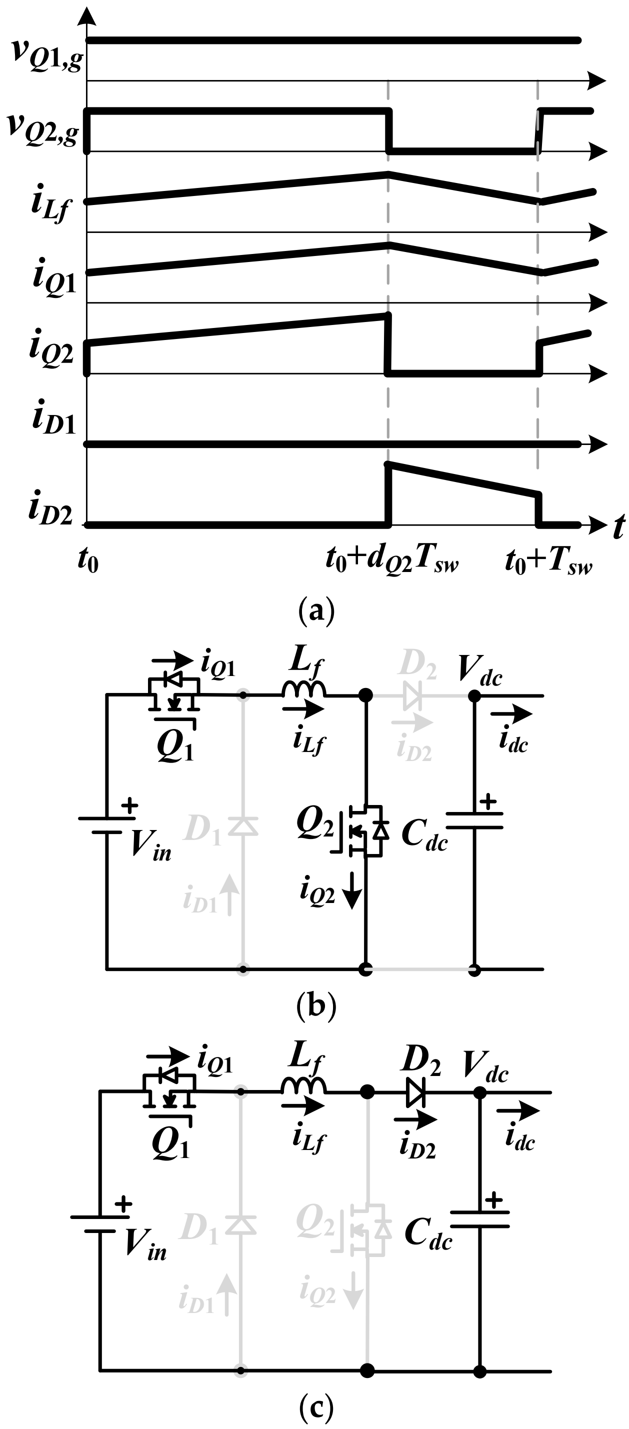

Figure 3. Buck/boost converter under low voltage range (boost operation) (**a**) pulse-width modulation (PWM) signals (**b**) mode 1 equivalent circuit (**c**) mode 2 equivalent circuit.

Mode 2 [$t_0 + d_{Q2}T_{sw}$~$t_0 + T_{sw}$]: At $t = t_0 + d_{Q2}T_{sw}$, Q_2 is turned off. The inductor i_{Lf} flows through D_2 to charge C_{dc}. The inductor voltage $v_{Lf} = V_{in} - V_{dc} < 0$ so that i_{Lf} decreases. The drain-to-source voltage of Q_2 is equal to the DC bus voltage V_{dc}. Mode 2 is ended at time $t_0 + T_{sw}$.

When $4V_{in,min} < V_{in} \leq 16V_{in,min}$, the buck/boost converter operates as a voltage step-down operation (Figure 2b). The switch Q_2 is controlled at an off state, diode D_2 is always conducting and Q_1 is activated by pulse-width modulation to accomplish a voltage step-down. The pulse-width modulation waveforms of the voltage step-down operation are given in Figure 4a and two circuit modes are shown in Figure 4b,c under a continuous conduction mode. Based on a flux balance on inductor L_f, the DC bus voltage V_{dc} is calculated as $d_{Q1}V_{in}/(1 - d_{Q2}) = d_{Q1}V_{in}$ where $d_{Q2} = 0$ under the buck operation.

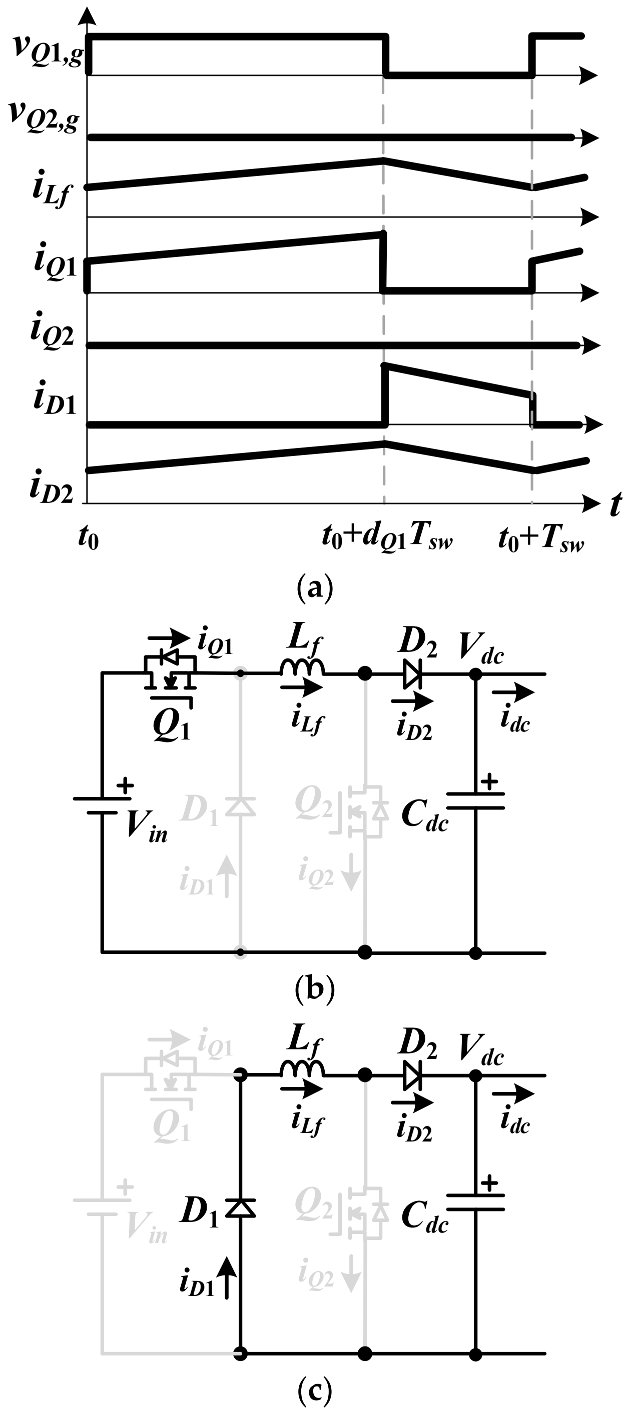

Figure 4. Buck/boost converter under high voltage range (buck operation) (**a**) PWM signals (**b**) mode 1 equivalent circuit (**c**) mode 2 equivalent circuit.

Mode 1 [t_0~$t_0 + d_{Q1}T_{sw}$]: At time t_0, Q_1 turns on. Since Q_2 is always off and D_2 is forward biased for the voltage step-down operation, the inductor voltage $v_{Lf} = V_{in} - V_{dc} > 0$ and v_{D1} is $-V_{in}$. In this mode, i_{Lf} increases, the D_1 is reverse biased and C_{dc} is charged.

Mode 2 [$t_0 + d_{Q1}T_{sw}$~$t_0 + T_{sw}$]: At time $t_0 + d_{Q1}T_{sw}$, Q_1 turns off. In mode 2, $v_{Lf} = -V_{dc}$, i_{Lf} decreases, $v_{Q1,ds} = V_{in}$, $v_{Q2,ds} = V_{dc}$ and C_{dc} is discharged. This mode ends at time $t_0 + T_{sw}$.

3.2. Circuit Operation of the LLC Resonant Circuit

Since the DC bus voltage V_{dc} is a constant voltage due to the buck/boost circuit operation, the *LLC* resonant converter is operated under almost constant voltage V_{dc}. Thus, the switching frequency of the *LLC* resonant circuit is controlled at a limited narrow frequency range. The converter voltage gain is calculated as G_{LLC} = $2nV_o/V_{dc}$ = $2nV_o$ $(1 - d_{Q2})/d_{Q1}V_{in}$. Figure 5a gives the main circuit waveforms of the resonant converter and Figure 5b–g shows the six mode operations.

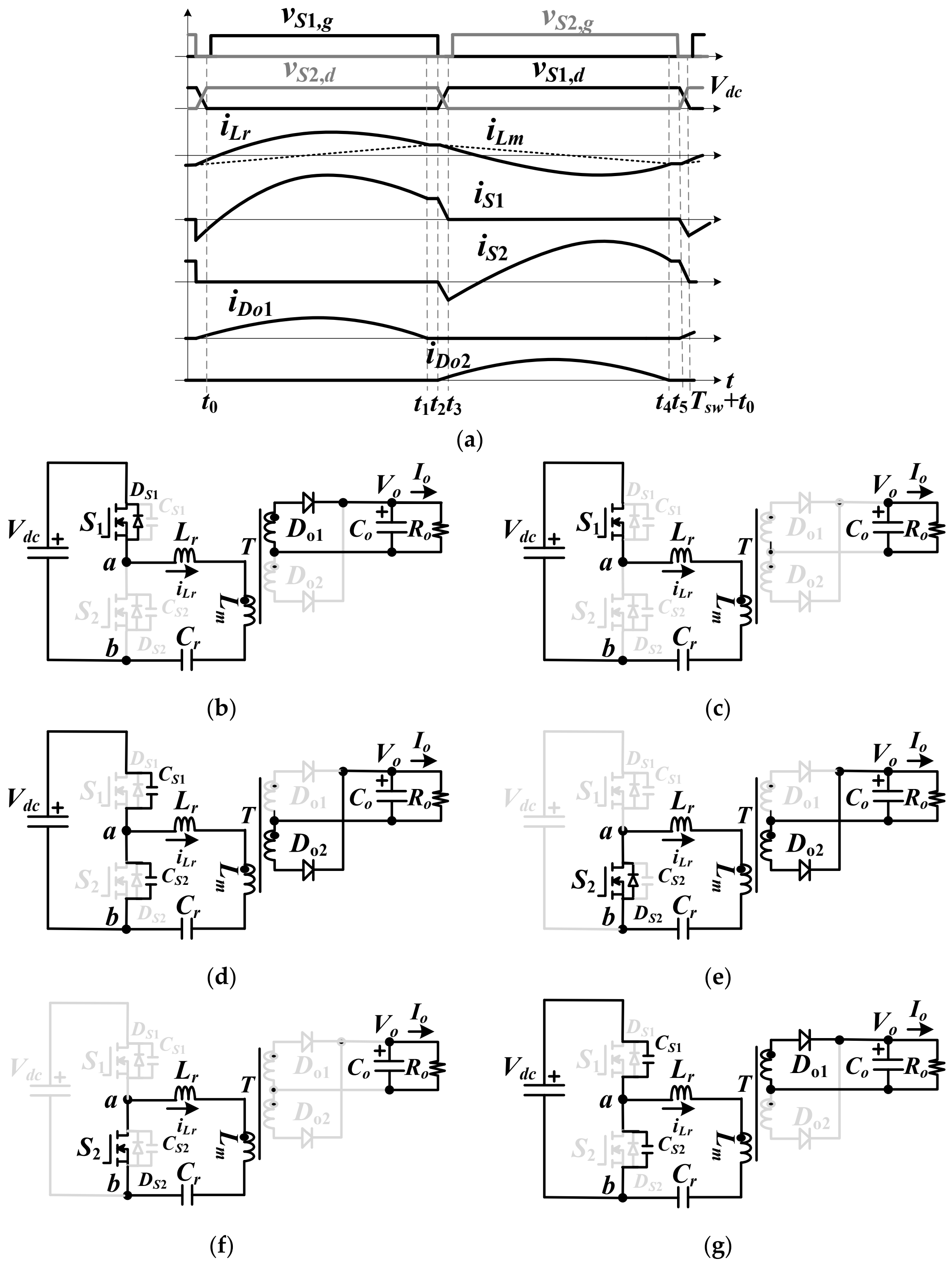

Figure 5. Circuit operations of resonant converter (**a**) PWM signals (**b**) mode 1 equivalent circuit (**c**) mode 2 equivalent circuit (**d**) mode 3 equivalent circuit (**e**) mode 4 equivalent circuit (**f**) mode 5 equivalent circuit (**g**) mode 6 equivalent circuit.

Mode 1 [t_0~t_1]: At time $t < t_0$, the active device S_1 is off, v_{CS1} is positive and i_{Lr} is negative. At time t_0, $v_{CS1} = 0$ and D_{S1} is conducting. After time t_0, S_1 can turn on at the ZVS action. Since D_{o1} is conducting, $v_{Lm} = nV_o$. Power is delivered to a load side through the components S_1, L_r, T, C_r and D_{o1}. L_r and C_r are naturally resonant, with frequency $f_r = 1/2\pi\sqrt{L_rC_r}$. If f_r is greater than the switching frequency f_{sw}, then the circuit proceeds to mode 2, or it goes to mode 3.

Mode 2 [t_1~t_2]: Since $f_r > f_{sw}$, i_{Do1} will decrease to 0 at t_1. D_{o1} is off. i_{Lr} will flow through S_1, L_m, L_r and C_r. Together with L_r and L_m, C_r is naturally resonant, with frequency $f_m = 1/2\pi\sqrt{(L_m + L_r)C_r}$ and $f_m < f_r$.

Mode 3 [t_2~t_3]: Active device S_1 is turned off at time t_2 under zero voltage. After time t_2, $i_{Lr} > 0$ and $i_{Lr} < i_{Lm}$. Thus, C_{S2} (C_{S1}) discharges (charges) and the secondary diode D_{o2} conducts.

Mode 4 [t_3~t_4]: At time t_3, C_{S2} is discharged to zero and D_{S2} is conducting due to $i_{Lr}(t_3) > 0$. After t_3, S_2 turns on under zero voltage. D_{o2} is forward biased on the secondary side, $v_{Lm} = -nV_o$. Energy stored on C_r is transferred to the output load. L_r and C_r are naturally resonant, with frequency f_r.

Mode 5 [t_4~t_5]: If $f_{sw} < f_r$, then i_{D2} will decrease to 0 at t_4. D_{o2} is reverse biased. No power is delivered to the output load. L_r, L_m and C_r are naturally resonant, with frequency f_m.

Mode 6 [t_5~$T_{sw} + t_0$]: S_2 turns off at time t_5. C_{S1} (C_{S2}) discharges (charges) and D_{o1} conducts because the $i_{Lr}(t_5) < 0$ and $i_{Lr}(t_5) > i_{Lm}(t_5)$. Mode 6 ends at time $T_{sw} + t_0$.

4. Circuit Characteristics

The buck/boost converter is operated by a 16:1 wide voltage range operation. The output voltage V_{dc} of the buck/boost converter is controlled at $V_{dc,ref} = 4V_{in,min}$. If V_{in} is on a low voltage range ($V_{in} < V_{dc,ref} = 4V_{in,min}$), then the converter is operated at the boost operation. As a result, Q_1 stays on, Q_2 is operated by a duty cycle control and D_1 is reverse biased. When V_{in} is on a high input voltage range ($V_{in} > V_{dc,ref} = 4V_{in,min}$), the converter is operated at a buck operation. As a result, Q_2 stays off and Q_1 is operated by pulse-width modulation. Thus, the *LLC* resonant circuit is operated at a constant input voltage of $V_{dc} = 4V_{in,min}$. The buck/boost converter is controlled at a continuous conduction mode. For the boost operation, $V_{Lf} = V_{in}$ (or $V_{in} - V_o$) if Q_2 is on (or off) as shown in Figure 3. For the buck operation, $V_{Lf} = V_{in} - V_o$ (or $-V_o$) if Q_1 is on (or off) as shown in Figure 4. For a continuous conduction mode, the DC bus voltage V_{dc} is calculated as:

$$V_{dc} = \begin{cases} V_{in}/(1 - d_{Q2}), & V_{in} < V_{dc,ref} = 4V_{in,min} \\ d_{Q1}V_{in}, & V_{in} > V_{dc,ref} = 4V_{in,min} \end{cases} \tag{1}$$

where d_{Q1} and d_{Q2} are duty cycles of Q_1 and Q_2, respectively. V_{in} is greater than $V_{in,min}$ and less than $4V_{in,min}$ on the low voltage range. Therefore, the maximum and minimum duty cycles of Q_2 are expressed as:

$$d_{Q2,max} = (V_{dc,ref} - V_{in,min})/V_{dc,ref} \tag{2}$$

$$d_{Q2,min} = (V_{dc,ref} - 4V_{in,min})/V_{dc,ref} \tag{3}$$

In the same manner, the maximum and minimum duty cycles of Q_1 are expressed as (4) and (5) on the high input voltage range ($4V_{in,min} < V_{in} < 16V_{in,min}$).

$$d_{Q1,max} = V_{dc,ref}/4V_{in,min} \tag{4}$$

$$d_{Q1,min} = V_{dc,ref}/16V_{in,min} \tag{5}$$

If the DC bus current and d_{Q1} and d_{Q2} are given, then the root mean square (*rms*) currents $I_{Q1,rms}$ and $I_{Q2,rms}$ are obtained in (6) and (7).

$$I_{Q1,rms} = \begin{cases} I_{dc}/(1-d_{Q2}), & V_{in} < V_{dc,ref} = 4V_{in,min} \\ \sqrt{d_{Q1}}I_{dc}, & V_{in} > V_{dc,ref} = 4V_{in,min} \end{cases} \quad (6)$$

$$I_{Q2,rms} = \begin{cases} I_{dc}\sqrt{d_{Q2}}/(1-d_{Q2}), & V_{in} < V_{dc,ref} = 4V_{in,min} \\ 0, & V_{in} > V_{dc,ref} = 4V_{in,min} \end{cases} \quad (7)$$

From the on/off states of Q_1, Q_2, D_1 and D_2, the voltage ratings of Q_1 and Q_2 are $V_{in,max}$ and V_{dc}, respectively. The average currents I_{D1} and I_{D2} are obtained in (8) and (9).

$$I_{D1} = \begin{cases} 0, & V_{in} < V_{dc,ref} = 4V_{in,min} \\ (1-d_{Q1})I_{dc}, & V_{in} > V_{dc,ref} = 4V_{in,min} \end{cases} \quad (8)$$

$$I_{D2} = I_{dc} \quad (9)$$

$V_{in,max}$ and V_{dc} are the voltage ratings of D_1 and D_2 respectively. Based on the boost or buck operation, the *rms* inductor current is calculated as:

$$I_{Lf,rms} = \begin{cases} I_{dc}/(1-d_{Q2}), & V_{in} < V_{dc,ref} = 4V_{in,min} \\ I_{dc}, & V_{in} > V_{dc,ref} = 4V_{in,min} \end{cases} \quad (10)$$

The half-bridge resonant circuit is controlled with pulse frequency modulation. Since S_1 and S_2 have a 50% duty cycle, a square wave voltage waveform with 0 and V_{dc} is generated on voltage v_{ab}. The *rms* value of v_{ab} approximates $V_{ab,rms} = \sqrt{2}V_{dc}/\pi$. According to the conducting states of D_{o1} and D_{o2}, a square voltage waveform is generated on the magnetizing voltage v_{Lm} and $V_{Lm,rms} = 2\sqrt{2}nV_o/\pi$. The fundamental primary-side resistance is calculated as $R_{ac} = 8n^2R_o/\pi^2$, where R_o is the DC load resistance. Since the resonant tank (L_m, C_r, L_r and R_{ac}) is adopted in the rear-stage, in (11) the voltage transfer function of the resonant tank is obtained.

$$\begin{aligned} |G_{LLC}| &= \frac{V_{Lm,rms}}{V_{ab,rms}} = \left|\frac{R_{ac}//j2\pi f_{sw}L_m}{j2\pi f_{sw}L_r + (j2\pi f_{sw}C_r)^{-1} + R_{ac}//j2\pi f_{sw}L_m}\right| \\ &= \frac{1}{\sqrt{\left[1+\frac{1}{L_B}\frac{f_n^2-1}{f_n^2}\right]^2 + Q^2\left[\frac{f_n^2-1}{f_n}\right]^2}} = \frac{2nV_o}{V_{dc}} \end{aligned} \quad (11)$$

where $L_B = L_m/L_r$, $Q = \sqrt{L_r/C_r}/R_{ac}$ and $f_n = f_{sw}/f_r$. Since the DC bus voltage V_{dc} is regulated at $V_{dc,ref}$ by the front-stage buck/boost circuit, the switching frequency f_{sw} depends on I_o or R_o. The *LLC* resonant circuit is controlled at an inductive load. Therefore, active devices of the resonant circuit are operated using a soft switching operation.

5. Experimental Results

The studied circuit is tested and investigated to show the performance of the prototype circuit. The prototype is designed under the following specifications: V_{in} = 288 V~18 V (16:1 ratio), V_o = 12 V, $P_{o,rated}$ = 500 W and f_r = 60 kHz. When V_{in} = 18 V~65 V, the buck/boost converter is controlled at boost operation. The voltage V_{dc} is maintained at 72 V. If the input voltage V_{in} = 76 V~288 V, then the buck/boost converter is operated at a buck operation and the DC bus voltage V_{dc} = 72 V. However, no voltage step-up or step-down is operated on the buck/boost converter when 65 V < V_{in} < 76 V. Q_1 (Q_2) is on (off) under this condition and V_{dc} = V_{in}. Therefore, the resonant circuit is designed under the input of a DC bus voltage V_{dc} = 65 V~76 V. Two Schmitt voltage comparators are used to detect the three input voltage ranges 18 V~65 V, 65 V~76 V and 76 V~288 V. If V_{in} is on a low voltage range

(18 V~65 V), Q_2 is controlled by a duty cycle scheme to achieve a boost operation. The duty cycle of Q_2 is calculated in (12) and (13) under continuous conduction mode.

$$d_{Q2,min} = \frac{V_{dc,ref} - V_{in,high}}{V_{dc,ref}} = \frac{72 - 65}{72} \approx 0.1 \tag{12}$$

$$d_{Q2,max} = \frac{V_{dc,ref} - V_{in,low}}{V_{DC,ref}} = \frac{72 - 18}{72} \approx 0.75 \tag{13}$$

For a high input voltage range of 76 V~288 V, Q_1 is controlled by a duty cycle scheme to achieve a buck operation. The duty cycle of Q_1 is given in (14) and (15) under continuous conduction mode.

$$d_{Q1,min} = \frac{V_{dc,ref}}{V_{in,high}} = \frac{72}{288} \approx 0.25 \tag{14}$$

$$d_{Q1,max} = \frac{V_{dc,ref}}{V_{in,low}} = \frac{72}{76} \approx 0.95 \tag{15}$$

It is assumed that the ripple current Δi_{Lf} is 5% of the maximum input current at 18 V of input voltage. Therefore, inductance L_f is given in (16).

$$L_f = \frac{V_{in,min} d_{Q2,max}}{\Delta i_{Lf} f_{sw}} = \frac{18 \times 0.75}{0.04 \times (500/18) \times 60 \times 10^3} \approx 203 \mu\text{H} \tag{16}$$

The *rms* switch currents $I_{Q1,rms}$ and the $I_{Q2,rms}$ are expressed in (17) and (18).

$$I_{Q1,rms} = \begin{cases} \frac{I_{dc}}{1-d_{Q2,max}} = \frac{500/72}{1-0.75} \approx 28\text{A}, \ 18\text{V} < V_{in} < 65\text{V} \\ \sqrt{d_{Q1,max}} I_{dc} = \sqrt{0.95} \frac{500}{72} \approx 6.8\text{A}, \ 76\text{V} < V_{in} < 288\text{V} \end{cases} \tag{17}$$

$$I_{Q2,rms} = \begin{cases} \frac{I_{dc}\sqrt{d_{Q2,max}}}{1-d_{Q2,max}} = \frac{\frac{500}{72}\sqrt{0.75}}{1-0.75} \approx 24, 18\text{V} < V_{in} < 65\text{V} \\ 0, \ 76\text{V} < V_{in} < 288\text{V} \end{cases} \tag{18}$$

The voltage ratings of Q_1 and Q_2 are $V_{in,max}$ = 288 V and $V_{dc,max}$ = 76 V. Switch Q_1 used two MOSFETs STB35N60DM2 (STMicroelectronics, Geneva, Switzerland) with 600 V/28 A ratings, while switch Q_2 adopted MOSFET IRFB4110PbF (Infineon Technologies, Neubiberg, Germany) with 100 V/120 A ratings. The average diode currents of D_1 and D_2 are obtained in (19) and (20).

$$I_{D1} = \begin{cases} 0, & 18\text{V} < V_{in} < 65\text{V} \\ (1 - d_{Q1,min}) I_{dc} \approx 5.2\text{A}, & 76\text{V} < V_{in} < 288\text{V} \end{cases} \tag{19}$$

$$I_{D2} = I_{dc} = 500/72 \approx 7\text{A} \tag{20}$$

D_1 has a voltage stress of $V_{in,max}$ = 288 V and D_2 has a voltage stress of $V_{dc,\max}$ = 76 V. SF1006G (TSMC, Hsinchu, Taiwan) and STPS20SM100S (STMicroelectronics, Geneva, Switzerland) with 400 V/10 A and 100 V/20 A ratings are used for diodes D_1 and D_2, respectively.

For the *LLC* resonant circuit design, the necessary resonant frequency and inductor ratio are selected as f_r = 60 kHz and L_B = 8. The minimum, nominal and maximum DC bus voltages are 65 V, 72 V and 76 V, respectively. The nominal voltage gain of G_{nom} at $V_{dc,nom}$ = 72 V is designed at unity. Therefore, the turn-ratio n of the transformer is calculated as follows.

$$n = \frac{G_{LLC,nom} V_{dc,nom}}{2V_o} = \frac{1 \times 72}{2 \times 12} \approx 3 \tag{21}$$

The TDK EER42 with n_s = 4 and n_p = 12 is used for the transformer T. Thus, the voltage gains $G_{LLC,max}$ and $G_{LLC,min}$ at V_{dc} = 65 V and 76 V are calculated in (22) and (23).

$$G_{LLC,max} = \frac{2nV_o}{V_{dc,min}} = \frac{2 \times 3 \times 12}{65} \approx 1.1 \tag{22}$$

$$G_{LLC,min} = \frac{2nV_o}{V_{dc,max}} = \frac{2 \times 3 \times 12}{76} \approx 0.95 \tag{23}$$

For full rated power, the fundamental primary-side resistance R_{ac} is obtained in (24).

$$R_{ac} = \frac{8n^2 R_o}{\pi^2} = \frac{8 \times 3^2 \times (12^2/500)}{\pi^2} \approx 2.1\Omega \tag{24}$$

The selected quality factor Q is 0.7. From the given Q, R_{ac} and f_r, the resonant inductance L_r is obtained as:

$$L_r = \frac{QR_{ac}}{2\pi f_r} = \frac{0.7 \times 2.1}{2\pi \times 60000} \approx 3.9\mu\text{H} \tag{25}$$

due to L_B = 8, $L_m = L_B \times L_r$ = 31.2 µH. C_r can be calculated as:

$$C_r = \frac{1}{4\pi^2 L_r f_r^2} = \frac{1}{4\pi^2 \times 3.9 \times 10^{-6} \times (60000)^2} \approx 1.8\mu\text{F} \tag{26}$$

The voltage ratings of S_1 and S_2 equal $V_{dc,max}$ = 76 V and the voltage rating of diodes D_{o1} and D_{o2} equals $2V_o$ = 24 V. Power switches IPP111N15N3 (150 V/83 A) are adopted for active devices S_1 and S_2 and S60SC6M (60 V/60 A) (Shindengen Electric Manufacturing, Tokyo, Japan) switches are selected for D_{o1} and D_{o2}. The selected C_{dc} = 680 µF and C_o = 1000 µF. UC3843 (Texas Instruments, Dallas, TX, USA) is selected to regulate the buck/boost circuit while the UCC25600 (Texas Instruments, Dallas, TX, USA) is adopted to regulate the *LLC* resonant circuit.

Figure 6 illustrates the experiments of the presented converter at V_{in} = 18 V and the rated power. Since V_{in} = 18 V < V_{dc} = 72 V, the buck/boost converter is operated at a boost operation. Therefore, Q_1 is on and Q_2 is controlled by the duty cycle modulation. Figure 6a shows the experimental waveforms of $v_{Q2,g}$, i_{Lf}, i_{Q2} and i_{D2}. When Q_2 is on or off, the i_{Lf} equals i_{Q2} or i_{D2}. Figure 6b provides the test results of the input voltage V_{in}, dc bus voltage V_{dc}, the gate voltage $v_{Q2,g}$ and leg voltage v_{ab}. The duty cycle of Q_2 equals 0.75, $V_{dc} > V_{in}$ (boost operation) and the leg voltage v_{ab} is a square voltage. Figure 6c gives the primary-side experimental waveforms of the *LLC* resonant circuit at full load. As the switching frequency is close to the resonant frequency, v_{Cr} and i_{Lr} are sinusoidal waveforms and v_{ab} is a square waveform. Since the half-bridge *LLC* is controlled in the second stage, the v_{Cr} contains a DC voltage value ($v_{Cr,dc} = V_{dc}/2$). Figure 6d provides the secondary side currents and load voltage at full load. The output voltage is regulated at 12 V and the load current I_o = 42 A. No serious reverse recovery current is observed on the rectifier diodes D_{o1} and D_{o2}. In the same manner, Figure 7 illustrates the experiments at V_{in} = 65 V and the rated power conditions. Since V_{in} = 65 V < V_{dc} = 72 V, the duty cycle of Q_2 is calculated as 0.1. The measured waveforms $v_{Q2,g}$, i_{Lf}, i_{Q2} and i_{D2} are shown in Figure 7a. The experimental waveforms V_{in}, V_{dc}, $v_{Q2,g}$ and v_{ab} are illustrated in Figure 7b. The experimental waveforms of the resonant converter are provided in Figure 7c,d. Since V_{dc} = 72 V by the buck/boost converter for both V_{in} = 18 V and 65 V, it can be seen that the measured waveforms of the resonant converter under V_{in} = 18 V (Figure 6c,d) and V_{in} = 65 V (Figure 7c,d) are identical. Figures 8 and 9 show the experiments of the proposed circuit for V_{in} = 76 V and 288 V input on the high input voltage range and rated power. When the input voltage ranges between 76 V and 288 V, the buck/boost circuit is controlled at a buck operation and Q_2 is off. The duty cycle of Q_1 equals 0.95 (0.25) at V_{in} = 76 V (288 V). The measured waveforms of $v_{Q1,g}$, i_{Lf}, i_{Q1} and i_{D1} at V_{in} = 76 V and 288 V are illustrated in Figures 8a and 9a. The buck/boost converter is operated at a buck operation and V_{dc} is controlled at 72 V for both V_{in} = 76 V and V_{in} = 288 V. The experiments of the resonant converter for a 76 V (288 V) input are shown in Figure 8c,d (Figure 9c,d). When 65 V < V_{in} < 76 V, Q_1 is on and Q_2 is off. No voltage step-up or step-down is realized on the buck/boost converter so that the DC bus voltage V_{dc} = V_{in}. Under this condition, only the resonant converter is worked to regulate the load voltage. Figures 10 and 11 provide the measured waveforms of the resonant circuit at 67 V and 74 V input and the rated power. When V_{dc} = 67 V, the resonant converter needs more voltage gain compared to V_{dc} = 72 V and $f_{sw} < f_r$. Thus, i_{Lr} likes a quasi-sinusoidal signal in Figure 10a and D_{o1} and D_{o2} are turned off at zero current switching in Figure 10b. In the same manner, the switching frequency at V_{dc} = 74 V shown in Figure 11 is greater than the resonant frequency in order to achieve a lower voltage gain. Figure 12 illustrates the experiments of S_1 at V_{in} = 18 V, 67 V, 74 V and 288 V. Figure 12a,b shows the experimental waveforms of S_1 under 20% load and full load at V_{in} = 18 V condition. In the same manner, Figure 12c,d gives the measured results of S_1 at 67 V input. Figure 12e,f provides the test results of S_1 at 74 V input. Likewise, Figure 12g,h shows the experimental waveforms of S_1 at 288 V input (high input voltage range). From the test results in Figure 12, it can be seen that S_1 turns on at ZVS from a 20% load for all input voltage ranges and turns off at hard switching. Since switch S_2 possesses the same switching characteristics as S_1, it can be expected that S_2 also turns on under zero voltage from a 20% load and turns off at hard switching.

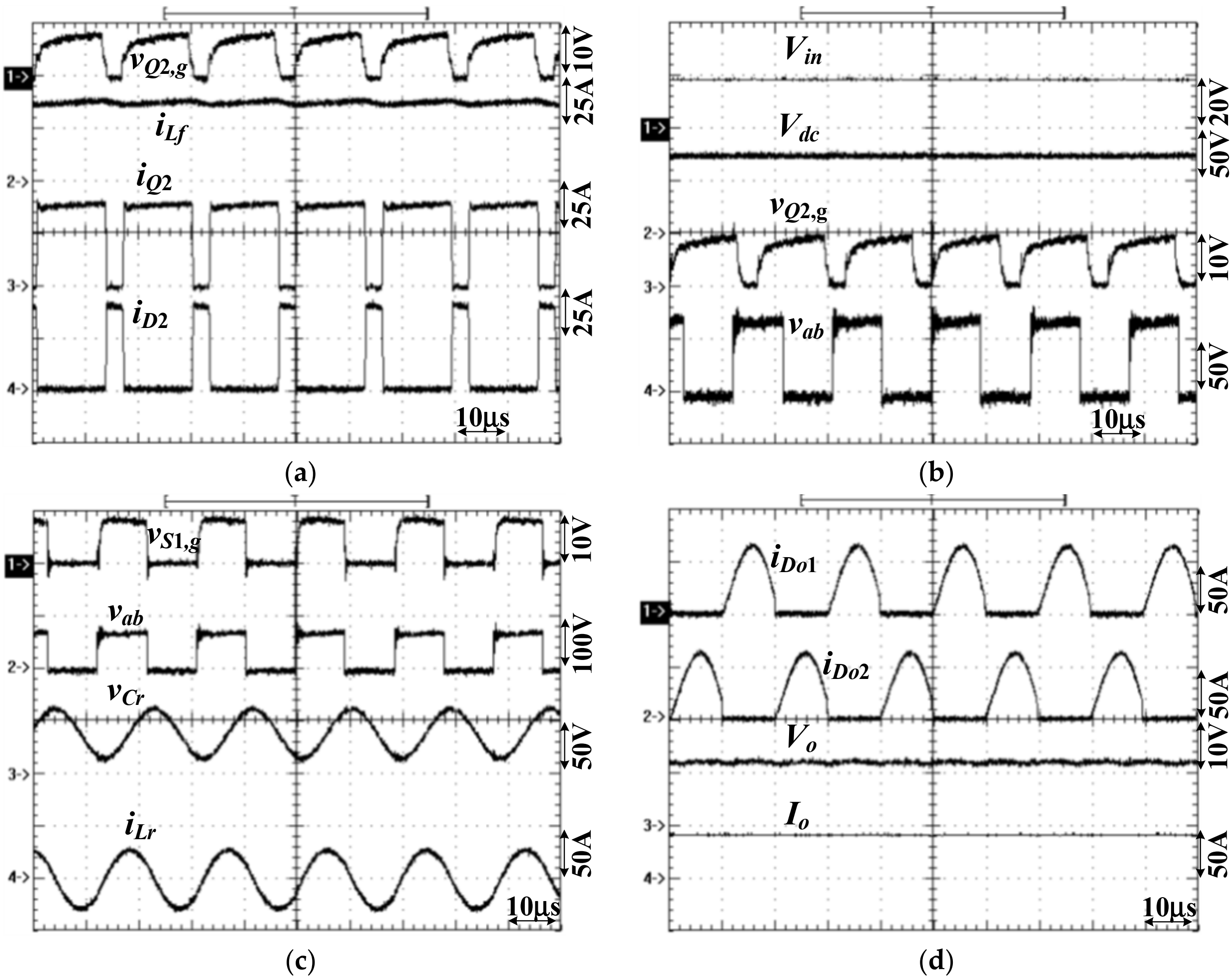

Figure 6. Measured results at V_{in} = 18 V and P_o = 500 W (**a**) $v_{Q2,g}$, i_{Lf}, i_{Q2} and i_{D2} (**b**) V_{in}, V_{dc}, $v_{Q2,g}$ and v_{ab} (**c**) $v_{S1,g}$, v_{ab}, v_{Cr} and i_{Lr} (**d**) i_{Do1}, i_{Do2}, V_o and I_o.

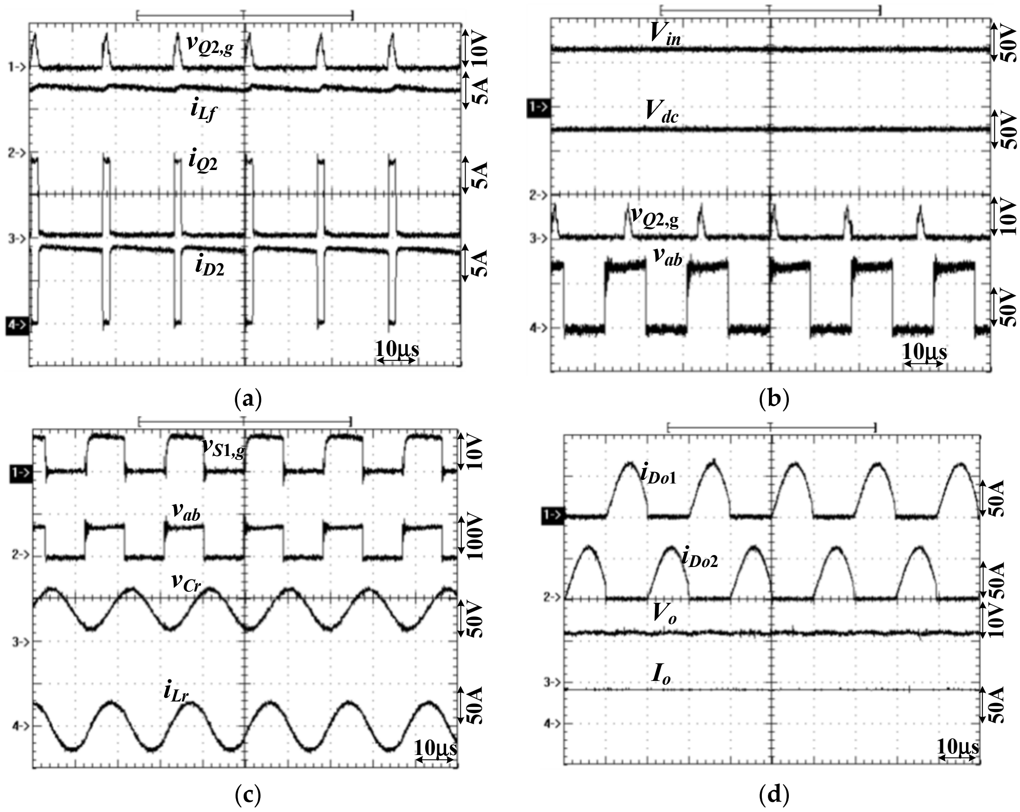

Figure 7. Measured results at V_{in} = 65 V and P_o = 500 W (**a**) $v_{Q2,g}$, i_{Lf}, i_{Q2} and i_{D2} (**b**) V_{in}, V_{dc}, $v_{Q2,g}$ and v_{ab} (**c**) $v_{S1,g}$, v_{ab}, v_{Cr} and i_{Lr} (**d**) i_{Do1}, i_{Do2}, V_o and I_o.

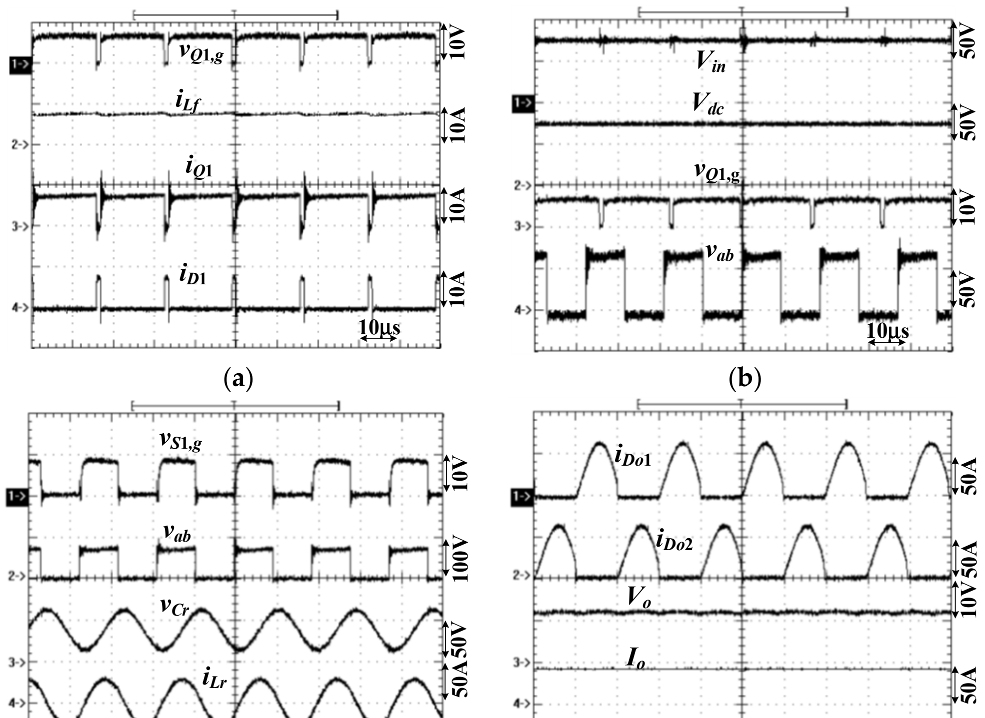

Figure 8. Measured results at V_{in} = 76 V and P_o = 500 W (**a**) $v_{Q1,g}$, i_{Lf}, i_{Q1} and i_{D1} (**b**) V_{in}, V_{dc}, $v_{Q1,g}$ and v_{ab} (**c**) $v_{S1,g}$, v_{ab}, v_{Cr} and i_{Lr} (**d**) i_{Do1}, i_{Do2}, V_o and I_o.

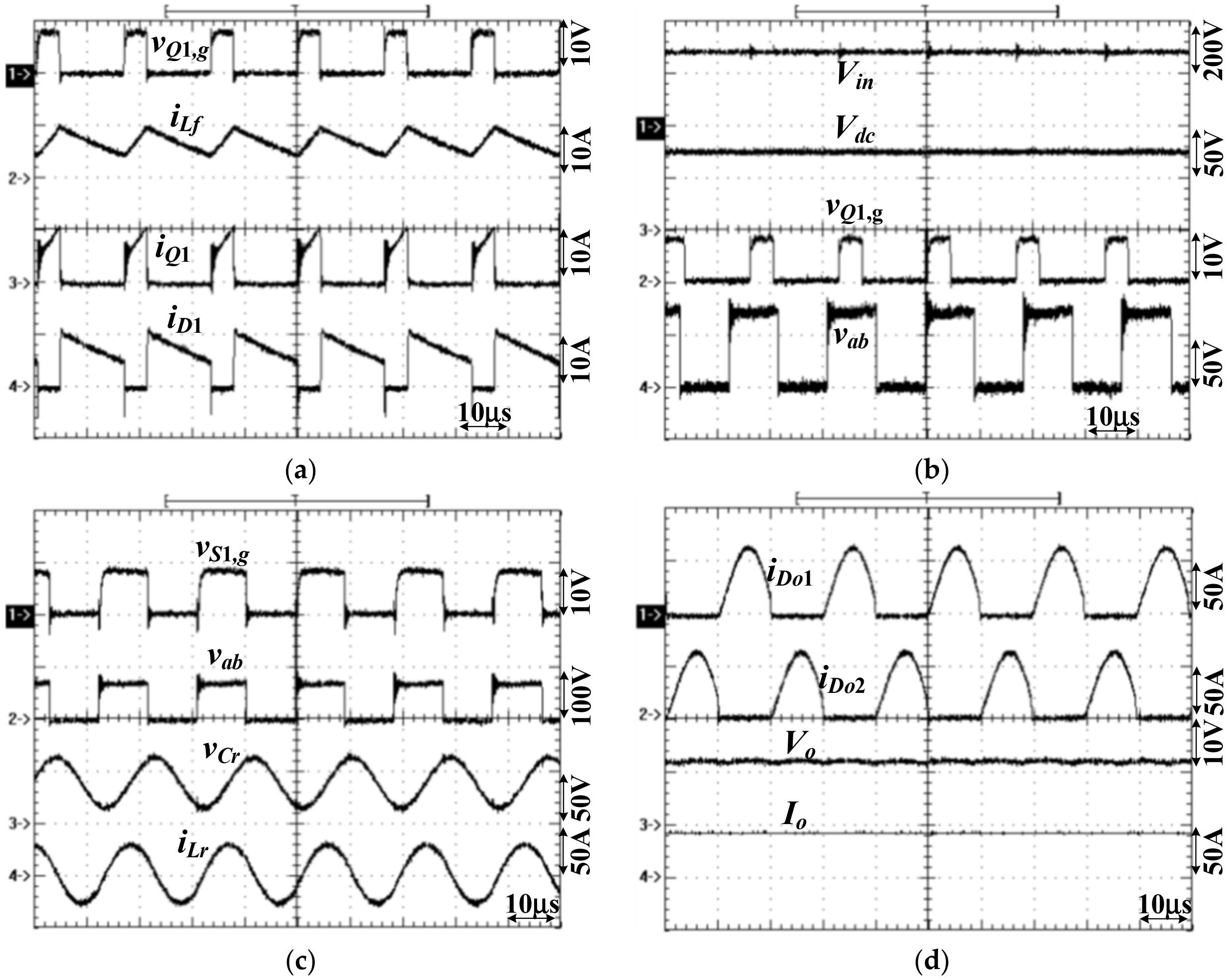

Figure 9. Measured results at V_{in} = 288 V and P_o = 500 W (**a**) $v_{Q1,g}$, i_{Lf}, i_{Q1} and i_{D1} (**b**) V_{in}, V_{dc}, $v_{Q1,\mathrm{g}}$ and v_{ab} (**c**) $v_{S1,g}$, v_{ab}, v_{Cr} and i_{Lr} (**d**) i_{Do1}, i_{Do2}, V_o and I_o.

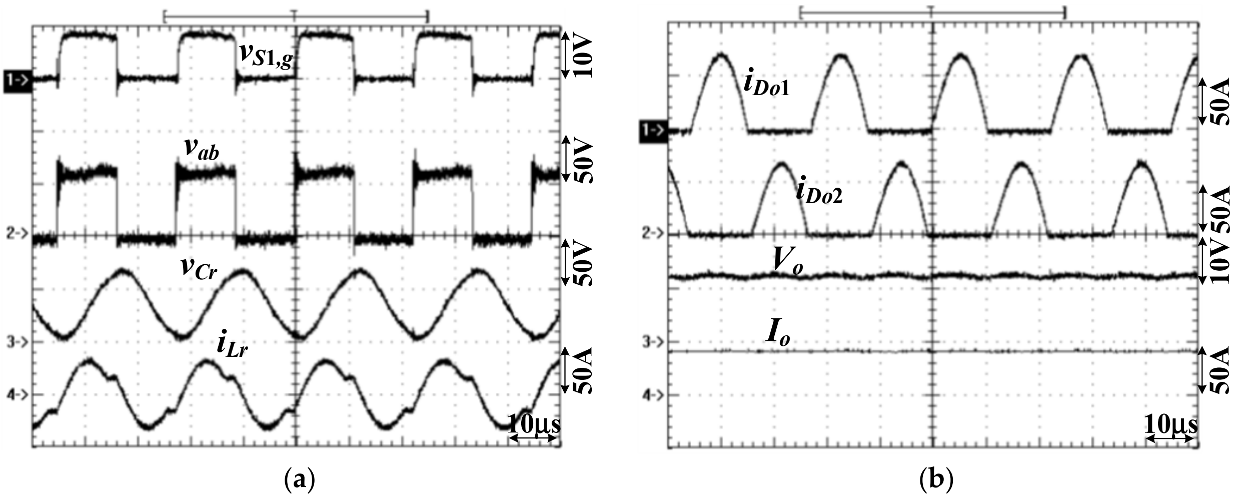

Figure 10. Measured results at V_{in} = 67 V and P_o = 500 W (**a**) $v_{S1,g}$, v_{ab}, v_{Cr} and i_{Lr} (**b**) i_{Do1}, i_{Do2}, V_o and I_o.

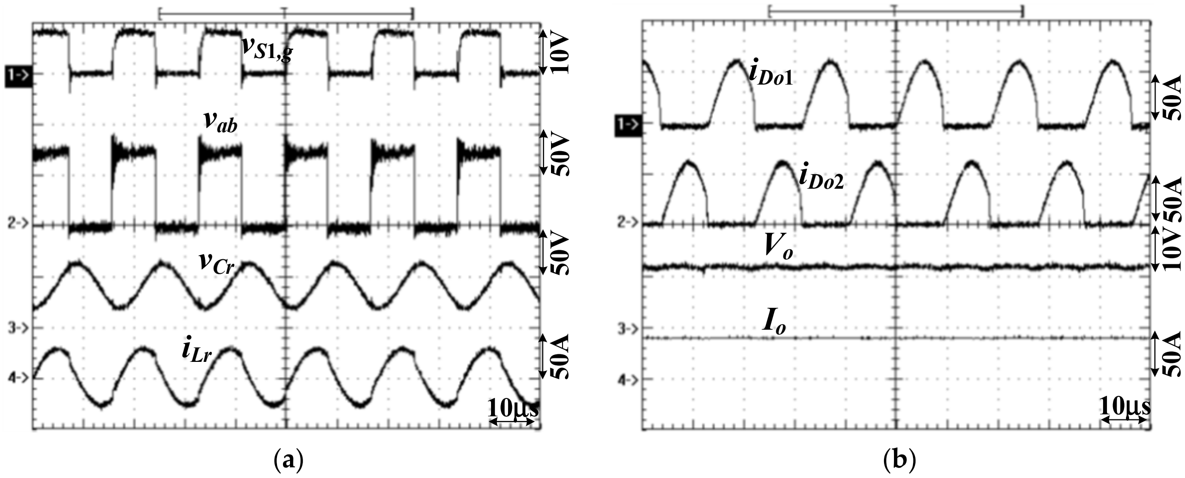

Figure 11. Measured results at V_{in} = 74 V and P_o = 500 W (**a**) $v_{S1,g}$, v_{ab}, v_{Cr} and i_{Lr} (**b**) i_{Do1}, i_{Do2}, V_o and I_o.

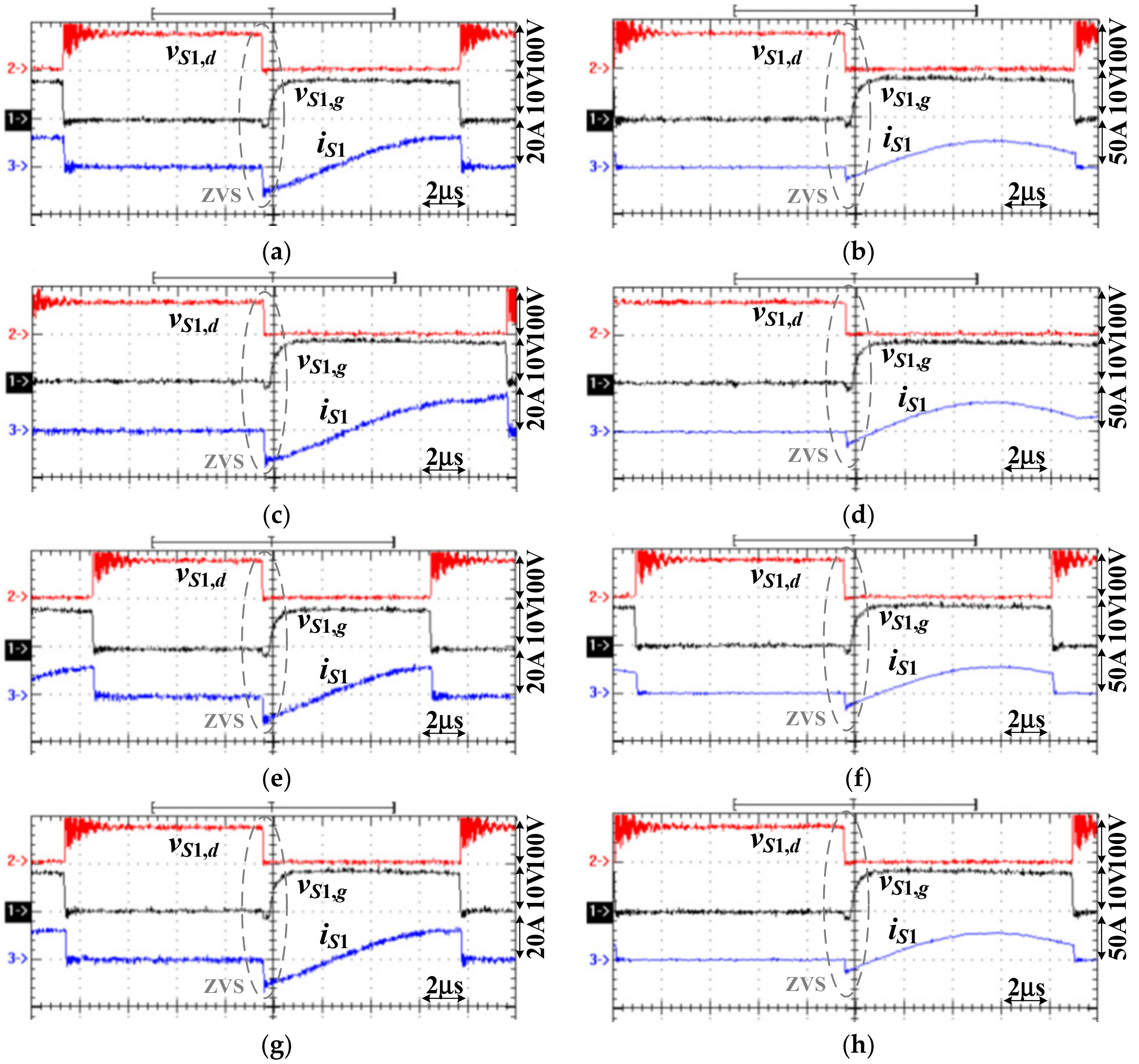

Figure 12. Experiments of switch S_1 of resonant converter at (**a**) V_{in} = 18 V and 20% power (**b**) V_{in} = 18 V and full power (**c**) V_{in} = 67 V and 20% power (**d**) V_{in} = 67 V and full power (**e**) V_{in} = 74 V and 20% power (**f**) V_{in} = 74 V and full power (**g**) V_{in} = 288 V and 20% power (**h**) V_{in} = 288 V and full power.

6. Conclusions

A wide input voltage (18 V~288 V) DC converter is discussed and examined for railway vehicles or for PV power conversion. To realize a 16:1 wide input voltage demand, a buck/boost circuit is used to accomplish the boost operation if V_{in} is on a low input voltage range and a buck operation if V_{in} is on a high input voltage range. Therefore, the DC bus voltage after the buck/boost converter is kept at a constant voltage. The resonant converter is employed on the rear-stage to achieve electric isolation and have a soft switching operation for active switches and power diodes. Since the *LLC* resonant converter is operated at a constant input voltage, the switching frequency variation is limited at a narrow frequency range. The performance of the studied circuit is investigated and examined through the test results.

Author Contributions: Writing—original draft, investigation, methodology, conceptualization, visualization, B.-R.L.; writing—review and editing, A.P.I.G.; validation, K.-W.W. All authors have read and agreed to the published version of the manuscript.

Funding: This research is supported by the Ministry of Science and Technology (MOST), Taiwan, under grant number MOST 108-2221-E-224-022-MY2.

Conflicts of Interest: The authors declare no conflict of interest.

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