



# Article Applying FPGA Control with ADC-Free Sampling to Multi-Output Forward Converter

Yeu-Torng Yau<sup>1</sup>, Kuo-Ing Hwu<sup>2,\*</sup> and Jenn-Jong Shieh<sup>3</sup>

- <sup>1</sup> Department of Ph.D. Program, Prospective Technology of Electrical Engineering and Computer Science, National Chin-Yi University of Technology, No.57, Sec. 2, Zhongshan Rd., Taiping Dist., Taichung 41170, Taiwan; tsmc35@yahoo.com.tw
- <sup>2</sup> Department of Electrical Engineering, National Taipei University of Technology, 1, Sec. 3, Zhongxiao E. Rd., Taipei 10608, Taiwan
- <sup>3</sup> Department of Electrical Engineering, Feng Chia University, No. 100, Wenhwa Road, Seatwen, Taichung 40724, Taiwan; jjshieh@fcu.edu.tw
- \* Correspondence: eaglehwu@ntut.edu.tw

**Abstract:** In this paper, a forward converter with multiple outputs is employed to build up a circuit system with full-digital control without any analog-to-digital (ADC) converter adopted. In this circuit, all the output voltages can be regulated by individual feedback control loops. As transient load variations due to the main output happens, the secondary outputs are affected quite slightly. Furthermore, the output voltage with the largest output current adopts not only the voltage mode control but also the interleaved control and current sharing control. Therefore, if this circuit system adopts full-digital control, the number of ADCs employed is relatively large, and the corresponding cost is expensive. Accordingly, the sampling of multiple output voltages and two-phase currents without any ADCs is used herein. Moreover, a nonlinear control strategy is proposed and applied to the traditional proportional-integral-derivative (PID) controller to accelerate the load transient response. In addition, the field programmable gate array (FPGA) is used as a control kernel.

**Keywords:** ADC-free sampling; current sharing control; forward converter; FPGA; interleaved control; nonlinear control; VHDL

# 1. Introduction

The more the functions in an electronic product, the more the voltage types required [1,2]. For example, in digital circuits that require different operating voltages according to different chips, multiple output positive voltage DC–DC converters are required [3,4]. In IGBT or SiC, drive circuits usually require multiple sets of multi-channel isolated power supplies with positive and negative outputs [5]. Accordingly, a DC–DC converter with good performance of multiple outputs is indispensable. Concerning the control of such a converter, it usually focuses on regulating the minimum output voltage with the maximum output current [6]. In the literature [7], the parasitic and leakage inductances lead to degrading the performance of the forward converter. In the literatures [8,9], cross regulation is discussed. As one or more output voltages are under load variations, the steady-state and dynamic cross regulations that exist between output voltages will occur.

The literatures [3,10] discuss the control of multi-output converters, but they both only take single output feedback control. From these studies, it can be found that regulation improvements based on such a method is limited. Therefore, if each output voltage is desired to be high-accuracy output voltage, then, in general, the coupled inductor and magnetic amplifier can be applied to achieve highly stabilized output voltages. If the uncontrolled output terminal adopts the coupled inductor [10,11], then the turns ratio of the coupled inductor should be equal to the turns ratio of the transformer. If not, there will be a large circulating current between the two output voltage terminals. In addition,



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**Copyright:** © 2021 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (https:// creativecommons.org/licenses/by/ 4.0/). if the output diodes have a slight difference in forward voltage between them, then the corresponding design will be complicated and unpredictable. If the uncontrolled output voltage terminal adopts the magnetic amplifier, then the circuit system control will be difficult due to the nonlinear behavior of the magnetic amplifier [12,13].

The literatures [14,15] adopt the secondary side post regulators (SSPRs) to regulate individual output voltages. In this paper, the forward converter with multiple outputs taking the SSPR technique along with synchronous rectification (SR) will be presented. There are three circuits in the proposed converter: one is an SR forward converter; another is an SR buck converter; the other is a two-phase Interleaved SR buck converter. Furthermore, the output voltage terminal with the maximum output current will adopt the interleaved control technique. In addition, the comparator sampling technique [16] will be applied to this converter to realize full digital control, and the voltage mode control is used herein to stabilize each output voltage at the desired value. Accordingly, the main novelty elements and advantages are as follows: (1) fast load transient response; (2) good current sharing; (3) good load regulation; (4) good line regulation; and (5) excellent cross regulation. In the following, Section 2 presents the system configuration; Section 3 explains the SSPR technique; Section 4 explains the two-phase interleaved control strategy; Section 5 introduces the ADC-free sampling technique; Section 6 introduces the nonlinear control strategy; Section 7 presents the experimental results; Section 8 makes comparisons; and Section 9 makes conclusions.

#### 2. System Configuration

Figures 1–3 show the proposed circuit system configuration. The main power stage is built up by an SR forward converter, as shown in Figure 1. At the same time, the SR buck converter, shown in Figure 2, is connected between point *A* and the ground, as shown in Figure 1, whereas an SR two-phase interleaved buck converter, shown in Figure 3, is connected between point *A* and the ground, as shown in Figure 1. The output voltage of the main output is signified by  $v_{o1}$ , the output voltage of the first secondary output is indicated by  $v_{o2}$ , and the output voltage of the second secondary output is denoted by  $v_{o3}$ . Each output voltage is controlled at a desired value based on sampling without ADC. As for the current sharing between two phases, it is achieved also based on sampling without ADC.



Figure 1. SR forward converter.



Figure 2. SR buck converter.



Figure 3. Two-phase interleaved SR buck converter.

The main output is constructed by an SR forward converter with an LC snubber built up by two diodes  $D_{s1}$  and  $D_{s2}$ , one inductor  $L_s$ , and one capacitor  $C_s$ . As for this converter, it is established by one transformer with two windings  $N_1$  and  $N_2$  and magnetizing inductance, one main switch  $S_1$  with one body diode  $D_{p1}$ , two SR switches  $S_2$  and  $S_3$  with individual body diodes  $D_{p2}$  and  $D_{p3}$ , one output inductor  $L_{o1}$ , one output capacitor  $C_{o1}$ , and one output resistor  $R_1$ . Regarding the corresponding symbols for currents and voltages,  $V_i$  is the input voltage,  $i_{Ds1}$  is the current flowing through  $D_{s1}$ ,  $i_{Ls}$  is the current flowing through  $L_s$  or  $D_{s2}$ ,  $i_{Cs}$  is the current flowing through  $C_s$ ,  $i_{S1}$  is the current flowing through  $S_1$ ,  $i_{S2}$  is the current flowing through  $S_2$ ,  $i_{S3}$  is the current flowing through  $S_3$ ,  $i_{Lo1}$  is the current flowing through  $L_{o1}$ ,  $v_{Lo1}$  is the voltage across  $L_{o1}$ ,  $v_{Cs}$  is the voltage across  $C_s$ , and  $v_{o1}$  is the voltage across  $R_1$ .

The first secondary output is constructed by the SR buck converter. As for this converter, it is established by one main switch  $S_4$  with one body diode  $D_{p4}$ , one SR switch  $S_5$  with one body diode  $D_{p5}$ , one output inductor  $L_{o2}$ , one output capacitor  $C_{o2}$ , and one output resistor  $R_2$ . Regarding the corresponding symbols for currents and voltages,  $i_{S4}$  is the current flowing through  $S_4$ ,  $i_{S5}$  is the current flowing through  $S_5$ ,  $i_{Lo2}$  is the current flowing through  $L_{o2}$ ,  $v_{Lo2}$  is the voltage across  $L_{o2}$ , and  $v_{o2}$  is the voltage across  $R_2$ .

The second secondary output is constructed by the two-phase interleaved SR buck converter. As for this converter, it is established by two main switches  $S_6$  and  $S_8$  with individual body diodes  $D_{p6}$  and  $D_{p8}$ , two SR switches  $S_7$  and  $S_9$  with individual body diodes  $D_{p7}$  and  $D_{p9}$ , two output inductors  $L_{o3}$  and  $L_{o4}$ , one output capacitor  $C_{o3}$ , and one output resistor  $R_3$ . Regarding the corresponding symbols for currents and voltages,  $i_{56}$ ,  $i_{57}$ ,  $i_{58}$  and  $i_{59}$  are the currents flowing through  $S_6$ ,  $S_7$ ,  $S_8$  and  $S_9$ , respectively,  $i_{Lo3}$  and  $i_{Lo4}$  are the currents flowing through  $L_{o3}$  and  $L_{o4}$ , respectively,  $v_{Lo3}$  and  $v_{Lo4}$  are the voltages across  $L_{o3}$  and  $L_{o4}$ , respectively, and  $v_{o3}$  is the voltage across  $R_3$ .

# 3. SSPR Technique

The SSPR technique can be classified into trailing-edge modulation and leading-edge modulation. Concerning the former, the main switches for the main output and the first secondary output are switched on with the same turn-on moment, as shown in Figure 4, resulting in reducing the peak current flowing through the main switch of the main output. Regarding the latter, the main switches for the main output and the first secondary output are both switched off with the same turn-off moment, as shown in Figure 5, leading to being widely used in peak current mode control. This is because the former has an error in

trigger due to having two peak values. However, in this paper, only the voltage control is utilized. Consequently, such a problem never happens, and hence the former is employed to reduce the peak current in the main switch of the main output, as well as to adjust easily the duty cycle for the main switch of the first secondary output.



Figure 4. Trailing-edge modulation technique.



Figure 5. Leading-edge modulation technique.

## 4. Two-Phase Interleaved Control Strategy

In the three output voltages, the interleaved control strategy is applied to the output voltage with the maximum output current. As for the SSPR technique, it is applied to multiple outputs; all the main switches should be switched on within the turn-on time of the main output. By doing so, the energy can be transferred from the input to the load. If the switching period of the second secondary output is the same as that of the main output, the second phase cannot transfer energy, as shown in Figure 6. Accordingly, the switching period of the second secondary output should be double that of the main output, as shown in Figure 7.



Figure 6. Two-phase switching period equal to that of the main output.



Figure 7. Two-phase switching period equal to double that of the main output.

#### 5. ADC-Free Sampling Technique

# 5.1. Comparator Sampling

The ADC-free sampling technique based on the comparator is used as a method for sampling the output voltages of the proposed multi-output forward converter. There are two counters and one sampling block in the FPGA. One is a fixed period counter *PWM\_CNT*, and the other is a counter *CNT* cooperated with a sampling block to count. The digital output voltage feedback information, named the value of CNT, is generated by comparing the output feedback voltage  $v_{o-sense}$  and the reference voltage  $V_{ref}$  through a comparator and a counter CNT. The reference voltage  $V_{ref}$  will be set as the average value of the output feedback voltage, and then a signal VFB with a high or low level will be obtained. Afterwards, this digital signal is sent to the FPGA, and cooperated with a sampling block, which is pre-written by using the very high-speed hardware description language (VHDL). The sampling block gets started within the preset range of the *PWM\_CNT* count value as the basis for starting and stopping the counting of CNT; CNT counts within one period and its value is the digital output voltage feedback information. The sampling block action is shown in Figure 8. First, supposing that the equivalent series resistance (ESR) of the output capacitor of the converter is large enough, the output voltage waveform is the DC output voltage plus the approximately linear triangular wave ripple. PWM\_CNT starts the sampling block at  $t_0$  and disables the sampling block at  $t_3$ . At the beginning of a switching cycle  $t_0$ , PWM\_CNT starts counting from zero and the sampling block starts. During the time interval between  $t_0$  and  $t_1$ , the output feedback voltage is smaller than  $V_{ref}$ . The output signal of the comparator is one (that is, VFB = 1), and CNT does not count. At  $t_1$ , the output feedback voltage is greater than the reference voltage, hence the comparator output changes from high level to low level (that is, VFB changes from one to zero), thereby making CNT start counting from zero. When the comparator output changes again (that is, when VFB changes from zero to one) at  $t_2$ , CNT stops counting, the sampling block is disabled, and the value of CNT is the digital output voltage feedback information.

Here the sampling clock is the same as the FPGA clock. If the sampling clock is defined as  $f_{sm}$ , then the value of *CNT* is

$$CNT = f_{sm}(t_2 - t_1) \tag{1}$$

Rewrite (1) as

$$CNT = f_{sm}[(t_a - t_1) + (t_2 - t_a)]$$
(2)

From the geometrical relationship, it can be seen that the instantaneous values of the signal  $v_{o-sense}$  to be sampled at  $t_1$  and  $t_2$  are

$$v_{o-sense}(t_1) = \frac{v_{o-ripple}}{\left(\frac{T_s}{2}\right)}(t_a - t_1)$$
(3)

$$v_{o-sense}(t_2) = \frac{v_{o-ripple}}{\left(\frac{T_s}{2}\right)}(t_2 - t_a) \tag{4}$$

Substituting Equation (3) and Equation (4) into Equation (2) yields

$$CNT = f_{sm} \frac{T_s}{2} \frac{[v_{o-sense}(t_1) + v_{o-sense}(t_2)]}{v_{o-rivvle}}$$
(5)

Equation (5) describes a linear mapping transformation from the analog value to the digital value. Therefore, the resolution of the digital feedback value is as follows:

$$Resolution = (t_3 - t_0) f_{sm} \tag{6}$$



Figure 8. Action of the comparator sampling block. CNT: counter; VFB: voltage feedback.

In the following, based on Figures 9-12, three cases and the corresponding control loop will be given. Under a constant switching frequency, since the FPGA clock is 100 MHz and the system switching frequency is 200 KHz, the PWM\_CNT counting cycle is set to 500CLK, so when the sampling block is enabled, it can be seen from Equation (1) that there are three cases for the value of CNT. The first case is that the average value of the output feedback voltage  $v_{o-sense}$  is equal to the value of  $V_{ref}$ , so the comparator output will get a signal *VFB* with the high-level time interval equal to the low-level time interval. At this time, the value of CNT will be equal to 250CLK, so the output voltage error  $v_{o-error}$  obtained by subtracting the value of *REG* from the reference value of 250 is zero, implying that the duty cycle of PWM remains fixed, as shown in Figure 9. It is noted that *REG* is the register for the value of CNT. The second case is that the average value of  $v_{o-sense}$  is less than the value of  $V_{ref}$ , and the comparator output will get a digital signal VFB with the high-level time interval larger than the low-level time interval. At this time, the value of CNT will be less than 250CLK. Therefore, the digital reference value 250 minus REG will produce a positive error value, so the PWM duty cycle must be increased to boost up the output voltage, as shown in Figure 10. The third case is that the average value of  $v_{o-sense}$  is greater than the value of  $V_{ref}$ , and the comparator output will get a digital signal VFB with the high-level time interval smaller than the low-level time interval. At this time, the value of CNT will be more than 250CLK. Therefore, the digital reference value of 250 minus REG will produce a negative error value, so the PWM duty cycle must be decreased to reduce the output voltage, as shown in Figure 11.



**Figure 9.** Average value of  $v_{o-sense}$  equal to the value of  $V_{ref}$ .



**Figure 10.** Average value of  $v_{o-sense}$  less than the value of  $V_{ref}$ .



**Figure 11.** Average value of  $v_{o-sense}$  greater than the value of  $V_{ref}$ .



Figure 12. Control loop block diagram: PID: proportional-integral-derivative; REG: register.

For the control loop shown in Figure 12, when the sampling block is disabled within the remaining time of *PWM\_CNT*, that is, before the end of a cycle, the value of *REG* is subtracted from the digital reference value of 250 to obtain output voltage error  $v_{o-error}$ , and this error is sent to the digital proportional-integral-derivative (PID) controller for calculation. Eventually, the controller outputs a control force  $v_f$ , and this control force is added to a digital value of 250, leading to generating the corresponding duty cycle; this duty cycle will be limited to the prescribed range and then will be used in the next cycle.

# 5.2. Triangular Wave Injection Method

The previous discussion of the ADC-free sampling technology is to consider that the output capacitor of the DC–DC converter has an equivalent series resistance (ESR), so its

output voltage waveform possesses the DC voltage and triangular ripple. However, since the solid organic semiconductor capacitor (OSCON) or the multilayer ceramic capacitor (MLCC) can be used as the output voltage capacitor, the output voltage ripple will become smaller, and the linearity of the output voltage ripple waveform is degraded, as shown in Figure 13.



Figure 13. Output voltage ripple with nonlinearity.

Therefore, this section will introduce a triangular wave injection method to improve the problem that the voltage cannot be accurately controlled due to the decrease in the linearity of the output voltage ripple. The solution is to inject a triangular wave into the output feedback voltage to improve the output voltage ripple due to poor linearity, as shown in Figure 14; hence, a modified triangular waveform will be obtained, which is combined with the previously-discussed comparator sampling method to obtain precise output voltage control, as shown in Figure 15.



Figure 14. Comparator sampling with the triangular wave injection method.



Figure 15. Waveforms before and after triangular wave injection.

In the following, the accuracy after injection can be expressed as follows. From Equation (7), it can be seen that there is a relationship between the sampling accuracy and peak-to-peak value of the triangular wave injected output voltage, called  $\tilde{v}_{op}$ . Therefore,  $\tilde{v}_{op}$ 

is large. Although the original poor linearity of the output voltage ripple can be modified into a better linearity of the triangular waveform, according to Equation (7), the cost of the injection method is at the expense of sampling accuracy.

$$Accuracy = \frac{\widetilde{v}_{op}}{\text{Resolution}}$$
(7)

# 5.3. Interleaved Current Sampling Method

In this paper, an interleaved ADC-free sampling strategy is proposed. Firstly, it is assumed that the inductor current ripple is small enough and the amplitude of the injected triangular wave is large enough. In Figure 16, the currents  $i_{s1}$  and  $i_{s2}$ , generated by individual current sensing devices with the same gain K, are added to individual triangular waves and then compared with the same prescribed current reference  $I_{ref}$  to obtain high- or low-level signals (IFB1 and IFB2). Afterwards, these two signals are sent to the FPGA, which has four counters. There are two synchronous counters, PWM\_ICNT1 and PWM\_ICNT2, with the same period and two counters, ICNT1 and ICNT2, in the sampling block. Accordingly, the value of ICNT1 minus the value of ICNT2 can be obtained, and then this result is sent to the current sharing controller. Therefore, the corresponding control force  $v_{f1}$  will be obtained. The sampling operation principle in the sampling block is the same as mentioned in Section 5.1, so it will not be redescribed herein. The next duty cycle of *PWM*1 can be determined by the present values  $v_{f1}$  and  $v_{f2}$  based on  $v_{f2}$  minus  $v_{f1}$  plus DUTY\_CYCLE, and then passed through a prescribed limiter, called *Limiter*1, whereas the next duty cycle of *PWM*2 can be determined by the prescribed values  $v_{f1}$  and  $v_{f2}$  based on  $v_{f2}$  plus  $v_{f1}$  plus DUTY\_CYCLE, and then passed through a prescribed limiter, called Limiter2, with a phase shift of 180 degrees from PWM1. In Figure 17, PWM\_ICNT1 counts between  $t_0$  and  $t_2$ , whereas PWM\_ICNT2 counts between  $t_1$  and  $t_3$ ; ICNT1 counts between  $t_a$  and  $t_1$ , whereas *ICNT*<sup>2</sup> counts between  $t_b$  and  $t_2$ . Additionally, *PWM\_ICNT*<sup>2</sup> will start to count when PWM\_ICNT1 counts to half of the cycle. ICNT1 and ICNT2 will get different or identical count values, which can be regarded as feedback information of the two-phase currents at the same point.



Figure 16. Block diagram of sampling and control loop.



Figure 17. Interleaved current sampling.

# 6. Nonlinear Control Strategy

The nonlinear control strategy is explained in detail as follows. For the upload mode to be considered, as shown in Figure 18, when the value of *REG* is equal to the value of *MIN\_CNT*, the program chooses to disable the PID controller and fix the duty cycle at a certain value higher than the steady-state duty cycle. However, in order to prevent the transformer of the forward converter from being saturated, the time required for resetting the magnetic flux of the transformer must be considered. Here, the duty cycle  $d_m$  for the main output is set to 0.62 to make the output feedback voltage ripple rapidly climb to approach the reference voltage. For the normal mode to be considered, when the value of *REG* is between the value of *MIN\_CNT* and the value of *MAX\_CNT*, that is, when the reference voltage is within the output feedback voltage ripple, the open loop control is disabled and the PID controller is restored to reduce the steady-state error. For the download mode to be considered, when the value of REG is equal to the value of MAX\_CNT, it means that the output voltage is too high. The program chooses to disable the PID controller and reduce the duty cycle to a value lower than the steady-state duty cycle. As discussed in Section 5, the duty cycle  $d_m$  for the main output must be larger than the duty cycles for the other two secondary outputs. If not, two secondary outputs will not be supplied with electricity. So, the value of  $d_m$  will be set to be greater than the maximum value of the steady-state duty cycle of the two secondary outputs, such as  $d_a$ .



Figure 18. Block diagram for nonlinear control.

#### 7. Experimental Results

Prior to this section, Tables 1–3 display the specifications for the main output, the first secondary output, and the second secondary output.

Table 1. Main output specifications.

System Parameters	Specifications
Operating Mode	CCM
Input Voltage ( $V_i$ )	$36 \mathrm{V} \pm 10\%$
Output Voltage ( $V_{o1}$ )	12 V
Rated Output Current ( <i>I</i> <sub>01</sub> )	10 A
Rated Output Power ( $P_{o1}$ )	120 W
Turns Ratio ( $n = N_2/N_1$ )	5/6
Inductor Current Slew Rate (SR <sub>L01</sub> )	2 A/µs
Switching Frequency ( $f_{s1}$ )	200 kHz
Output Voltage Ripple ( $\Delta v_{o1,max}$ )	=<100 mV

Table 2. First secondary output specifications.

System Parameters	Specifications
Operating Mode	CCM
Input Voltage ( $V_i$ )	$36 \text{ V} \pm 10\%$
Output Voltage ( $V_{o2}$ )	5 V
Rated Output Current ( $I_{o2}$ )	8 A
Rated Output Power ( $P_{o2}$ )	120 W
Inductor Current Slew Rate ( $SR_{Lo2}$ )	2 A/µs
Switching Frequency ( $f_{s2}$ )	200 kHz
Output Voltage Ripple ( $\Delta v_{o2,max}$ )	=<100 mV

Table 3. Second secondary output specifications.

System Parameters	Specifications	
Operating Mode	ССМ	
Input Voltage $(V_i)$	$36~\mathrm{V}\pm10\%$	
Output Voltage ( $V_{o3}$ )	3.3 V	
Rated Output Current ( $I_{03}$ )	12 A	
Rated Output Power ( $P_{o3}$ )	40 W	
Inductor Current Slew Rate (SR <sub>L03</sub> )	2 A/µs	
Switching Frequency ( $f_{s3}$ )	200 kHz	
Output Voltage Ripple ( $\Delta v_{o3,max}$ )	=<100 m	

## 7.1. Current Sharing Waveforms

The waveforms shown in Figure 19 are two-phase inductor currents of the second secondary output at the rated load and in the steady state. The inductor current waveforms shown in Figures 20 and 21 are load transient responses from the rated/light load to light/rated load for the second secondary output. Therefore, it can be found that from this figure, the proposed two-phase interleaved current sampling method, together with the current sharing control, can make the output current evenly distributed among two phases. As the load changes, the two inductor currents will follow each other. It is noted that variations in each inductor current due to a step load change from the light/rated load to rated/light load belong to a large-signal response. Accordingly, each current-sharing controller with only the proportional gain  $k_p$  used to make the corresponding inductor current during the download transient period only has one undershoot. Therefore, the value of  $k_p$  is tuned to be 0.4. Afterwards, this value of  $k_p$  is applied to the upload transient response, causing each inductor current to have an overshoot and ring.



Figure 19. Two-phase inductor currents at rated load for the second secondary output.



Figure 20. Load transient response from light load to rated load for the second secondary output.



Figure 21. Load transient response from rated load to light load for the second secondary output.

# 7.2. Dynamic Cross Regulation Performance

Figures 22 and 23 show that the main output is varied from a light/rated load to rated/light load, respectively, on the condition that the first and second secondary outputs are at a light load, whereas Figures 24 and 25 show that the main output is varied from a light/rated load to rated/light load, respectively, on the condition that the first and second secondary outputs are at a rated load. The results of the dynamic cross regulation are tabulated in Table 4, including the peak overshoot voltage, peak undershoot voltage, peak

overshoot voltage percentage, peak undershoot voltage percentage, and setting time. From Table 4, it can be seen that each response has its peak overshoot and undershoot voltage percentages within 1.6%, which are smaller than 5% from industrial applications.



**Figure 22.** Dynamic response waveforms on condition that the main output load is changed from light load to rated load as the first and second secondary outputs are located at light load.



**Figure 23.** Dynamic response waveforms on condition that the main output load is changed from rated load to light load as the first and second secondary outputs are located at light load.



**Figure 24.** Dynamic response waveforms on condition that the main output load is changed from light load to rated load as the first and second secondary outputs are located at rated load.





Table 4. Results for dynamic cross regulation.

Item	Figure	22	23	24	15
	Peak Overshoot	<i>v</i> <sub>01</sub> : 156.52 mV	<i>v</i> <sub>01</sub> : 104.35 mV	<i>v</i> <sub>01</sub> : 130.43 mV	<i>v</i> <sub>01</sub> : 104.35 mV
1	or	<i>v</i> <sub>02</sub> : 17.39 mV	<i>v</i> <sub>02</sub> : 17.39 mV	<i>v</i> <sub>02</sub> : 52.19 mV	<i>v</i> <sub>02</sub> : 34.78 mV
	Undershoot	v <sub>o3</sub> : 52.17 mV	<i>v</i> <sub>03</sub> : 26.09 mV	<i>v</i> <sub>03</sub> : 34.78 mV	<i>v</i> <sub>03</sub> : 52.17 mV
	Percentage of	1.31% of V <sub>01</sub>	0.87% of V <sub>01</sub>	1.09% of V <sub>01</sub>	0.87% of <i>V</i> <sub>01</sub>
2	Output Voltage for	0.35% of V <sub>02</sub>	0.35% of V <sub>02</sub>	1.04% of V <sub>02</sub>	0.70% of V <sub>02</sub>
	Item 1	$1.58\%$ of $V_{o3}$	0.79% of V <sub>03</sub>	1.06% of V <sub>03</sub>	$1.58\%$ of $V_{o3}$
		v <sub>01</sub> : 40 μs	<i>v</i> <sub>01</sub> : 40 μs	<i>v</i> <sub>01</sub> : 40 μs	$v_{o1}: 40 \ \mu s$
3	Setting Time	v <sub>o2</sub> : 60 μs	<i>v</i> <sub>02</sub> : 60 μs	<i>v</i> <sub>02</sub> : 40 μs	<i>v</i> <sub>o2</sub> : 40 μs
	Ū.	v <sub>o3</sub> : 80 μs			

# 7.3. Overall Efficiency and Prototype Photo

Figure 26 shows the overall efficiency, where each point of the efficiency cure is plotted at the same load current percentage for three outputs. From this figure, it can be seen that the efficiency can be up to 91% and the efficiency at the rated load is 86%. In addition, Figure 27 displays the photo of the experimental setup.



Figure 26. Curve of efficiency versus load current at the same load current percentage for three outputs.



Figure 27. Photo of the experimental setup.

# 7.4. Current Sharing Error Percentage

Figure 28 shows the current sharing error percentage, which is obtained based on the following equation:

Current Sharing Error % = 
$$\left| \frac{I_{03} - I_{04}}{I_{03} + I_{04}} \right| \times 100\%$$
 (8)



Figure 28. Curve of current sharing error versus load current for the second secondary output.

Therefore, the corresponding maximum value of the current sharing error percentage, displayed in Figure 28, is 3.8%, which is smaller than the 5% from industrial applications.

## 7.5. Load Regulation

Figure 29 shows the load regulation of the main output on the condition that the first and second secondary outputs are at the rated load. Figure 30 shows the load regulation of the first secondary output on the condition that the main and second secondary outputs are at the rated load. Figure 31 shows the load regulation of the second secondary output on the condition that the main and first secondary outputs are at the rated load. After that, the load regulation percentage equation is defined as:

Load Regulation % = 
$$\left| \frac{V_o(\text{Rated Load}) - V_o(\text{Light Load})}{V_o(\text{Half Load})} \right| \times 100\%$$
 (9)







**Figure 30.** Curve of first secondary output voltage versus load current on condition that the main and second secondary outputs are located at rated load.



**Figure 31.** Curve of second secondary output voltage versus load current on condition that the main and first secondary outputs are located at rated load.

Therefore, the corresponding values of the load regulation percentages for Figures 29–31 are 0.17%, 0.60% and 0.91%, respectively, which are all smaller than the 1% from industrial applications.

# 7.6. Line Regulation

Figure 32 shows the line regulation of the main output on the condition that the first and second secondary outputs are at the rated load. Figure 33 shows the line regulation of the first secondary output on the condition that the main and second secondary outputs are at the rated load. Figure 34 shows the line regulation of the second secondary output on the condition that the main and first secondary outputs are at the rated load. Afterwards, the line regulation percentage equation is defined to be the following:

Line Regulation % = 
$$\left| \frac{V_o(\text{High Input Voltage}) - V_o(\text{Low Input Voltage})}{V_o(\text{Rated Input Voltage})} \right| \times 100\%$$
 (10)



**Figure 32.** Curve of main output voltage versus input voltage on condition that the first and second secondary outputs are located at rated load.



**Figure 33.** Curve of first secondary output voltage versus input voltage on condition that the main and second secondary outputs are located at rated load.



**Figure 34.** Curve of second secondary output voltage versus input voltage on condition that the main and first secondary outputs are located at rated load.

Therefore, the corresponding values of the line regulation percentages for Figures 32–34 are 0.17%, 0.60% and 0.91%, respectively, which are all smaller than the 1% from industrial applications.

#### 8. Comparisons

Table 5 shows the comparisons between the proposed circuit and the existing circuits, including output number, feedback number, converter type, voltages and powers, number of passive components, cross regulation, advantages, disadvantages, and rated-load efficiency. From Table 5, it can be seen that the proposed circuit has high accuracy, a fast transient load response and excellent cross regulation.

Item	Proposed	[5]	[10]	[13]	[14]
Output Number	3	6	6	4	2
Feedback Number	3	1	1	4	2
Converter Type	Forward +SSPRs	Flyback	Push-pull + Coupled Inductor	Resonant Converter +Magnetic Amplifier	LLC+SSPRs
Voltages and Powers	12V/120W 5V/8A 3.3V/12A	16V/1.6W -16V/1.6W 16V/1.6W -16V/1.6W 16V/1.6W -16V/1.6W	3.4V/17.5W 6.4V/7.2W -6.4V/2.6W 14V/1.3W -14V/1.3W 14V/0.6W 60V/1.8W	3.3V/132W 5V/170W 12V/300W –12V/12W	100V/60W 100V/60W
Number of Passive Components	4 Magnetic Devices 0 Diodes	3 Magnetic Devices 6 Diodes	2 Magnetic Devices 16 Diodes	10 Magnetic Devices 16 Diodes	1 Magnetic Device 4 Diodes
Number of Active Components	7	1	2	10	4
Cross Regulation	Excellent	Poor	Medium	Good	Good
Advantages	High Accuracy Fast Load Transient Response	Single PWM IC and Switch	1 Transformer 1 Inductor	High Accuracy	High Accuracy
Disadvantages	Complex	High cost	Complex	Complex High Cost	Two Outputs with the Same Voltage
Rated-Load Efficiency	86%	NA	NA	85%	90%

Table 5. Comparisons between the proposed circuit and the existing circuits.

# 9. Conclusions

An SR forward converter with a set of three outputs takes the SSPR technology to control the stability of the output voltages. The output with the largest current adopts a two-phase interleaved structure, and the associated switching period is twice that of the main switch of the main output to facilitate the realization of the proposed current sharing strategy. The voltage/current sampling for each output adopts ADC-free sampling technology. In the two-phase current sampling for the second secondary output, the proposed interleaved current sampling method is employed so that the currents in two phases are sampled in the same position. As for the voltage controller to be concerned, a nonlinear control strategy is added to the traditional PID controller so that the main output can accelerate the load transient response when the load changes instantaneously. From the experimental results, as the transient load variations due to the main output happen, the effect of these variations on the secondary outputs is quite small, meaning that the proposed circuit has excellent cross regulation performance. In addition, a low current sharing error percentage, low load regulation percentage and low line regulation percentage are also advantages of the proposed circuit.

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