

## Article

# Wideband Reconfigurable Integrated Low-Pass Filter for 5G Compatible Software Defined Radio Solutions

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**Abstract:** This article presents a wideband reconfigurable integrated low-pass filter (LPF) for 5G NR compatible software-defined radio (SDR) solutions. The filter uses Active-RC topology to achieve high linearity performance. Its bandwidth can be tuned from 2.5 MHz to 200 MHz, which corresponds to a tuning ratio of 92.8. The order of the filter can be changed between the 2nd, 4th, or 6th order; it has built-in process, voltage, and temperature (PVT) compensation with a tuning range of  $\pm 42\%$ ; and power management features for optimization of the filter performance across its entire range of bandwidth tuning. Across its entire order, bandwidth, and power configuration range, the filter achieves in-band input-referred third-order intercept point (IIP3) between 32.7 dBm and 45.8 dBm, spurious free dynamic range (SFDR) between 63.6 dB and 79.5 dB, 1 dB compression point ( $P_{1dB}$ ) between 9.9 dBm and 14.1 dBm, total harmonic distortion (THD) between  $-85.6$  dB and  $-64.5$  dB, noise figure (NF) between 25.9 dB and 31.8 dB and power dissipation between 1.19 mW and 73.4 mW. The LPF was designed and verified using 65 nm CMOS process; it occupies a  $0.429$  mm<sup>2</sup> area of silicon and uses a 1.2 V supply.



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**Keywords:** 5G; active-RC; reconfigurable; software defined; low-pass; wideband

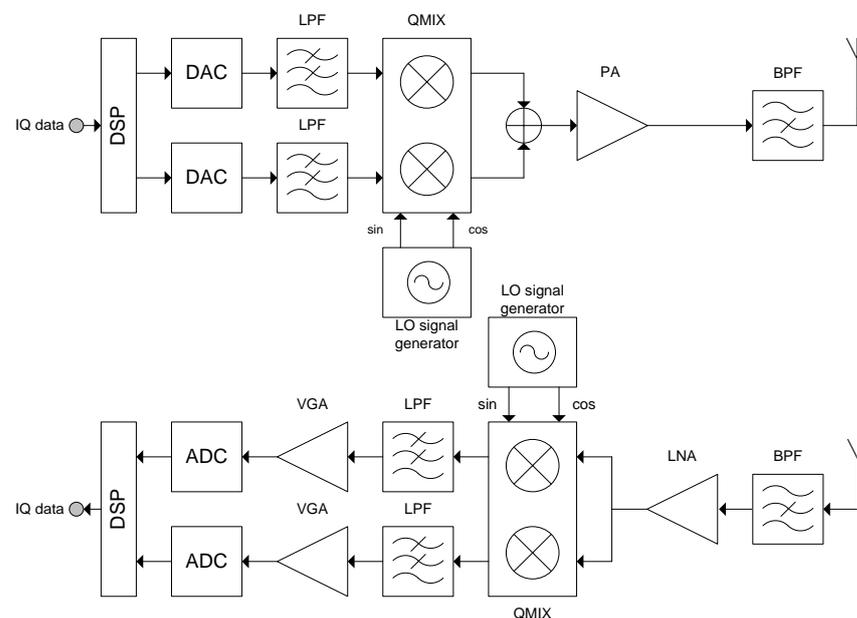
## 1. Introduction

### 1.1. Background

Constant growth and evolution of telecommunication market has set new requirements for wireless connection devices. One of the main requirements—hardware deployed in the field—must have the ability to be re-configured, thus enabling support of new or developing technologies. One of the widely developed and promising technologies is a software defined radio (SDR) [1]. The main idea behind this technology—a wide range of physical level functions—can be supported and implemented using the same hardware. Ideally, support of various physical level functions would be then defined and limited only by the software. In reality, the hardware used in the SDR still defines what physical level functions can be controlled with software, but it is designed in a way that enables access to various parameter changes via digital control.

SDR transceivers are already used in the telecommunication industry as base stations, test and measurement equipment, and intelligent transport system frameworks to transmit and receive data in a wide frequency range, usually implemented as a single integrated circuit (IC) [2–4]. An important economic problem lies behind this approach—designed hardware must have competitive price and market introduction time, which does not fall within existing standards of telecommunication market. The competitive price is achieved by a decreasing number of discrete components, which is needed to implement software defined radio, e.g., by increasing scale of integration. It is made by employing fast-improving manufacturing technologies of integrated circuits to combine various hardware components into a single chip [5,6].

Transceivers used in SDRs are usually referred to as multi-standard, since they can be configured to work with different channel bandwidths, modulation, channel access methods, and other configurations of communication channel [7,8]. Due to the versatility of its configuration, direct conversion transceiver architecture is best suited and most widely used in SDR implementations [9–11]. A common structure of a direct conversion transceiver is shown in Figure 1. It is composed of a digital signal processing (DSP) stage, followed by a digital to analog or vice versa conversion interface (DAC or ADC), then an analog baseband, which is composed of a set of variable gain amplifier (VGA) and channel selection filter stages. The analog baseband is connected to a quadrature signal mixer (QMIX), used for baseband signal frequency conversion, where the radio frequency (RF) is set by the local oscillator (LO) signal generator. Depending on the radio link direction, the RF signal is amplified either by a power amplifier (PA) or low noise amplifier (LNA) stage.



**Figure 1.** General structure diagram of a direct conversion architecture transceiver.

Channel selection filters in SDR transceivers, alongside tuneable band selection filters (BPF), are used to suppress unwanted out-of-band signals and images, what prevents desensitization of receiver and allows meeting adjacent channel power ratio (ACPR) requirements [12]. Requirements for channel selection filters are changing with an increasing number of wireless standards. Channel bandwidth can be dynamically changed to distribute the available resources across the entire network. Due to this dynamic nature of modern wireless traffic, channel selection filters used in SDR applications have to meet one main requirement—their parameters have to be controllable. Thus, the reconfigurable nature of the SDR requires that the baseband channel selection filters, which in direct conversion transceivers are usually implemented as low-pass filters (LPF), should have a high degree of filter configuration capabilities, mainly focused, but not limited to bandwidth, power dissipation, and order of the filter [13].

### 1.2. Motivation

One of the most developed and deployed air interface cellular mobile communication technology is 3GPP LTE, while its successor, 5G NR, has been for some time and still is a major focus of many researchers regarding various use-cases in network resource management, Internet of Things (IoT) devices, intelligent transport systems, and other topics [6,14]. With the gradual deployment of 3GPP 5G NR commercial cells, both non-standalone (NSA) and standalone (SA), SDR-based transceivers can be used to implement a flexible wideband radio solutions, which can be deployed in any region, have common

radio management features, support various channel bandwidths, and can be used as O-RAN compliant white-box hardware [15].

To comply with the 3GPP 5G NR channel bandwidth requirements, transceivers used in eNodeB/gNodeB cells have to work over an extremely wide range of channel bandwidth options, ranging from 1.4 MHz up to 400 MHz, when both frequency range 1 (FR1) and frequency range 2 (FR2) is taken into account (excluding ultra-wideband carrier aggregation scenarios) [16,17]. Since 3GPP LTE/5G NR uses orthogonal frequency-division multiplexing (OFDM) scheme, the entire signal chain of the transceiver has to be designed with heavy focus on the linearity of the blocks to handle the high peak-to-average power ratio (PAPR) and avoid intermodulation distortion. These requirements dictate that channel selection filters must have variable bandwidth close to over two decades while maintaining good linearity and dynamic range parameters across the entire frequency range. Integrated LPF designed for SDR applications should also have configurable order of the filter to achieve best performance in respect to power, linearity, and channel selectivity [18]. Therefore, development of integrated transceiver blocks that meet the aforementioned requirements is very important for SDR technology.

### 1.3. Related Work

State-of-the-art LPFs usually target specific wireless communication systems with a limited configurable filter parameter set, mostly focused on bandwidth tuning. In most reported cases, bandwidth selection is limited to several pre-defined values and a tuning ratio not exceeding 10 [19,20]. Small signal linearity performance of wideband filters, expressed as in-band input-referred third-order intercept point (IIP3), is typically around 20 dBm. Reported linearity-related improvements, like feedforward compensation techniques in operational amplifiers, or use of additional active stages, can enhance linearity performance at the expense of power consumption and design complexity [20,21]. Furthermore, LPF parameters such as noise figure (NF), linearity performance, for both small and large signal conditions, are typically dependent on the settings of filter bandwidth, with no means of compensation [19,20,22].

Most of the reported flexible channel selection filters are based on active-RC or gm-C designs. While wideband designs can use gm-C filters, they are more suited for low power solutions, have poor linearity and dynamic range performance compared to active-RC designs [23]. Channel selection filter implementation typically does not exceed the 8th order, with most common values being 2nd, 4th, or 6th [20,24]. None of the reported filters have functionality to reconfigure order of the filter.

Although most of the reviewed filters use either a Butterworth or a Chebyshev approximation, there are reports of elliptical filter implementations for wideband low-pass filters [25]. While elliptical filters with transmission zero in stopband in theory could offer sharper transition from passband to stopband while maintaining a flat passband response, they require extreme gain-bandwidth product (GBWP) for large bandwidths to meet the specifications of passband linearity and have an accurate realization of the active-RC filter [22]. Implementations of wideband filters can suffer from PVT and hence complex tuning schemes are usually needed. Without precise calibration of quality factor (Q), elliptical filters can produce a response that deviates from the initial design, while still requiring additional elements to implement them [25].

In this work, a wideband reconfigurable integrated LPF for 5G NR compatible SDR solutions is designed and validated. The proposed LPF has programmable bandwidth and filter order, as well as process, voltage, temperature (PVT) compensation, and power management features. This article consists of four chapters. In the second chapter, LPF and operation amplifier design is presented. In the third chapter, post layout simulation results of the LPF are reported. The final chapter concludes the presentation.

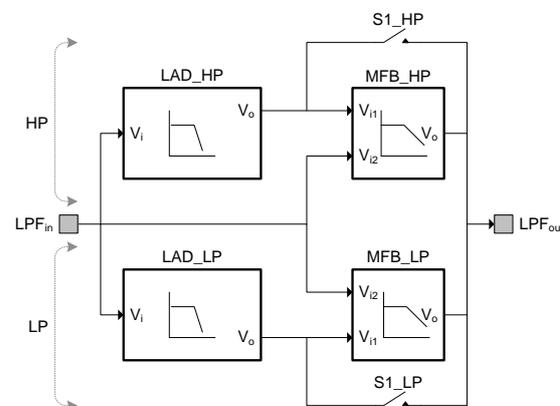
## 2. Design of Low-Pass Filter

### 2.1. Reconfigurable Structure of the Filter

A wideband reconfigurable integrated LPF for SDR transceivers has to cover bandwidths ranging from several to hundreds of megahertz. The proposed wideband reconfigurable integrated LPF is designed to have a bandwidth tuning range from 2.5 MHz to 200 MHz, which allows it to work with all 5G NR FR1 and FR2 and nearly all LTE bandwidth configurations, excluding 1.4 MHz and 3 MHz options [16,17].

The structure of the proposed wideband reconfigurable integrated LPF for SDR transceivers is shown in Figure 2. Due to high requirements for bandwidth tuning range, the LPF is split into two paths—low frequency path (LP) and high frequency path (HP), where each path can be tuned over a decade. Moreover, this approach of split LPF paths gives several advantages to the design:

1. Optimization of the active stage. This feature allows optimizing layout size and power dissipation for each path, since size and current consumption of the LP active stage can be scaled in respect to HP, while maintaining same performance.
2. Compensation of each stage over the entire tuning range for each path can be optimized for large signal response.
3. Count of passive elements of the tuning banks in the LPF can be distributed in both paths, which reduces the size of the bandwidth control step over the entire LPF tuning range for the same bit count of the control word. Hence, size of the control step can be reduced without adding additional parasitic capacitance due to a large number of switching elements.
4. If the design requires, LP and HP can be split into two separate and independently controlled LPFs that can work with narrow and wide bandwidths simultaneously, for example in 5G NR NSA implementation.



**Figure 2.** Structure of the proposed wideband reconfigurable integrated low-pass filter.

The configuration of the order of the proposed LPF is achieved by designing both LP and HP paths with two independently controlled, interconnected filter stages—a 2nd and a 4th order implementation with a low-pass response. As shown in Figure 2, they are respectively designated as MFB\_LP and LAD\_LP for LP path, and MFB\_HP and LAD\_HP for HP path. Each path can be configured to either one of the stages or their combination. This allows each path to be configured as 2nd, 4th, or 6th order LPF.

### Design of the Filter Stages

Active-RC topology is chosen for each stage of the filter, due to its high linearity and robustness with insensitivity to the parasitics compared to gm-C designs [18].

The 2nd and 4th order stages, respectively, use fully differential multiple feedback (MFB) topology and ladder filter (LAD) topologies. Their schematics are respectively shown in Figures 3 and 4. Since MFB topology uses a single operational amplifier (OA), as

opposed to two active stages in a biquad, it can be used for low power applications, while having excellent linearity performance. Ladder filter topology provides a more robust design for higher order filters against PVT.

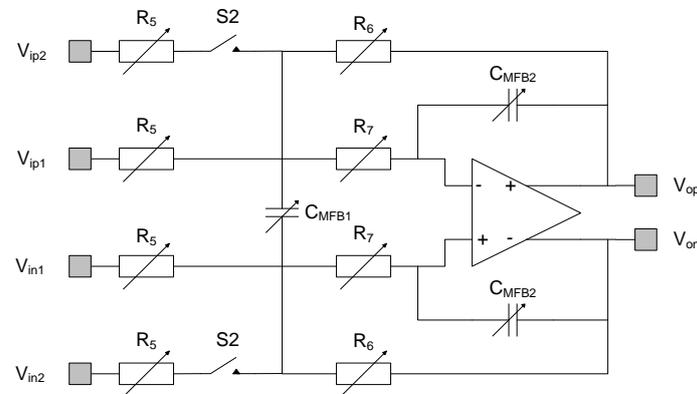


Figure 3. Schematic of 2nd order active-RC multiple feedback topology low-pass filter.

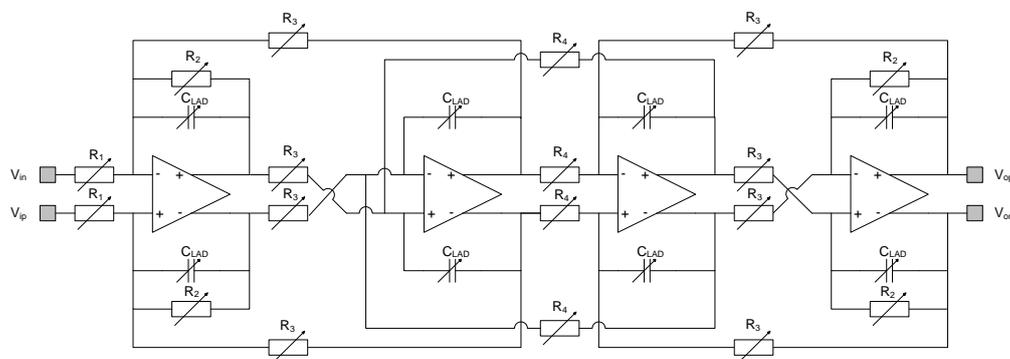


Figure 4. Schematic of 4th order active-RC ladder topology low-pass filter.

MFB stage has two differential inputs  $V_{ip1}$ ,  $V_{in1}$  and  $V_{ip2}$ ,  $V_{in2}$ . The first differential input is used when the active filter path is configured as a 6th order LPF, while the second differential input is used for 2nd order LPF configuration. This dual input approach removes the need to have two bypass transmission gates for each stage of the filter path—only the 2nd order stage is bypassed via a transmission gates under large signal conditions. These transmission gates in Figure 2 are marked as S1\_LP and S1\_HP for LP and HP paths, respectively. The S2 transmission gate in MFB topology (Figure 3) is placed at the summing node to achieve better linearity performance at large signal conditions.

Butterworth approximation is used for all stages in both LP and HP. Butterworth is chosen due to lower Q, which in turn relaxes OA gain–bandwidth product (GBWP) requirement. Furthermore, maximally flat passband response does not impact the signal-to-noise ratio (SNR) at large signal conditions, since minimal back off is not needed for margin against peaking in passband.

It can be noted that connecting a 2nd and 4th order filters of the proposed reconfigurable LPF in cascade produces a 6th order LPF transfer function (1), which is not equal to a 6th order Butterworth transfer function (2):

$$H(s) = 1 / \left( (s^2 + s/0.541 + 1) \times (s^2 + s/1.31 + 1) \right) \times 1 / (s^2 + s/0.707 + 1), \quad (1)$$

$$H(s) = 1 / \left( (s^2 + s/0.518 + 1) \times (s^2 + s/1.932 + 1) \times (s^2 + s/0.707 + 1) \right). \quad (2)$$

Cascading two filters with a Butterworth response retains the flatness in the passband, though if both 2nd and a 4th order filters have equal bandwidths, the overall path bandwidth will be reduced by ~14%, and have a slower roll-off around the transition band.

Designing each stage with a higher maximum bandwidth limit can counter the aforementioned bandwidth reduction. Looking at (3), increase of the bandwidth limit for both 2nd and 4th order filters allows to relax the requirements by about 20% for OA GBWP for the same bandwidth, compared to implementing a 6th order Butterworth transfer function. The small change of the roll-off near the transition band can be easily corrected in the digital domain by a channel equalizer, which can be found in most wireless communication systems [26].

$$\text{GBWP}_{\text{OA}} \approx 2 \times \omega_{\text{max}} \times Q/\Delta Q, \quad (3)$$

where  $\omega_{\text{max}}$  is the maximum passband frequency;  $Q$  is the maximum quality factor and  $\Delta Q$  is the tolerable quality factor variation for the filter [22].

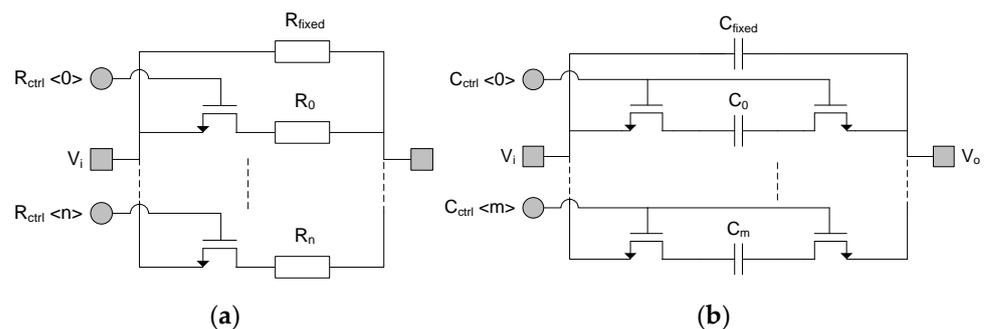
The requirement for OA GBWP can still be further reduced, if the bandwidth limit for the 2nd order filter is increased more than for the 4th order filter. In this scenario, the 2nd order filter would add additional signal suppression in stopband, while the 4th order filter would retain the near maximally flat response in the passband.

## 2.2. Calibration and Bandwidth Tuning

In the proposed filter structure, PVT induced variation and bandwidth tuning is implemented via digitally controlled resistor and capacitor tuning banks. Resistor banks are primarily used for IC process and temperature compensation, while capacitor banks are used to tune the bandwidth and to compensate for the residual, mostly constant, IC process parameter spread.

### 2.2.1. PVT Compensation

Resistor tuning banks in the 2nd and 4th order filters of both LP and HP paths use discrete-step tuning controls. They are composed of binary-controlled  $n$  number of MOS-switched resistors connected in parallel with a resistor of fixed value. The implementation of the resistor tuning bank with discrete control is shown in Figure 5a. The capacitor tuning bank utilizes the same structure, with a small modification for the  $C_{\text{MFB1}}$  bank (refer to Figure 3) of the 2nd order MFB filter, as shown in Figure 5b, where instead of one, two symmetrically placed MOS switches are used to equalize parasitic load on both summing nodes.



**Figure 5.** Schematic of: (a) resistor tuning bank with discrete control; (b) capacitor tuning bank with discrete control.

Careful selection of the quantity of the control bits for digital control of the resistor and capacitor tuning banks is important to minimize the total parasitic value from MOS switches. The value of the resistor  $R_{\text{fixed}}$  in the resistor tuning bank, as shown in (4), can be determined from the nominal value of the tuning bank  $R$  and the tuning range  $\Delta\omega$ , which is defined by the specific IC process and the desired margin. In this case, the minimum value of the resistance can be calculated from (5).

$$R_{\text{fixed}} = R \times (1 + \Delta\omega/100\%), \quad (4)$$

$$R_{\min} = R \times (1 - \Delta\omega/100\%), \quad (5)$$

where  $\Delta\omega$  is the bandwidth tuning range expressed in percentage. The resistance, which is needed to change the value of the resistor tuning bank by a maximum tuning step size  $\varphi_R$  can then be found:

$$R_p = 100\% \times (R_{\text{fixed}})^2 / (R \times \varphi_R) - R_{\text{fixed}}, \quad (6)$$

where  $\varphi_R$  is the maximum allowed tuning step size from the wanted frequency, expressed in percentage. The minimum number of MOS-switched resistors  $n$  needed to satisfy requirements of the tuning range  $\Delta\omega$  and tuning step size  $\varphi_R$  can be found using (7)–(9).

$$n = \begin{cases} \alpha, & \beta > 1 \\ \alpha + 1, & \beta \leq 1 \end{cases}, \quad (7)$$

$$\alpha = \lceil \log_2(2 \times R_{\text{fixed}} \times \Delta\omega / (R \times \varphi_R)) \rceil, \quad (8)$$

$$\beta = R_{\min} \times (R_{\text{fixed}} \times 2^\alpha + R_p) / (R_{\text{fixed}} \times R_p), \quad (9)$$

The values of the individual resistors in the tuning bank can then be found using (10).

$$R_n = R_p / 2^n. \quad (10)$$

A resistor bank with step size of 7% and 5-bit control is used in the proposed filter, which has a tuning range of 42%. The tuning range is derived from the corner models of the 65 nm node process, where value spread of both resistors and capacitors are taken into account.

### 2.2.2. Bandwidth Tuning

Similarly, the minimum number of MOS-switched capacitors  $m$ , which is needed to meet the requirements of the tuning range for maximum and minimum bandwidth, with a desired maximum step  $\varphi_C$  can be calculated from (11).

$$m = \lceil \log_2(\omega_{\max} / \omega_{\min} \times 100\% / \varphi_C) \rceil \quad (11)$$

where  $\omega_{\max}$  and  $\omega_{\min}$  are the maximum and minimum bandwidth, respectively, with bandwidth margins taken into account;  $\varphi_C$  is the maximum allowed step size from  $\omega_{\max}$ , expressed in percentage. The value of the smallest capacitor  $C_0$  can then be found as a ratio to  $C_{\text{fixed}}$ , using (12), while the values of the remaining capacitors are calculated in the same way as  $R_n$  using (10).

$$C_{\text{fixed}} / C_0 = \omega_{\min} \times (2^m - 1) / \omega_{\max} \quad (12)$$

For both proposed filter paths, the capacitor banks are designed with 8-bit control and  $C_{\text{fixed}} / C_0$  ratio of 22. The corresponding tuning ranges are 2.5–25 MHz and 20–200 MHz for the LP and HP path, respectively, with a 16%  $\omega_{\max}$  margin, and a 4.6%  $\varphi_C$ .

### 2.2.3. Calibration

The concept of calibration of the resistor tuning bank used for the LPF structure is shown in Figure 6. The calibration is done by comparing the value of an external temperature insensitive reference resistor  $R_{\text{ext}}$  to the value of an internal resistor bank  $R_{\text{int}}$ . The internal resistor bank  $R_{\text{int}}$  is designed to have nominal value equal to  $R_{\text{ext}}$  and same tuning specification as the resistor tuning bank in the LPF. Two internal stabilized current sources are used to create a voltage drop across both resistors, while a comparator is used to compare and tune the value of  $R_{\text{int}}$ .

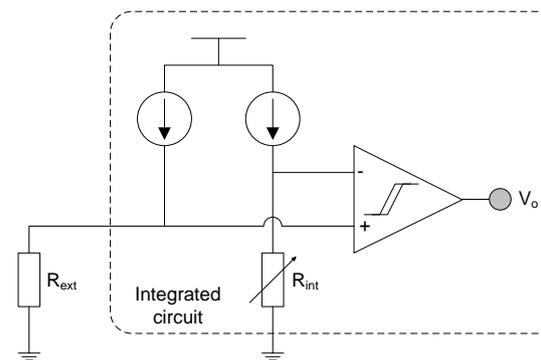


Figure 6. Structure of the resistor bank calibration.

Usually, direct transceiver architecture employs loopback-based direct channel calibration methods using a reference signal sweep to calibrate baseband induced imbalances, for example, amplitude and phase mismatches of the quadrature path signal [27]. Values of capacitors are much more stable over temperature compared to resistors, hence a single frequency sweep based on direct calibration can be used to determine the PVT-caused offset in the capacitor banks. Alternatively, dummy circuits can be added in the design to calibrate the value of the capacitor bank.

### 2.3. Operational Amplifier

Linear active stages are critical for any high linearity filter, since they are the most contributing sources of nonlinearity [21]. The structure of two-stage fully differential operation amplifier (FDOA), used for both LPF topologies, is shown in Figure 7. The FDOA is composed of two gain stages, an input differential pair stage ( $M_1$ – $M_5$ ) and an output stage ( $M_{13}$ – $M_{22}$ ), both of which are controlled by two common mode feedback (CMFB) loop amplifiers. The biasing of the input stage and the first CMFB loop amplifier ( $M_6$ – $M_{10}$ ) can be controlled by changing the value of current source  $I_{bias1}$ , which is mirrored and scaled by  $M_{11}$ . In a similar way, biasing of the output stage and second CMFB loop amplifier ( $M_{23}$ – $M_{27}$ ) can be controlled by  $I_{bias2}$ , which is mirrored and scaled by  $M_{12}$ . The first CMFB loop amplifier controls the bias point of the output stage via  $M_5$ .

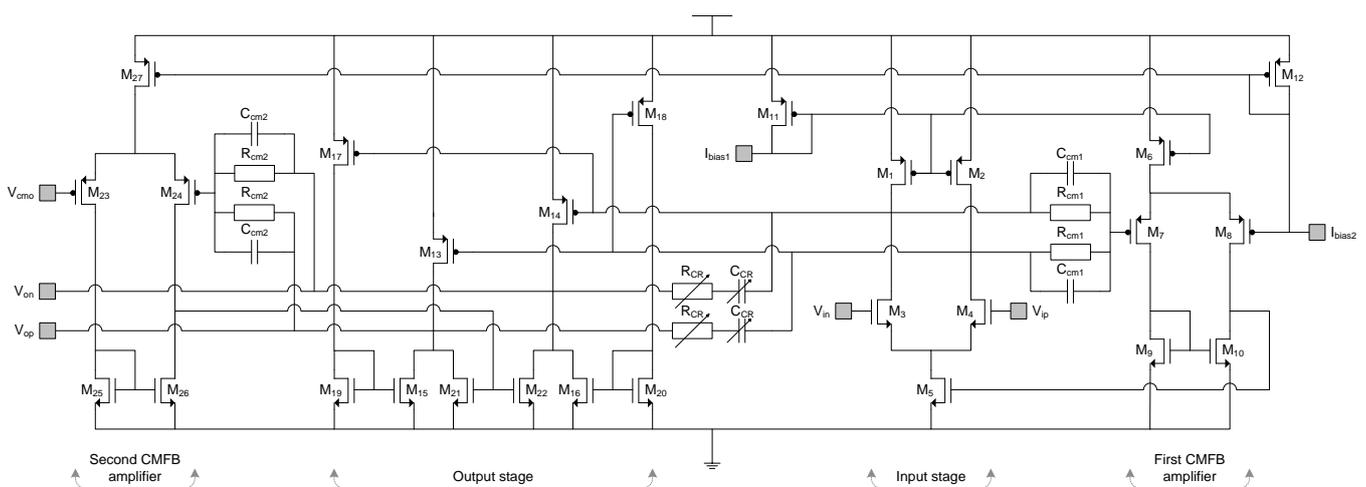


Figure 7. Schematic of the proposed fully differential operational amplifier for 2nd and 4th order low-pass filter topologies.

The output stage is designed to work in class-A configuration, where each single-ended output leg is driven by the differential output of the input stage. The voltage of the common mode output of the FDOA is set by  $V_{CM0}$  and controlled by the second CMFB

loop amplifier via  $M_{21}$ – $M_{22}$  in the output stage. In the designed filter, the  $V_{CMO}$  voltage is fixed to half of the supply voltage.

Passive RC common signal sense elements ( $R_{cm1}$ ,  $R_{cm2}$ ,  $C_{cm1}$ ,  $C_{cm2}$ ) are used between the input and output stage sensing nodes and the corresponding CMFB amplifier input for improved linearity performance, as opposed to using active elements. Miller compensation elements  $R_{CR}$  and  $C_{CR}$  are used between the input and output stages. The values of the resistor and capacitor are controlled using resistor and capacitor tuning banks, which have same structures as shown in Figure 5a. The corresponding control word of the LPF capacitor tuning bank is used to automatically select the required compensation values of the  $R_{CR}$  and  $C_{CR}$ .

When FDOA is powered down (circuitry is not show in Figure 7), the output stage is in a high-impedance state, where the impedance is mainly defined by the CMFB common signal sense and Miller compensation elements, if terminating switches are not present.

Control of  $I_{bias1}$  and  $I_{bias2}$  allows to change the GBWP of the FDOA at the expense of increased power consumption, without significantly affecting other FDOA parameters, such as gain and linearity. Thus, bias control enables power optimization of the FDOA at different filter bandwidth configurations, over a wide operation range.

LP and HP stages use same structure of the FDOA, but transistor sizing and driving strength are different to meet the different requirements for them. The FDOA in the 2nd and 4th order stages on the same path (LP or HP) are identical, only having subtle variations in the values of the  $R_{CR}$  and  $C_{CR}$  compensation bank.

### 3. Post-Layout Simulation Results

The proposed wideband reconfigurable integrated LPF was designed and verified using a 65-nm CMOS process. Layout of the designed filter in a quadrature baseband stage implementation is shown in Figure 8. The total occupied area for a single quadrature path is  $0.429 \text{ mm}^2$ , where LP and HP path occupy  $0.251 \text{ mm}^2$  and  $0.178 \text{ mm}^2$ , respectively. A single FDOA without Miller compensation elements occupies  $0.0035 \text{ mm}^2$  and  $0.0058 \text{ mm}^2$  in LP and HP path, respectively.

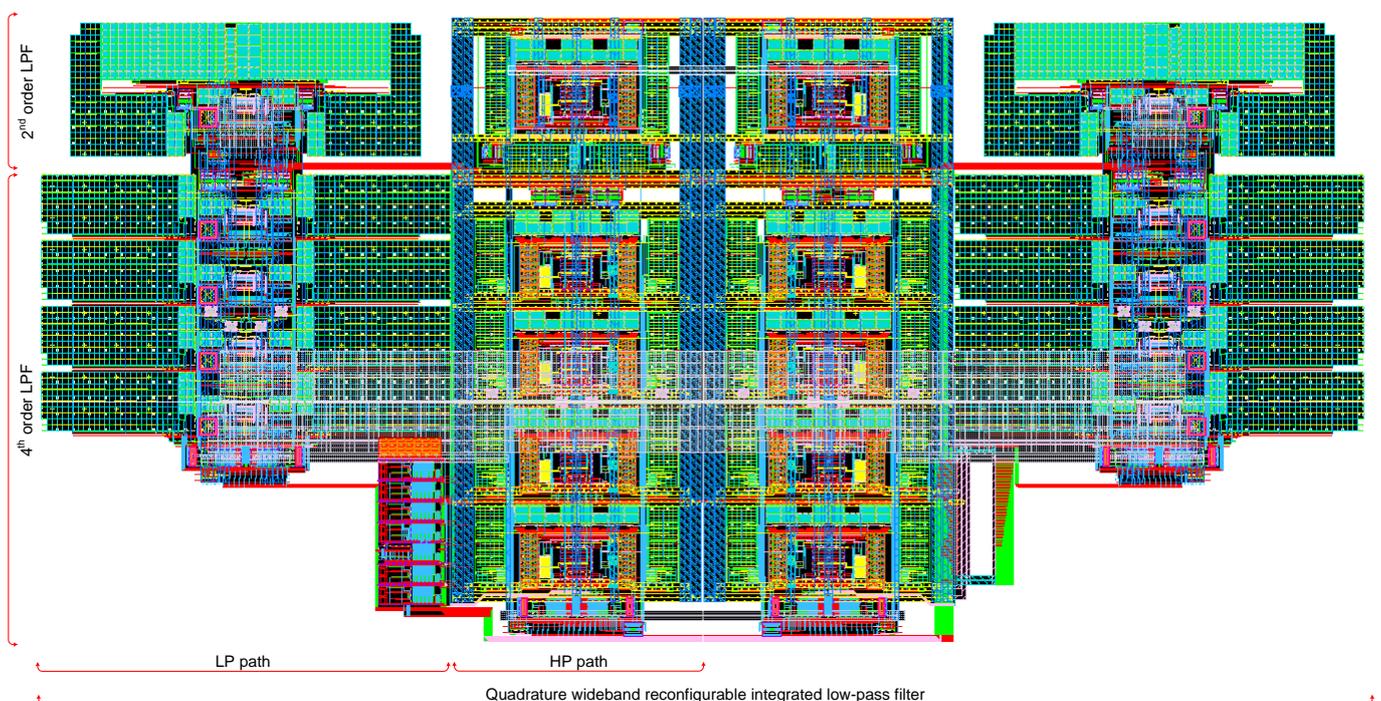
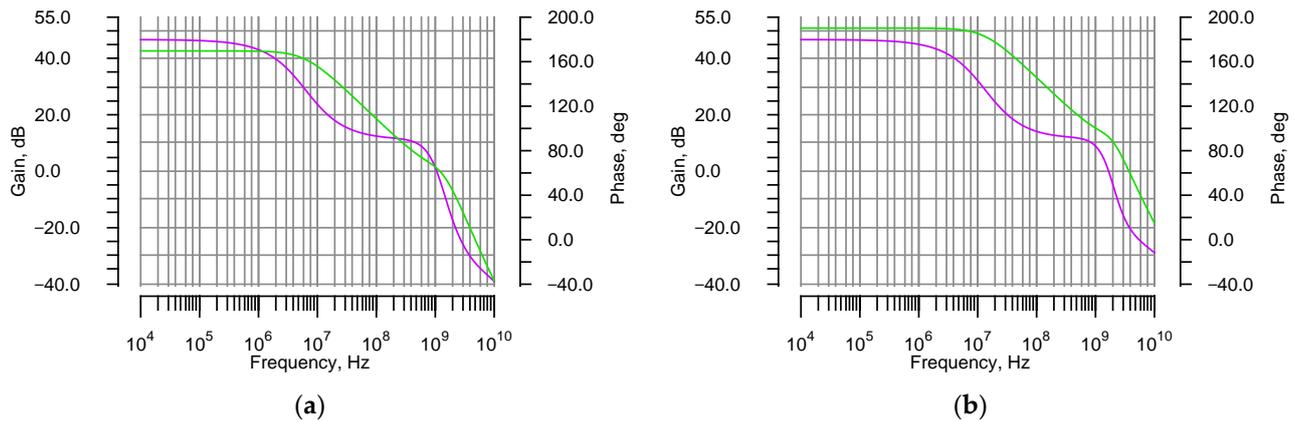


Figure 8. Layout of the wideband reconfigurable integrated low-pass filter in quadrature baseband configuration.

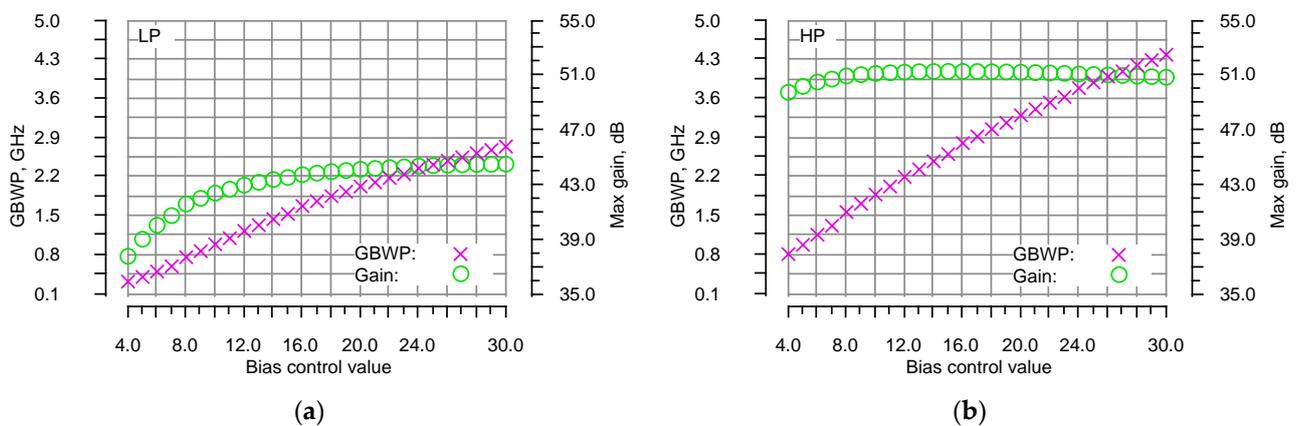
### 3.1. Operational Amplifier

In this section, results of post-layout simulation of the FDOA used in 2nd order filter are presented. Gain and phase response under nominal bias conditions of the LP and HP path FDOA is shown in Figure 9. The LP path FDOA has 43.1 dB gain, a phase margin of 50.8 degrees, and a bandwidth of 6.27 MHz, which equals a GBWP of 1.26 GHz. The power consumption is 2.32 mW from 1.2 V supply. Similarly, the HP path FDOA has 51.3 dB gain, a phase margin of 19.1 degrees, and a bandwidth of 7.59 MHz, which equals a GBWP of 2.22 GHz. The power consumption is 7.64 mW from 1.2 V supply.

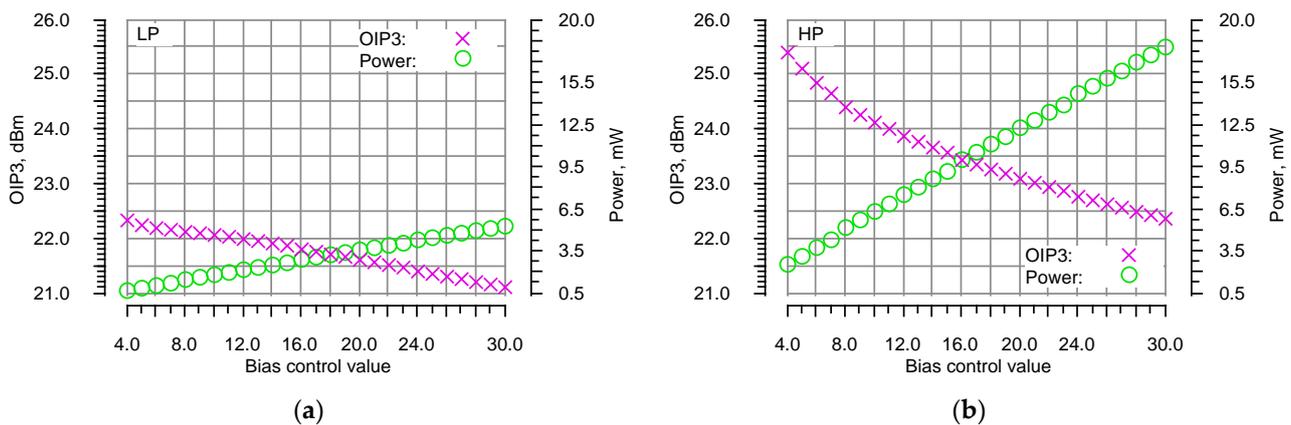


**Figure 9.** Gain and phase response under nominal bias conditions of the fully differential operational amplifiers used in 2nd order filter: (a) low frequency path (LP); (b) high frequency path (HP).

FDOA gain–bandwidth product, maximum passband gain, in-band output-referred third-order intercept point (OIP3) and power consumption at different bias control values are shown in Figures 10 and 11. By changing the value of the bias control, power consumption can be used as a trade-off to change the GBWP of FDOA and optimize performance of the filter for different bandwidth settings. For LP and HP paths, respectively, the GBWP can be changed from 0.36 GHz to 2.7 GHz and from 0.85 GHz to 4.4 GHz. The change of bias has a small impact on other FDOA parameters. For LP path, the gain varies from 38 dB to 44.6 dB, the OIP3 from 22.4 dBm to 21.15 dBm, while for HP path, the gain varies from 49.8 dB to 51.3 dB, the OIP3 from 25.4 dBm to 22.4 dBm across the bias control range.



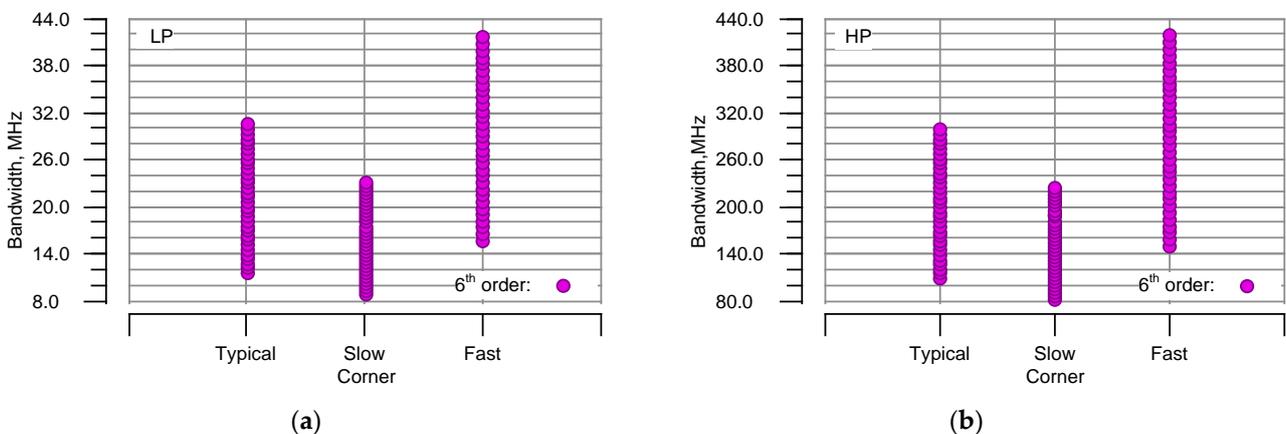
**Figure 10.** Gain–bandwidth product (GBWP) and maximum gain response at different bias control values of the fully differential operational amplifiers used in 2nd order filter: (a) low frequency path (LP); (b) high frequency path (HP).



**Figure 11.** In-band output-referred third-order intercept point (OIP3) and power consumption at different bias control values of the fully differential operational amplifiers used in 2nd order: (a) low frequency path (LP); (b) high frequency path (HP). OIP3 input tone configuration: 1 MHz and 1.7 MHz, both tone amplitude  $-10$  dBm.

### 3.2. Low-Pass Filter

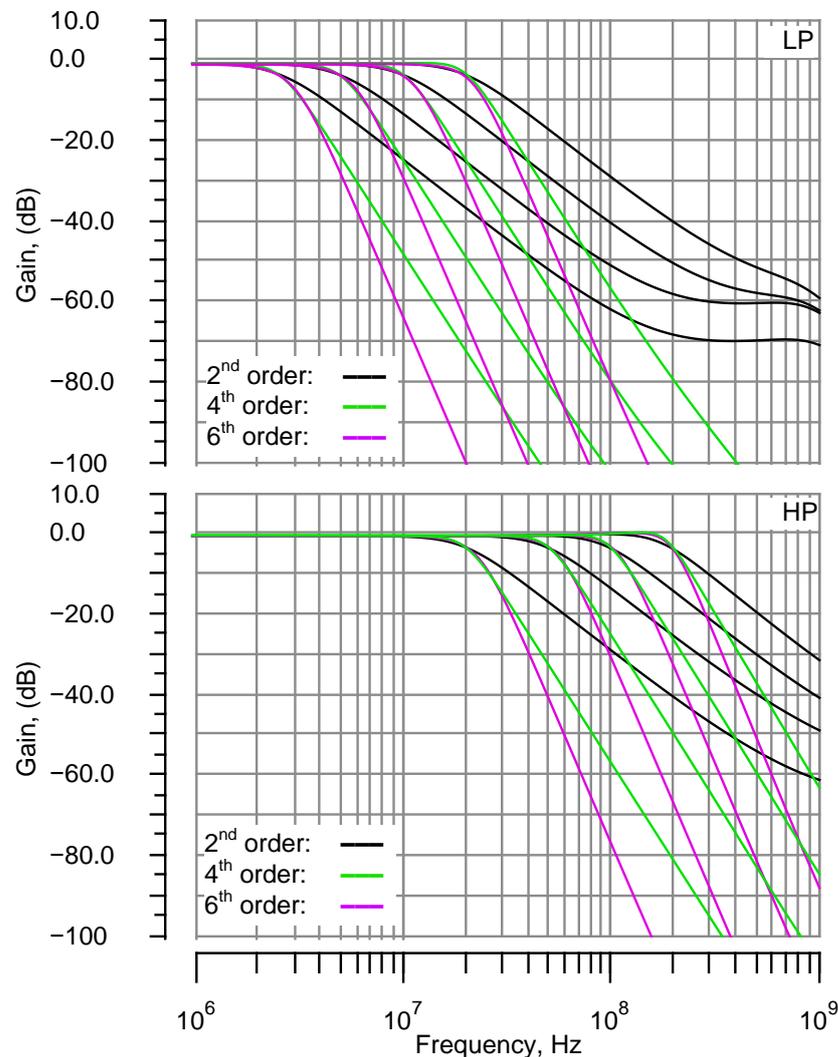
In this section, results of the post-layout simulation of the proposed wideband reconfigurable integrated LPF at different filter order and bandwidth configuration sets are presented. The tuning range of the resistor bank of the 6th order filter, a cascade of 2nd and 4th order filters, for both LP and HP can be seen in Figure 12. As seen from the overlapping bandwidth tuning ranges, resistor bank based frequency tuning is sufficient to compensate bandwidth offset related to technology process corner with a minimum tuning word margin of 5.



**Figure 12.** Bandwidth tuning range at different technology process corners for the 6th order configuration: (a) low frequency path (LP), configured for 20 MHz bandwidth; (b) high frequency path (HP), configured for 200 MHz bandwidth.

The filter response for all three configurations of the LPF order at various corner and intermediate bandwidth configurations is shown in Figure 13. The gain varies from  $-0.55$  dB to  $-0.84$  dB with a maximum passband ripple of 0.1 dB for the LP across the entire bandwidth tuning range and for all configurations of the filter order. For the same HP configuration, the gain varies from  $-0.26$  dB to  $-0.48$  dB with a maximum passband ripple of 0.75 dB. The small negative gain is caused by resistor bank parameter variations in filter topologies, internal resistance of the transmission gates, and by finite gain of the FDOA. It is possible to compensate this by adding a separate control for either the  $R_1$  and  $R_5$  or the  $R_3$  and  $R_4$  pairs (see Figures 3 and 4). Since margin of the tuning word is at least 5, an offset value for the selected pair can be added when tuning the bandwidth to

compensate the gain variation of the LPF. Lastly it can be noted that the gain control in typical SDR transceivers is implemented by using VGA stages before or after the LPF.

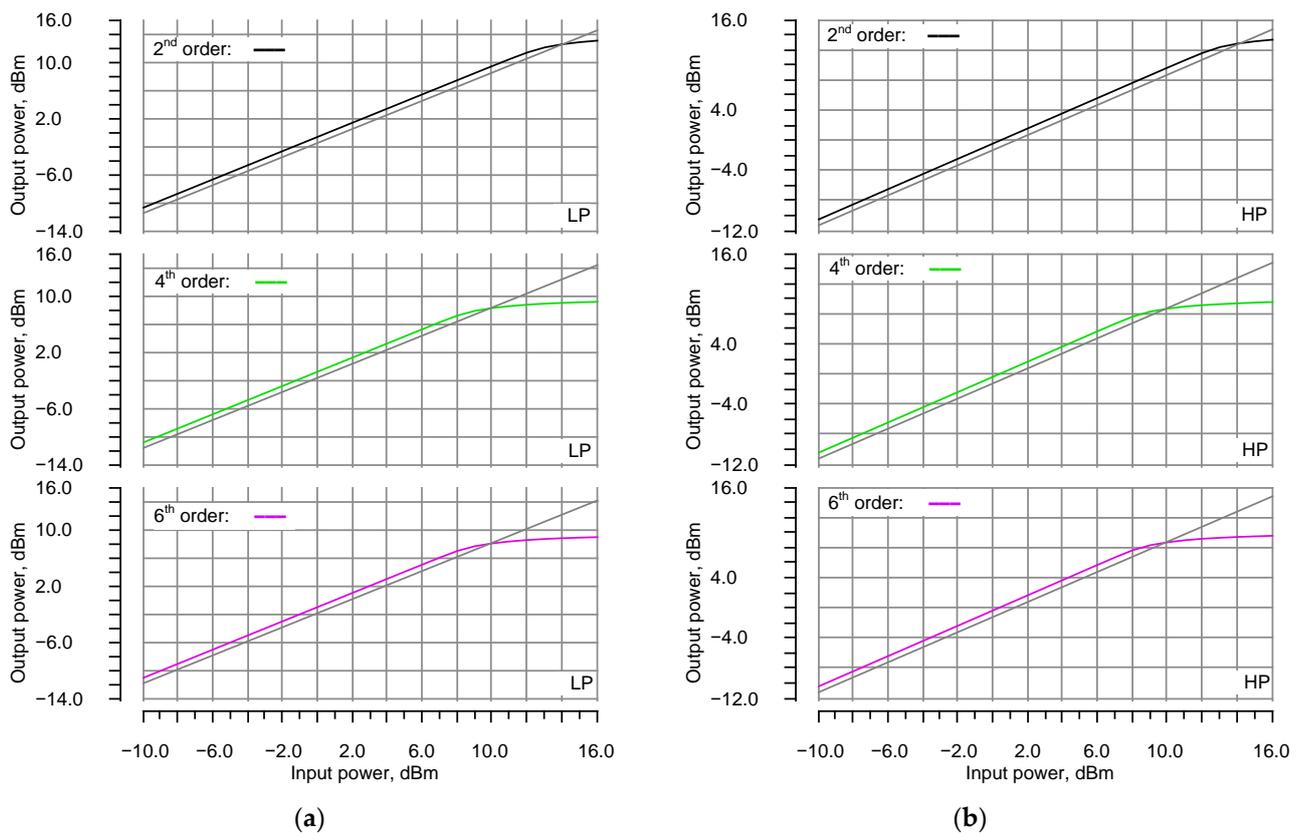


**Figure 13.** Low frequency path (LP) and high frequency path (HP) response for all order configurations, tuned to 2.5 MHz, 5 MHz, 10 MHz, 20 MHz, 50 MHz, 100 MHz, and 200 MHz.

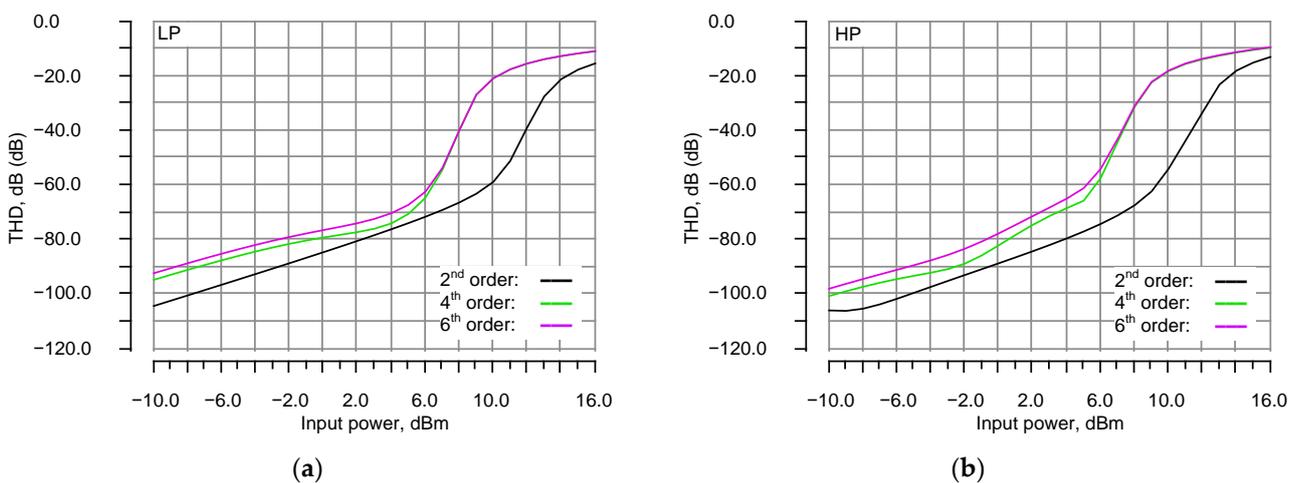
1 dB compression point ( $P_{1dB}$ ) for all three configurations of the filter order for LP and HP is shown in Figure 14. The 2nd order stage has a  $P_{1dB}$  of 14.1 dBm, while the compression point of the 4th order stage is 9.9 dBm for both LP and HP. Due to cascaded structure of the 6th order configuration, its  $P_{1dB}$  value is determined by the most nonlinear stage, and therefore it has the same value as the 4th order stage.

Since the capacitor bank are used in the filter for bandwidth selection and minimum bandwidth of the filter is well above the  $1/f$  noise corner, LPF has small NF variation at same load conditions over the entire range of bandwidth control. Due to aforementioned small variations in NF and  $P_{1dB}$ , large signal dynamic range per hertz of the proposed filter is nearly invariant to different sets of bandwidth and order configurations.

Total harmonic distortion (THD) for LP and HP is shown in Figure 15. If LP is configured for 20 MHz, THD values for 2nd, 4th and 6th filter order configuration vary from  $-103.1$  dB to  $-91.7$  dB with a  $0.2 V_{pp}$  input and from  $-75.7$  dB to  $-69.9$  dB with a  $1 V_{pp}$  input. One percentage THD is reached with 12 dBm for 2nd filter order and 8 dBm level input signal for 4th and 6th filter order.



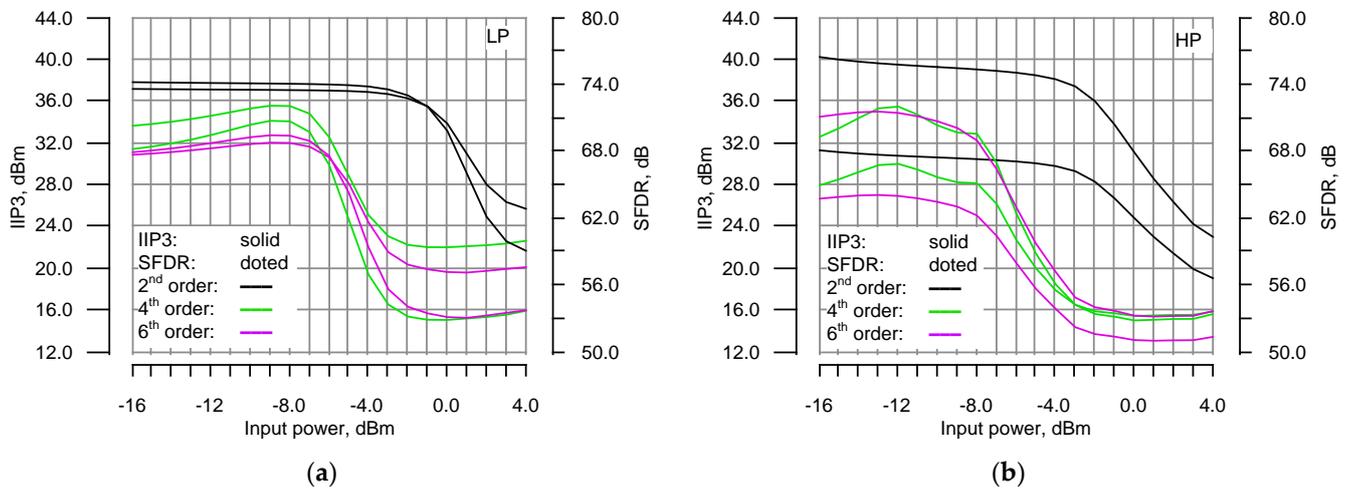
**Figure 14.** 1 dB compression point ( $P_{1dB}$ ) for all filter order configurations: (a) low frequency path (LP), configured for 20 MHz bandwidth; (b) high frequency path (HP), configured for 200 MHz bandwidth. Input tone frequency: 10% of bandwidth.



**Figure 15.** Total harmonic distortion (THD) at different input power levels for all filter order configurations: (a) low frequency path (LP), configured for 20 MHz bandwidth; (b) high frequency path (HP), configured for 200 MHz bandwidth. Input tone frequency: 10% of bandwidth.

When HP is configured for 200 MHz, values of the THD for the same configurations of the filter order vary from  $-105.5$  dB to  $-97.4$  dB with a  $0.2 V_{pp}$  input and from  $-79.1$  dB to  $-64.6$  dB with a  $1 V_{pp}$  input. One percentage THD is reached with  $11.3$  dBm for 2nd filter order and  $7.2$  dBm level input signal for 4th and 6th filter order.

In-band input-referred third-order intercept point (IIP3) and spurious free dynamic range (SFDR) for LP and HP is shown in Figure 16. If LP is configured for 20 MHz, values of the IIP3 and SFDR for 2nd, 4th and 6th filter order configurations, respectively, vary from 32.7 dBm to 37.8 dBm and from 68.75 dB to 73.6 dB with 0.2 V<sub>pp</sub> tones.



**Figure 16.** In-band input-referred third-order intercept point (IIP3) and spurious free dynamic range (SFDR) at different input power levels for all filter order configurations: (a) low frequency path (LP), configured for 20 MHz bandwidth; (b) high frequency path (HP), configured for 200 MHz bandwidth. IIP3 input tone configuration: first at 40%, second at 70% of bandwidth, both tone amplitude  $-10$  dBm.

When HP is configured for 200 MHz, values of the IIP3 and SFDR for 2nd, 4th and 6th filter order configurations, respectively, vary from 34.2 dBm to 39.3 dBm and from 63.59 dB to 67.56 dB with 0.2 V<sub>pp</sub> tones.

The results for key sets of LPF configuration are summarized in Table 1 and a comparison to previous works is presented in Table 2. Comparing the results, it can be seen, that the proposed filter has the best in-band IIP3 and THD parameters. Although the reported filter [20] has excellent NF and large signal distortion performance, it has to be noted that this is achieved by utilising input and output buffer stages with source and load matching. Comparing integrated noise and large signal dynamic performance (P<sub>1dB</sub>) of the proposed filter, it can be seen that it also has better parameters of the remaining lot.

**Table 1.** Summary of the designed wideband reconfigurable integrated low-pass filter parameters.

Path	Low Frequency Path (LP)						How Frequency Path (HP)							
Technology	65 nm CMOS													
Supply, V	1.2													
Tuning ratio	11.6						92.8							
Topology <sup>1</sup>	MFB		LAD		MFB + LAD		Active-RC		MFB		LAD		MFB + LAD	
Type <sup>2</sup>	LPF-B		LPF-B		LPF-C-B		LPF-B		LPF-B		LPF-B		LPF-C-B	
Order	2nd		4th		6th		2nd		4th		6th		6th	
Area, mm <sup>2</sup>	0.073		0.172		0.251		0.044		0.131		0.178		0.178	
Gain, dB	-0.55		-0.57		-0.84		-0.48		-0.26		-0.39		-0.39	
P <sub>1dB</sub> , dBm	14.06		9.95		9.94		14.2		9.94		9.94		9.94	
Bandwidth, MHz	2.5	20	2.5	20	2.5	20	20	200	20	200	20	200	20	200
In-band IIP3, dBm <sup>3</sup>	38.84	38.58	36.32	35.51	35.05	34.83	45.81	44.61	37.61	37.94	36.03	36.72	38.48	37.79
Out-band IIP3, dBm <sup>4</sup>	38.94	36.98	28.19	24.32	25.66	22.17	35.72	37.37	32.57	20.66	30.21	16.06	38.42	34.16
SFDR, dB <sup>3</sup>	79.45	74.13	78.46	73.04	75.47	70.2	79.32	71.07	75.12	68.57	71.52	65.29	79.21	73.6
			77.58	71.94	74.31	68.75	76.73	67.56	74.58	65.76	73.12	63.59		

Table 1. Cont.

Path	Low Frequency Path (LP)						How Frequency Path (HP)					
THD, dB <sup>5</sup>	−105 −76.95	−103.7 −75.7	−95.1 −74.75	−94.16 −73.57	−92.3 −72.11	−91.74 −69.85	−112.4 −85.63	−105.5 −79.06	−104.4 −71.64	−100.1 −68.04	−101.2 −69.22	−97.39 −64.55
NF, dB	29.65	28.34	28.62	26.9	31.83	30.48	27.78	28.95	25.87	26.05	29.7	29.74
Intg. Noise, $\mu\text{V}_{\text{RMS}}$ <sup>6</sup>	21.88	52.8	19.82	45.31	28.45	67.72	49.43	182.2	40.19	132.3	62.13	202.7
Noise Floor, dBm	−80.35	−72.63	−78.17	−70.48	−78.17	−70.48	−73.19	−62.02	−75.08	−64.92	−71.26	−61.23
Dynamic range, dB <sup>7</sup>	94.26	86.54	91.18	83.87	87.96	80.28	87.24	76.07	84.89	74.71	81.06	71.02
Dynamic range, dB-Hz <sup>8</sup>	92.2	84.48	89.23	81.92	86.02	78.34	84.34	73.17	82.15	71.97	78.35	68.28
Power, mW	158.24	159.55	155.16	156.88	151.94	153.29	160.25	159.08	157.9	157.72	154.07	154.03
	1.19	2.31	4.98	9.5	6.2	11.8	3.9	14.8	15.9	58.6	19.8	73.4

<sup>1</sup> MFB—multiple feedback topology; LAD—ladder topology. <sup>2</sup> LPF-B—Butterworth; LPF-C-B—cascaded Butterworth. <sup>3</sup> Upper numbers with input tone configuration: first at 10%, second at 19% of bandwidth, both tone amplitude −10 dBm; lower numbers with input tone configuration: first at 40%, second at 70% of bandwidth, both tone amplitude −10 dBm. <sup>4</sup> Input tone configuration: first at 150%, second at 250% of bandwidth, both tone amplitude −10 dBm. <sup>5</sup> Upper numbers with −10 dBm input tone; lower numbers with 4 dBm input tone. <sup>6</sup> Integrated from 1 kHz to Bandwidth. <sup>7</sup> Upper numbers at  $P_{1\text{dB}}$  value; lower numbers at 1% THD value. <sup>8</sup>  $P_{1\text{dB}}/(k \times T \times \text{Noise Factor})$  [22].

Table 2. Summary of the designed wideband reconfigurable integrated low-pass filter parameters.

	[19] <sup>3</sup>	[24] <sup>4</sup>	[20] <sup>5</sup>	[28] <sup>6</sup>	This Work <sup>7</sup>	
Process	130 nm CMOS	28 nm CMOS	180 nm CMOS	180 nm CMOS	65 nm CMOS	
Supply, V	0.6	1.1	1.8	1.8	1.2	
Tuning ratio	4	N/A	9	N/A	92.8	
Topology <sup>1</sup>	A-RC	gm-C	A-RC	A-RC/A-gm-RC	A-RC	
Type <sup>2</sup>	C-BQ	-	SK-BQ	FLFB	MFB + LAD	
Order	LPF-B	LPF-B	LPF	LPF-B	LPF-C-B	
Bandwidth, MHz	4th	6th	2	4	2.5	200
Area, mm <sup>2</sup>	20–160	50	50–450	22.5	0.429	
Gain, dB	0.236	0.2	0.5	0.35	0.429	
$P_{1\text{dB}}$ , dBm	0	−5.8	0	0.5	−0.84	−0.39
In-band IIP3, dBm	6.96–4.26	2.8, 4.5	12	8.5	9.94	9.94
Out-band IIP3, dBm	21–9.56	18, 16.5	27–24	21.5, 9	35.05	36.72
SFDR, dB	17.4–9.7	-	-	-	25.66	16.06
THD, dB	66.6–50.7	−42.5	-	-	75.47	65.29
NF, dB	66.2–50.7	−40	-	−40, −30	−72.11	−64.55
Intg. Noise, $\mu\text{V}_{\text{RMS}}$	-	-	15	-	31.83	29.74
Dynamic range, dB	243–520	277	-	87	28.45	202.7
Power, mW	64.2–51	-	93.84–84.30	63	86.02	68.28
	5.56–23.77	3.63	25.2	12.6	6.2	73.4

<sup>1</sup> A-RC—active RF; C-BQ—cascaded biquad; SK-BQ—Sallen-Key biquad; FLFB—follow-the-leader-feedback; MFB—multiple feedback topology; LAD—ladder topology. <sup>2</sup> BPF-CH—bandpass filter, Chebyshev; LPF-B—Butterworth; LPF-C-B—cascaded Butterworth. <sup>3</sup> In-band IIP3 frequencies for 20 MHz were 6 MHz and 7 MHz, for 160 MHz—48 MHz and 56 MHz; Intg. Noise integrated from 1 to Bandwidth; Dynamic range at 1% THD. <sup>4</sup>  $P_{1\text{dB}}$ , at 10 MHz and 40 MHz; In-band IIP3 frequencies 10 MHz and 11 MHz, 40 MHz and 41 MHz; SFDR is in dBc, with 40 MHz and 41 MHz, −5 dBm input tones; THD is in dBc, with an input tone 10 MHz, 1 dBm, includes up to 5th harmonics. <sup>5</sup> Uses Low noise amplifier—Source Follower—LPF—Output buffer configuration. Designed with 50 $\Omega$  resistor banks, therefore low NF value at expense of area and power. In-band IIP3 frequencies 40 MHz and 50 MHz, 290 MHz and 300 MHz at 50 MHz and 300 MHz, −4 dBm input tones. <sup>6</sup>  $P_{1\text{dB}}$ , at 5 MHz; In-band IIP3 frequencies 5 MHz and 6 MHz, 20 MHz and 21 MHz; THD is in dBc, input tone 2 MHz and 10 MHz, 0.33  $V_{0\text{-Peak}}$ . <sup>7</sup> See Table 1 for conditions.

#### 4. Conclusions

In this work, a wideband reconfigurable integrated LPF for 5G NR compatible SDR solutions was designed and validated. The LPF has programmable bandwidth with 92.8 tuning ratio—from 2.5 MHz to 200 MHz. This is achieved by connecting two overlapping frequency paths that are connected in parallel, both using Active-RC topology. The order of the filter can be configured to realize a 2nd, 4th, or 6th order LPF function, it has built-in PVT compensation with a tuning range of  $\pm 42\%$  and power management features, which enable optimization of the filter across its entire bandwidth tuning range.

The LPF was designed and verified using 65 nm CMOS process, it occupies 0.429 mm<sup>2</sup> and uses a 1.2 V supply. Across the entire 2.5 MHz to 200 MHz bandwidth selection range

of the LPF, in-band IIP3 varies between 32.7 dBm and 45.8 dBm. Similarly, THD value varies between  $-85.63$  dB and  $-64.55$  dB when amplitude of the input tone is 4 dBm. One percentage THD is reached when the level of the input signal is 11.3 dBm for 2nd filter order and 7.2 dBm for 4th and 6th filter orders. The large signal performance of the LPF is stable across its bandwidth tuning range— $P_{1dB}$  is equal to 14 dBm when the LPF is configured for 2nd order and 10 dBm when LPF implements a 4th and 6th order functions. Depending on the filter's order and bandwidth configuration, power dissipation can vary between 1.2 mW and 73.4 mW. Power management and performance optimization is achieved by utilizing two biasing controls of the operational amplifier for different sets of filter configuration.

The best small signal linearity performance is achieved, when the LPF is configured for 2nd order multiple feedback topology, where in-band IIP3 and THD mean values across the entire range of bandwidth selection are respectively 39 dBm and  $-79$  dB. Due to small variations in NF and  $P_{1dB}$ , large signal dynamic range per hertz of the proposed filter is nearly invariant to different sets of bandwidth and order configurations.

As a future step, the designed LPF will be used as part of an analog baseband chain of SDR transceiver in both transmit and receive paths. The use cases for aforementioned SDR transceiver will be primarily targeted at Intelligent Transport Systems, which utilise a variety of different wireless standards, including 5G NR.

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**Conflicts of Interest:** The authors declare no conflict of interest.

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