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History Erase Effect of Real Memristors

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Abstract: Different from the static (power-off) nonvolatile property of a memristor, the history erase effect of a memristor is a dynamic characteristic, which means that under the excitation of switching or different signals, the memristor can forget its initial value and reach a unique stable state. The stable state is determined only by the excitation signal and has nothing to do with its initial state. The history erase effect is a desired effect in memristor applications such as memory. It can simplify the complexity of the writing circuit and improve the storage speed. If the memristor's response depends on the initial state, a state reset operation is required before each writing operation. Therefore, it is of great theoretical and practical significance to judge whether the memristor has a history erase effect. Based on the study of the history erase effect of real memristors, this paper focuses on the history erase effect of a Hewlett-Packard (HP) TiO_2 memristor and the Self-Directed Channel (SDC) memristor of Knowm Company. The DC and AC responses of the HP TiO_2 memristor are given, and it is pointed out that there is no AC history erase effect. However, considering the parasitic memcapacitance effect, it is found that it has the effect. Based on the theoretical model of the SDC memristor, its history erase properties with and without considering parasitic effects are studied. It should be noted that this study method can be useful for other materials such as Al_2O_3 and MoS_2.

Keywords: memristor; history erase effect; dynamic route; power-off plot

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1. Introduction

A memristor has many unique properties, such as a simple physical structure, easy high-density integration, nonvolatility, historical behavior, low power consumption, and good scaling, which have attracted the extensive attention of scientists and researchers [1–3]. However, unlike other important inventions and discoveries throughout history, the memristor was first proposed as a theoretical concept. In 1971, Chua proposed the memristor as the fourth basic circuit element in his groundbreaking paper "Memristor: The Missing Circuit Element" [4]. In his paper, starting from the basic theory of circuits, professor Chua pointed out that just as resistance links voltage and current, capacitance links charge and voltage, and inductance links magnetic flux and current, there must be a fourth basic circuit element that links charge and magnetic flux. He considered this kind of element a memory resistor and coined the term memristor. He proved that this kind of element is not equivalent to any circuit consisting of the simple connection of the other three basic circuit elements; thus, it is a new basic circuit element. Since then, for more than 30 years, research on memristors has been limited to a few circuit theorists. It was not until 2008 that Dmitri [5] and others of Hewlett-Packard (HP) laboratories announced that nanomemristor devices had been manufactured artificially. Memristors returned to the public's attention and thus ushered in the upsurge of memristor research. Since 2008, a number of papers have been published in peer-reviewed journals involving memristor manufacturing and memristor applications in different scientific and technological fields [6–8].

Since memristors are extensively used as memory devices, the study of their switching dynamics is timely and interesting. The motivation of this paper is, by studying one of a memristor's properties, the history erase effect, to provide useful information

both theoretically and practically to guide scientists and engineers toward improving device performance.

Boyd introduced the concept of history erase in 1985 [9], but his strict mathematical definition was abstract and difficult to apply. Until 2016, Ascoli studied a tantalum dioxide memristor at HP laboratories using the concept of history erase and described it in a popular way [10]. After that, Tezlaff et al. [11,12] studied the local history erase effect of bistable memristors. In 2017, Menzel et al. [13] analyzed the origin of the history erase effect in ReRAM. In the same year, Ascoli et al. [14] analyzed its historical erasure effect by means of a closed analytical solution of the dynamic characteristics of the TaO memristor switch. In 2018, Ascoli, Tetzlaff, and Menzel published a summary [15]. Based on the circuit theory model, the history erase effect of a variety of practical memristors was studied.

In fact, the history erase effect describes the dynamic characteristics of memristors, which should be distinguished from their static nonvolatile memory characteristics. The so-called nonvolatility of the memristor refers to the state before power off is memorized when the power supply is cut off. The behavior of the memristor can be described by the power-off plot (POP). The history erase effect refers to the property that the memristor can forget its initial value under the excitation of the switching signal and reach its unique stable state after a period of time. This state is only determined by the excitation signal and is independent of the initial state of the memristor. Therefore, the history erase effect is a desired effect that can simplify the complexity of the writing circuit of the memory and improve the storage speed. If the memristor has no history erase effect and its response depends on the initial state, there is still an operation of state clearing before each writing operation. It is undoubtedly ideal to avoid such additional overhead.

Based on the above understanding, this paper studies the history erase effect of two practical memristor devices, namely the HP TiO_2 memristor and the Knowm self-aligning channel memristor. The authors found that the HP TiO_2 memory device has no history erase effect under AC signal excitation, but because of its parasitic memcapacitance, it leads to the history erase phenomenon in the actual device. As a supplement to this study, the authors also studied the latest commercial memristor device, the discrete Self-Directed Channel (SDC) memristor of Knowm Company [16–19]. There is no suitable model description for this kind of memristor. Therefore, the author first used the generic VTEAM model [20,21] to fit the characteristic curve of the memristor measured from the experiment, followed by the optimization method of simulated annealing to determine the model parameters. The history erase property of the SDC memristor is then studied by using the VTEAM model, and it is found that it has this effect.

Section 2 describes the concept of the history erase effect and points out that the ideal general memristor device does not have the history erase property. Section 3 studies the historical erase characteristics of the HP TiO_2 memristor and discusses the influence of the parasitic effect on the performance of the device. Section 4 studies the modeling and history erase effect of the discrete SDC memristor of Knowm Company. Finally, the conclusion of this paper is given in Section 5.

2. History Erase Effect of the Ideal Generic Memristor

It should be noted that not all memristors have a history erase effect. For example, it can be proved that the ideal generic memristor does not have a history erase effect. The lack of history erase effects in ideal generic memristors was already revealed in [10]; however, we rederive the results here by another method.

For the ideal generic memristor, the definition equation is as follows:

$$\frac{dx}{dt} = g(x)v_m \tag{1}$$

$$i_m = G(x)\, v_m \tag{2}$$

where x is the state variable, and v_m and i_m are the voltage and current across both ends of the memristor, respectively. $G(x)$ is the memconductance, and $g(x)$ is a function of state x.

Note that in (1), if $g(x) = 0$, then $dx/dt = 0$, $x = x_0$. Then, the response of the memristor depends on the initial state (we assume $G(x_0) \neq$ constant). If $g(x) \neq 0$, for (1), the variables are separated and the two sides are integrated, then we obtain:

$$\varphi_m = \varphi_{m0} + \int_0^x \frac{1}{g(x)} dx \tag{3}$$

Obviously, the memristor flux response φ_m is related to the initial state φ_{m0}, hence the memristor has no history erase effect.

3. HP TiO_2 Memristor

The HP TiO_2 memristor was invented by Strukov et al. of HP laboratories in 2008 [5,22]. Its linear ion drift model is as follows:

$$\begin{cases} v_m(t) = (R_{ON}\frac{w(t)}{D} + R_{OFF}(1 - \frac{w(t)}{D}))i_m(t) \\ \frac{dw(t)}{dt} = \mu_V \frac{R_{ON}}{D} i_m(t) \end{cases} \tag{4}$$

where $w(t)$ is the width of the doping region, D is the length of the device, R_{OFF} is the resistance value when the device is completely off, R_{ON} is the resistance value when the device is fully on, μ_V is the ion mobility, and v_m and i_m are the voltage and current of the device, respectively. Considering the dimensional limitation of the actual device, Equation (4) should be modified as follows:

$$\frac{dw(t)}{dt} = \begin{cases} \mu_V \frac{R_{ON}}{D} i_m(t) & w(t) \in (0, D) \text{ or } (w(t) = D, v_m(t) < 0) \text{ or } (w(t) = 0, v_m(t) > 0) \\ 0 & (w(t) = D, v_m(t) \geq 0) \text{ or } (w(t) = 0, v_m(t) \leq 0) \end{cases} \tag{5}$$

By substituting the current in Equation (5) with voltage, the following results can be obtained:

$$\frac{dw(t)}{dt} = \begin{cases} \mu_V \frac{R_{ON}}{D} \frac{v_m(t)}{(R_{ON}\frac{w(t)}{D} + R_{OFF}(1 - \frac{w(t)}{D}))}, & w(t) \in (0, D) or (w(t) = D, v_m(t) < 0) \\ & \text{or } (w(t) = 0, v_m(t) > 0); \\ 0 & (w(t) = D, v_m(t) \geq 0) \\ & \text{or } (w(t) = 0, v_m(t) \leq 0) \end{cases} \tag{6}$$

In Equation (6), if the parameters of the equation are assigned according to the data in Strukov's original paper [5], D = 10 nm, R_{OFF} = 16 kΩ, R_{ON} = 100 Ω, and $\mu_V = 10^{-14}$ $m^2 s^{-1} V^{-1}$, according to which the dynamic route of the memristor can be drawn, as shown in Figure 1.

The dynamic route is a diagram of dw/dt vs. $w(t)$ with the voltage v_m as a parameter, which is based on the state equation $dw/dt = g(w(t), v_m)$, as shown in Equation (6). Each dynamic route in the graph corresponds to a voltage of the memristor. The dynamic route of voltage v equal to zero is the power-off plot (POP). From the power-off plot $dw/dt = 0$, the corresponding continuous $w(t)$ value is the equilibrium point of the memristor, which shows that the memristor has infinite stable states and is distributed between (0, D). The physical meaning is that the memristor can store any state between (0, D) after power off. The arrow on the graph indicates the direction of change of the memristor state w, $dw/dt > 0$. When $v_m > 0$, state w moves to the right and converges to $w = D$ and $dw/dt < 0$. When $v_m < 0$, state w moves to the left and converges to $w = 0$. Note that the circle on the curve indicates that the value at that point is discontinuous. The circle on the left indicates that the value of all curves should be (0, 0), and the circle on the right indicates that the value of all curves should be (D, 0).

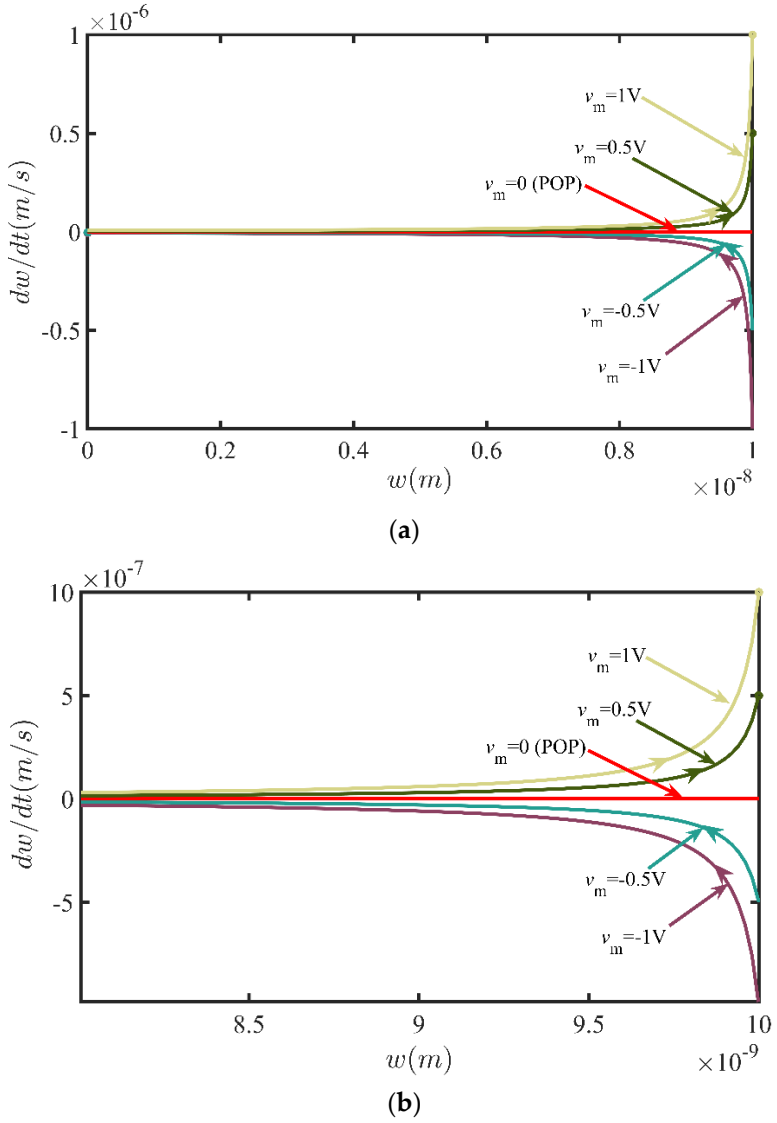


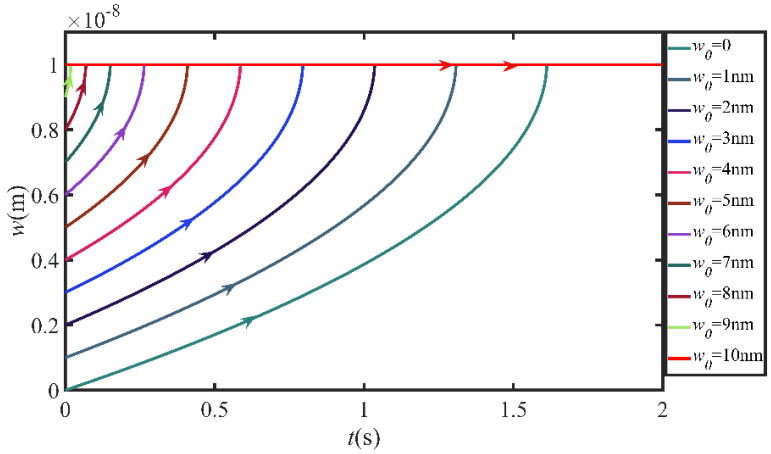
Figure 1. The dynamic route of the Hewlett-Packard (HP) TiO_2 memristor, in which the red line is the power-off plot (POP); that is, the relationship between $\frac{dw}{dt}$ and w when the voltage is 0. (**b**) Local zoom-in of (**a**). Note that the small circles in the curve indicate that the curve cannot obtain the value of that point.

3.1. DC Response

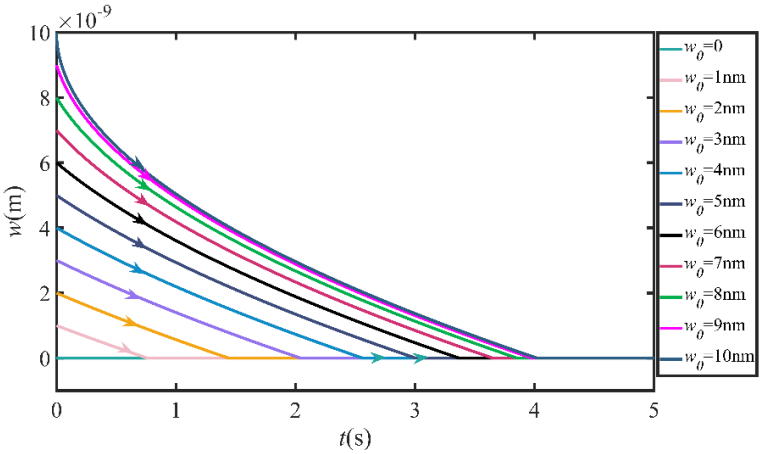
As for the DC response of the memristor, a large number of papers have been published stating that the memristor is excited by a low-frequency AC signal, which is called quasistatic excitation. However, this method is strictly incorrect. The correct method is to make the state equation of the memristor zero. For each V_K value of DC input, the stable equilibrium point X_K satisfying the equation is solved from the state equation, and then the corresponding I_K is obtained by substituting it into Ohm's law equation of the memristor. Then. the points (V_K, I_K) are drawn in the V–I plane and connected with arcs to obtain the relationship curve between I and V, i.e., the DC V–I diagram.

For the HP TiO_2 memristor, we have found that the system has two stable equilibrium points: $w = 0$ and $w = D$. Let $v_m = 0.5$ V and $v_m = -0.2$ V. According to Equation (6), the transient response of the memristor is obtained by solving the differential equation numerically, as shown in Figure 2. Figure 2a corresponds to the excitation of the $v_m = 0.5$ V DC voltage, and the memristor responds with different initial values that converge to $w = D$, i.e., to show the ON resistance R_{ON}. Figure 2b corresponds to $v_m = -0.2$ V. The response of the memristor with different initial values converges to $w = 0$ under the

excitation of −0.2 V, i.e., to show high resistance R_{OFF}. It can be seen from the figure that there are two stable equilibrium points in the memristor.



(**a**)



(**b**)

Figure 2. Transient response of the memristor under DC. (**a**) Corresponding voltage $v_m = 0.5$ V; (**b**) corresponding voltage $v_m = -0.2$ V. The initial value is $w_0 \in$ {0, 1 nm, 2 nm, 3 nm, 4 nm, 5 nm, 6 nm, 7 nm, 8 nm, 9 nm, 10 nm}.

By using the method mentioned above and substituting the two equilibrium points $w = 0$ and $w = D$ of the HP memristor into the first formula in (4), and noting the condition of the existence of the equilibrium point in (6) ($v_m \leq 0$, $w = 0$, and $v_m \geq 0$, $w = D$), the DC response curve can be obtained, as shown in Figure 3.

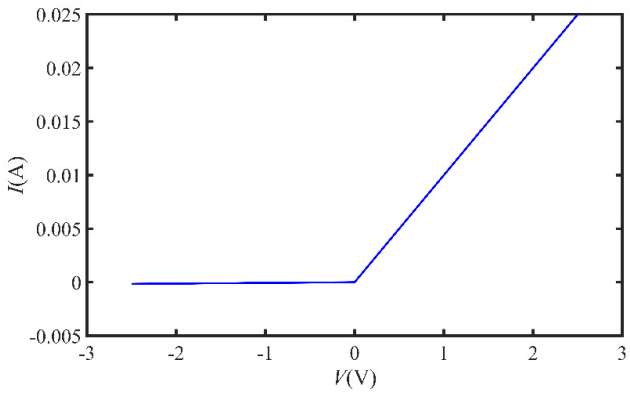
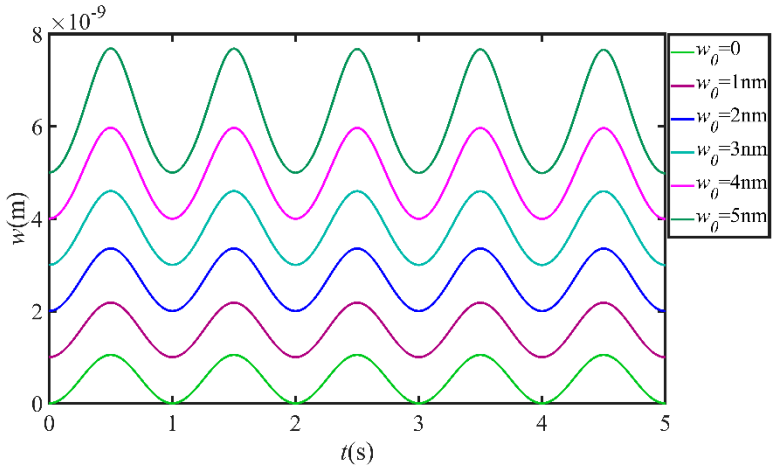


Figure 3. DC response of the HP TiO_2 memristor.

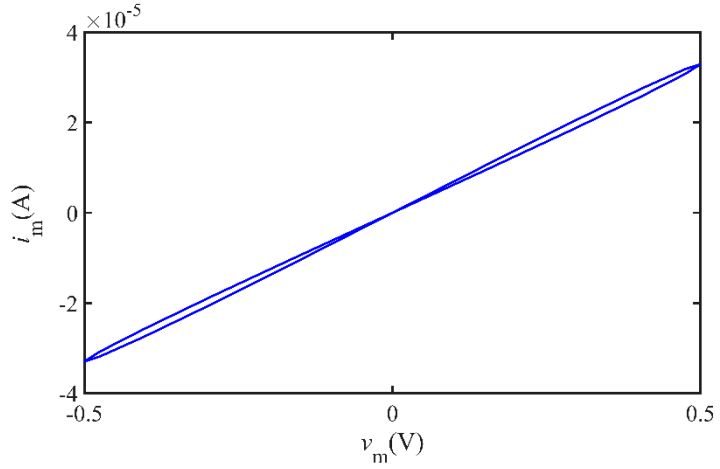
It can be seen from Figure 3 that the voltage and current correspond one-to-one. When $v_m < 0$, there is a high resistance R_{OFF}, and when $v_m > 0$, there is a low resistance R_{ON}. The response is independent of the initial value, and there is a history erase phenomenon. The method to derive Figure 3 is the same as [10], where the DC characteristic of a TaO memristor from HP labs was obtained similarly from the Strachan model, presented in [23] after opportune boundary conditions were imposed on the allowable memristor state existence domain.

3.2. AC Response

The AC response of the HP TiO_2 memristor is studied below. In other words, $v_m(t) = 0.5sin(2\pi ft)$ is substituted into Equation (6) to solve the differential equation with different initial values by a numerical method. The response of the solution is shown in Figure 4. Figure 4a corresponds to f = 1 Hz, which is equivalent to the excitation under quasistatic conditions, and Figure 4c corresponds to f = 10 Hz. The response in both cases shows that there is no history erase effect. In fact, this is predictable. If we look at Figure 1 carefully, we find that the curve family is symmetrical about the horizontal axis, which indicates that the rate of change dw/dt is symmetrical about the positive and negative swings of the AC signal. Thus, the net contribution of dw/dt to the state w in a signal cycle is 0. Therefore, periodic oscillation should be made around the initial value, and the curve distinguishes with different initial values. It should be noted that the amplitude of the response decreases when frequency increases. This is because the $v_\mathrm{m} - i_\mathrm{m}$ pinched loop shrinks when the frequency increases (see Figure 4b,d).

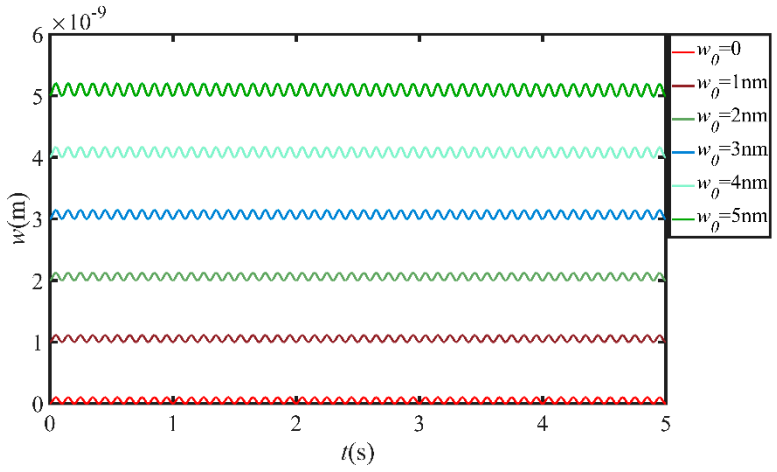


(**a**)

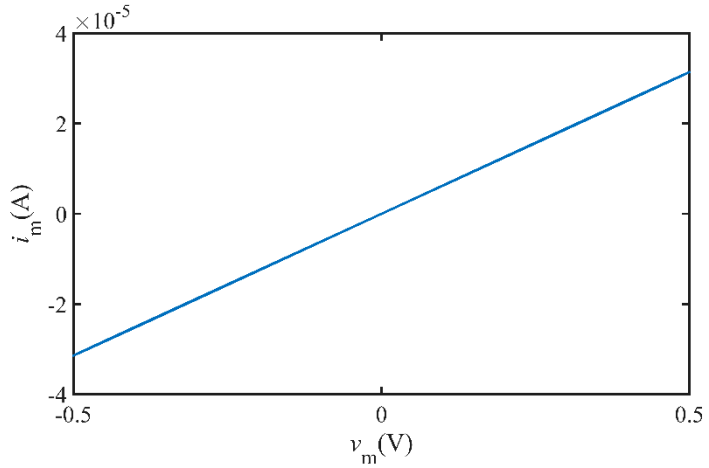


(**b**)

Figure 4. *Cont.*



(c)



(d)

Figure 4. $v_m(t) = V_0 sin(2\pi ft)$ is used as the excitation signal, where $V_0 = 0.5$ V. (**a**) corresponds to f = 1 Hz, equivalent to the excitation under quasistatic conditions; (**b**) corresponds to the locus of $v_\mathrm{m} - i_\mathrm{m}$ at f = 1 Hz; (**c**,**d**) correspond to f = 10 Hz.

3.3. Closed-Form Solution of th eDynamic Equation of the HP TiO_2 Memriston

It is observed that the HP TiO_2 memristor does not have a history erase effect according to the numerical method above. Next, the response properties of the HP TiO_2 memristor are given by a strict mathematical method.

Substituting the first equation of (4) into the second, the following relationship is obtained:

$$\frac{dw(t)}{dt} = \mu_v \frac{R_{ON}}{D} \frac{v_m(t)}{R_{ON}\frac{w(t)}{D} + R_{OFF}(1 - \frac{w(t)}{D})} \tag{7}$$

By separating the variables and integrating the two sides, the following results are obtained:

$$\int_{w(0)}^{w(t)} \left(R_{ON}\frac{w(t)}{D} + R_{OFF}(1 - \frac{w(t)}{D}) \right) dw(t) = \int_0^t \mu_v \frac{R_{ON}}{D} v_m(t) dt \tag{8}$$

Equation (8) can be further expressed as:

$$\tfrac{1}{2D}(R_{OFF} - R_{ON})w^2(t) - R_{OFF}w(t) + \mu_v \tfrac{R_{ON}}{D}\varphi_m(t) - \mu_v \tfrac{R_{ON}}{D}\varphi_m(0) - [\tfrac{1}{2D}(R_{OFF} - R_{ON})w^2(0) - R_{OFF}w(0)] = 0 \tag{9}$$

The expression of $w(t)$ is obtained by solving the equation.

$$w(t) = \frac{R_{OFF} \pm \sqrt{R_{OFF}^2 - \frac{2}{D}(R_{OFF} - R_{ON})[\mu_v \frac{R_{ON}}{D}\varphi_m(t) - \mu_v \frac{R_{ON}}{D}\varphi_m(0) - (\frac{1}{2D}R_{OFF}w^2(0) - R_{OFF}w(0))]}}{\frac{R_{OFF}-R_{ON}}{D}} \quad (10)$$

Note that because $0 \le w(t) \le D$ holds, we should drop the plus sign in Equation (10). Note also that $R_{OFF} \gg R_{ON}$, and the above formula is simplified as:

$$w(t) = (D - D\sqrt{1 - \frac{2}{D}[\mu_v \frac{R_{ON}}{DR_{OFF}}\varphi_m(t) - \mu_v \frac{R_{ON}}{DR_{OFF}}\varphi_m(0) - (\frac{1}{2D}w^2(0) - w(0))]}) \quad (11)$$

Under DC,

$$\frac{d\varphi_m(t)}{dt} = V \quad (12)$$

By integrating the two sides, we obtain:

$$\varphi_m(t) = \varphi_m(0) + Vt \quad (13)$$

Substituting Equation (13) into Equation (11), we obtain:

$$w(t) = D - D\sqrt{1 - T} \quad (14)$$

where

$$T = \frac{2}{D}[\mu_v \frac{R_{ON}}{DR_{OFF}}Vt - (\frac{1}{2D}w^2(0) - w(0))]$$

In Formula (14), $w(t)$ is a real number and $0 \le w(t) \le D$; therefore, $0 \le \sqrt{1-T} \le 1$ and $0 \le T \le 1$. If a positive DC voltage $V > 0$ is applied to the memristor, then T is a monotonic increasing function and $\sqrt{1-T}$ a monotonic decreasing function. When the memristor reaches $T = 1$, $w(t)$ reaches the upper limit D; if a negative DC voltage $V < 0$ is applied to the memristor, T is a monotonic decreasing function and $\sqrt{1-T}$ a monotonic increasing function. When $T = 0$ and $\sqrt{1-T} = 1$, with t increasing, $w(t)$ reaches the lower limit of 0.

Although the state variable w in Equation (11) is a function of the initial value w(0), under the excitation of positive and negative DC voltages, the memristor rapidly reaches two states, namely low resistance R_{ON} and high resistance R_{OFF}, which are independent of the initial value, indicating that the memristor has a history erase effect. If the memristor is excited by positive and negative pulse voltages, as long as its amplitude and pulse width meet the condition of the state transition, the memristor will become a nonvolatile binary switch device, which can be used in binary memory.

Figure 5 shows the DC response diagram of the memristor state variables when $V = 0.5$ V and $V = -0.2$ V, showing the two limit states under different initial values.

It will be proved that the AC response of the HP memristor has no history erase effect under any AC voltage excitation. When AC voltage is v, we have

$$\frac{d\varphi_m(t)}{dt} = v(t) \quad (15)$$

by integrating the two sides, we obtain:

$$\varphi_m(t) = \varphi_m(0) + \int_0^t v_m(t)dt \quad (16)$$

substituting Equation (16) into Equation (11) yields:

$$w(t) = (D - D\sqrt{1 - \frac{2}{D}[\mu_v \frac{R_{ON}}{DR_{OFF}}\int_0^t v_m(t)dt - (\frac{1}{2D}w^2(0) - w(0))]}) \quad (17)$$

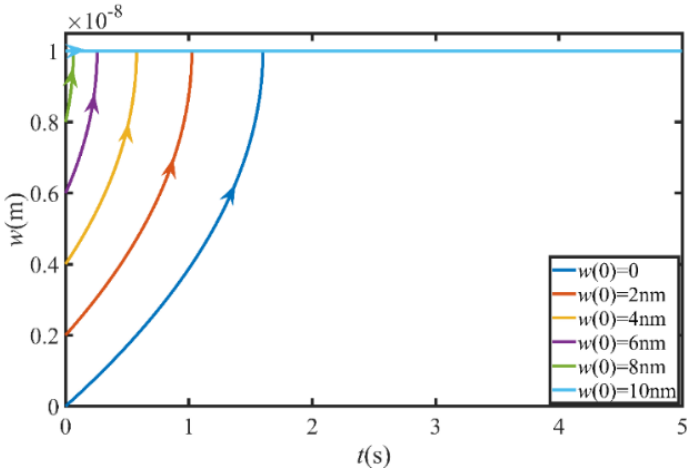
Because the AC signal $v_m(t)$ is arbitrarily chosen, the root term in Equation (17) is not a monotone increasing or decreasing function and is closely related to the initial value w(0) of the memristor. The state variable $w(t)$ is related to the initial value, and there is no history erase effect. Taking the cosine excitation signal as an example, the excitation voltage is assumed to be $v_m = cos(t)$, then $\int_0^t v_m(t)dt = \sin t$. Substituting it into Equation (17) will obtain:

$$w(t) = (D - D\sqrt{1 - \frac{2}{D}[\mu_v \frac{R_{ON}}{DR_{OFF}} \sin t - (\frac{1}{2D}w^2(0) - w(0))]}) \tag{18}$$

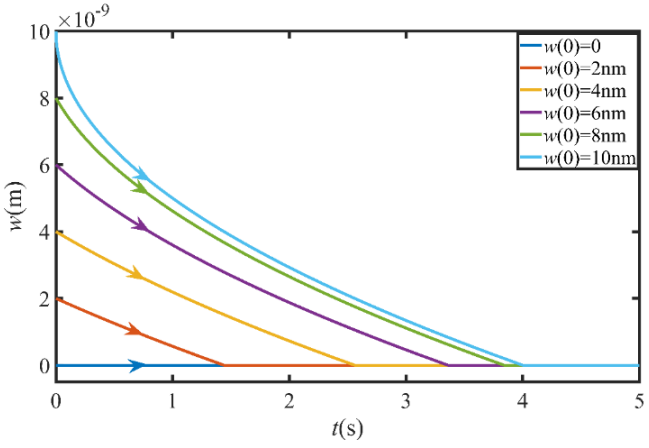
It is obvious that the state variable w varies with time t and initial value $w(0)$. Especially when $t = k\pi$, $k \in$ N Equation (18) becomes

$$w(k\pi) = (D - D\sqrt{1 + \frac{2}{D}(\frac{1}{2D}w^2(0) - w(0))}) \tag{19}$$

$w(k\pi)$ depends directly on the initial value $w(0)$, which shows that the AC response of the memristor is related to the initial value, and there is no history erase effect.



(**a**)



(**b**)

Figure 5. DC response diagram of the memristor, according to Equation (15). (**a**) Under a positive voltage $v_m = 0.5$ V, the responses of initial values $w(0) \in \{0,\ 2\text{ nm}, 4\text{ nm}, 6\text{ nm}, 8\text{ nm}, 10\text{ nm}\}$ are obtained. (**b**) Under a negative voltage $v_m = -0.2$ V, the responses of initial values $w(0) \in \{0,\ 2\text{ nm}, 4\text{ nm}, 6\text{ nm}, 8\text{ nm}, 10\text{ nm}\}$ are obtained.

3.4. HP TiO_2 Memristor Model with a Window Function

The HP memristor model represented by Equation (4) is an ideal model, in which the equation of state is linear, which means that the ions in the doped region move linearly under the external electric field. In practice, however, the drift motion is nonlinear. The boundary effect at the two ends of $w = 0$ and $w = D$ especially is strongly nonlinear. In order to describe this nonlinear effect, Strukov added a window function $w(D-w)/D^2$ to his memristor model in his original reference [5], and modified the memristor (Equation (4)) into the following form:

$$\begin{cases} v_m(t) = (R_{ON}\frac{w(t)}{D} + R_{OFF}(1-\frac{w(t)}{D}))i_m(t) \\ \frac{dw(t)}{dt} = \mu_V \frac{R_{ON}}{D} i_m(t) \frac{w(t)(D-w(t))}{D^2} \end{cases} \tag{20}$$

By inserting the first formula of Equation (20) with the second, separating variables, and integrating both sides, we obtain:

$$\int_{w(0)}^{w(t)} D\left(\frac{R_{ON}}{D-w(t)} + \frac{R_{OFF}}{w(t)}\right) dw(t) = \int_0^t \mu_v \frac{R_{ON}}{D} v_m(t) dt \tag{21}$$

In (21), the integral is solved and simplified to

$$\frac{w(t)^{R_{OFF}}}{(D-w(t))^{R_{ON}}} = \frac{w(0)^{R_{OFF}}}{(D-w(0))^{R_{ON}}} e^{-\mu_v \frac{R_{ON}}{D^2}\varphi_m(0)} e^{\mu_v \frac{R_{ON}}{D^2}\varphi_m(t)} \tag{22}$$

when DC excitation is applied:

$$\frac{d\varphi_m(t)}{dt} = V \tag{23}$$

By integrating the two sides, we obtain:

$$\varphi_m(t) = \varphi_m(0) + Vt \tag{24}$$

Substituting Equation (24) into Equation (22), we obtain the following results:

$$\frac{w(t)^{R_{OFF}}}{(D-w(t))^{R_{ON}}} = \frac{w(0)^{R_{OFF}}}{(D-w(0))^{R_{ON}}} e^{\mu_v \frac{R_{ON}}{D^2} Vt} \tag{25}$$

If a positive voltage is applied and the right side of the equation is an increasing function of t, which tends to infinity after a period of time, then there must be $w(t) \to D$ on the left side of the equation; if a negative voltage is applied and the right side of the equation is a decreasing function of t and tends to 0 after a period of time, then there must be $w(t) \to 0$ on the left side of the equation. It can be seen that under the excitation of positive and negative DC voltages, the memristor state variables w tend to D and 0, respectively; that is, the memristor is in R_{ON} and R_{OFF} states, respectively, and its response is independent of the initial value.

When an AC cosine voltage is applied, Equation (24) becomes $\varphi_m(t) = \varphi_m(0) + \sin(t)$. Let the responses of the state variable under two different initial values, respectively, be $w_1(t)$ and $w_2(t)$, which can be substituted into Equation (22) and divided:

$$\frac{\frac{w_2(t)^{R_{OFF}}}{(D-w_2(t))^{R_{ON}}}}{\frac{w_1(t)^{R_{OFF}}}{(D-w_1(t))^{R_{ON}}}} = \frac{\frac{w_2(0)^{R_{OFF}}}{(D-w_2(0))^{R_{ON}}}}{\frac{w_1(0)^{R_{OFF}}}{(D-w_1(0))^{R_{ON}}}} \tag{26}$$

when $t \to \infty$, if $w_1(t)$ tends to $w_2(t)$, the left side of Equation (26) is 1, while the right side is equal to a constant, which is not 1:

$$R.H.S. = \frac{\frac{w_2(0)^{R_{OFF}}}{(D-w_2(0))^{R_{ON}}}}{\frac{w_1(0)^{R_{OFF}}}{(D-w_1(0))^{R_{ON}}}} \tag{27}$$

In this case, Equation (26) would not hold, i.e., $w_1(\infty) \neq w_2(\infty)$. Therefore, there is no history erase effect in the memristor.

3.5. Parasitic Memcapacitance Effect of the HP TiO_2 Emristor

If we further observe the structure of the HP TiO_2 memristor, we will find that there is a parasitic parallel plate capacitor in the memristor; in fact, as shown next, it is a memcapacitor, because the capacitance is dependent on state variable w, and the dielectric between the two plates is undoped TiO_2. This is because undoped TiO_2 has a higher resistivity, equivalent to an insulator medium, while doped TiO_2 has a lower resistivity, equivalent to a conductor, as shown in Figure 6.

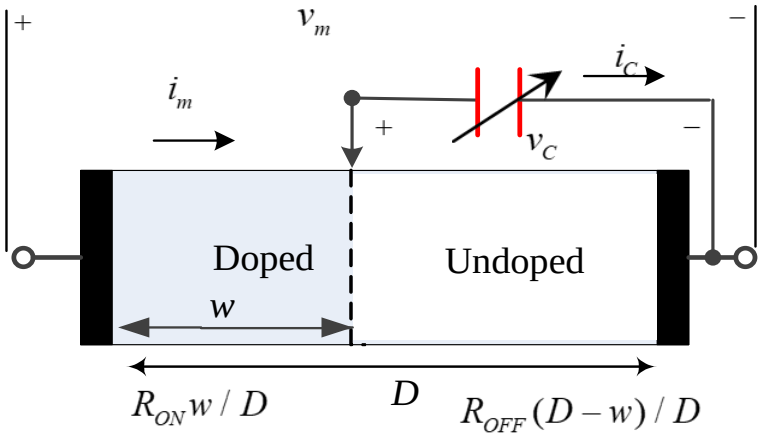


Figure 6. Structure of the HP TiO_2 memristor.

The parasitic capacitance is equivalent to a flat-plate capacitor, and because the capacitance is dependent on state variable $w(t)$, it is indeed a memcapacitor:

$$C = \frac{\varepsilon_{TiO_2} S}{D - w} \tag{28}$$

According to [24], we know $\varepsilon_{TiO_2} = 5\varepsilon_0 F/m$, $S = 1 \times 10^4$ nm^2. When the parasitic memcapacitance is considered, by KCl and KVL, we have:

$$\begin{cases} v_m(t) = R_{ON}\frac{w(t)}{D} i_m(t) + R_{OFF}(1 - \frac{w(t)}{D})(i_m(t) - i_C(t)) \\ i_C(t) = \frac{dC}{dt} v_C(t) + C\frac{dv_C(t)}{dt} \\ v_C(t) = v_m(t) - R_{ON}\frac{w(t)}{D} i_m(t) \\ \frac{dw(t)}{dt} = \mu_V \frac{R_{ON}}{D} i_m(t) \end{cases} \tag{29}$$

where $v_C(t)$ is the voltage across both ends of the capacitor, and dC/dt is the derivative of capacitance to time. Expression (28) of capacitance is substituted into the second equation of (29), and then the second equation is substituted into the first equation and the third equation into the forth, and Equation (30) is obtained:

$$\begin{cases} \frac{dw(t)}{dt} = \frac{\mu_V}{w(t)}(v_m(t) - v_C(t)) \\ \frac{dv_C(t)}{dt} = \frac{D(1-\frac{w(t)}{D})}{\varepsilon_{TiO_2} S}\left[\frac{v_m(t)-v_C(t)}{R_{ON}\frac{w(t)}{D}} - \frac{v_C(t)}{R_{OFF}(1-\frac{w(t)}{D})} - \frac{\varepsilon_{TiO_2} S}{D^3(1-\frac{w(t)}{D})^2}\frac{\mu_V}{\frac{w(t)}{D}}(v_m(t) - v_C(t))v_C(t)\right] \end{cases} \quad (30)$$

According to Equation (30), the AC response of state variable $w(t)$ to t is solved by MATLAB and shown as Figure 7. The excitation signal in the diagram is $v_m(t) = V_0 sin(2\pi ft)$, V_0 is selected as 0.5 V, and f is set to 10 Hz.

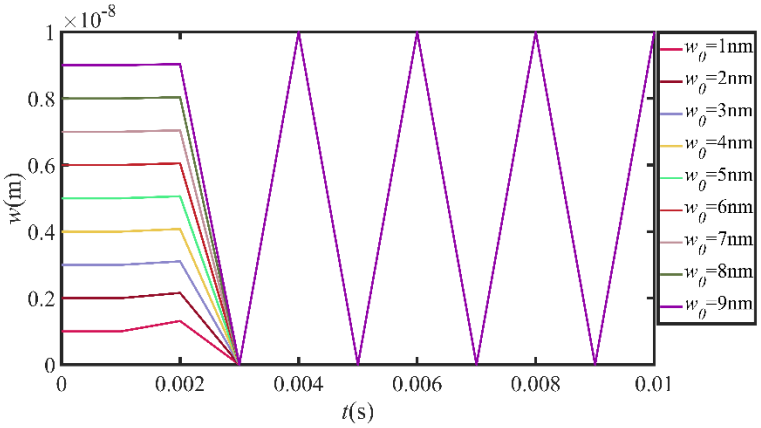


Figure 7. AC response of state variable $w(t)$ to t considering parasitic memcapacitance, in which the excitation signal is v_m (*t*) = V_0 *sin*($2\pi ft$), V_0 is selected as 0.5 V, and f is set to 10 Hz.

It can be seen from the figure that under different initial values, the AC response converges to a stable value after a period of time, so there is a history erase effect.

4. The Self-Directed Channel (SDC) Memristor

The Self-Directed Channel (SDC) memristor is a product developed by Knowm Company. This is an ion conduction device (also known as an electrochemical metallization (ECM) device), which changes the resistance of the device by relying on Ag+ entering the channel of the active layer of the device. The hysteretic curve can be measured by software and hardware tools provided by Knowm Company. However, there is no mathematical model. In order to analyze it theoretically and design a memristor circuit with it, it is necessary to establish a mathematical model for it.

4.1. Establishment of the SDC Memristor Model

In his 2015 paper [20], Kvatinsky proposed a generic voltage-controlled memristor model VTEAM. The model's equation is as follows:

$$i_m(t) = v_m(t)/(R_{ON} + \frac{w - w_{ON}}{w_{OFF} - w_{ON}}(R_{OFF} - R_{ON})) \quad (31)$$

$$\frac{dw(t)}{dt} = \begin{cases} k_{OFF}(\frac{v_m(t)}{v_{OFF}} - 1)^{\alpha_{OFF}}, & 0 < v_{OFF} < v, \\ 0 & v_{ON} < v_m < v_{OFF}, \\ k_{ON}(\frac{v_m(t)}{v_{ON}} - 1)^{\alpha_{ON}}, & v_m < v_{ON} < 0. \end{cases} \quad (32)$$

The equation has ten parameters, where R_{OFF}, R_{ON}, v_{OFF}, v_{ON}, w_{OFF}, w_{ON}, k_{OFF} and k_{ON} are real numbers, and α_{OFF}, α_{ON} are natural numbers. w_{OFF}, w_{ON} are the boundaries of the internal variable w, and R_{OFF}, R_{ON} are resistance values when the values of state variable are w_{OFF}, w_{ON}, respectively. k_{OFF}, k_{ON}, α_{OFF} and α_{ON} are constants, and v_{OFF}, v_{ON} are the threshold voltages.

VTEAM model is a generic model. Because of its inherent universality and robustness, it can be applied to a large number of memristor models and experimental data. Consid-

ering the current voltage characteristics of a specific memristor, a set of parameters are selected to make the VTEAM model conform to the reference I–V relationship of the SDC memristor. In order to determine the I–V curve, simulated annealing algorithms can be used to minimize the relative root mean square error. The relative root mean square error is

$$f(\mathrm{x}) = \sqrt{\frac{\left(\frac{\sum_{i=1}^{N} (v(\mathrm{x}) - v_{ref})^2}{\sum_{i=1}^{N} v_{ref}^2} + \frac{\sum_{i=1}^{N} (i(\mathrm{x}) - i_{ref})^2}{\sum_{i=1}^{N} i_{ref}^2} \right)}{N}} \tag{33}$$

where N is the number of samples, $v(\mathrm{x})$ and $i(\mathrm{x})$ are the sampling voltage and current values of the VTEAM model, respectively, and v_{ref} and i_{ref} are the actual measured sampling voltage and current values, respectively.

The fitting process is to make the program iterate over k_{OFF}, k_{ON} to minimize the error function given in (33). In order to avoid convergence to the local minimum instead of the best global fit, other parameters ($R_{OFF}, R_{ON}, v_{OFF}, v_{ON}, w_{OFF}, w_{ON}, \alpha_{OFF}, \alpha_{ON}$) are selected manually to show as much similarity as possible to the reference I–V relationship (relative root mean square error is less than 1.5%). In addition, the ideal window function can be used to constrain the state variables in the process of fitting.

In the experiment, the memristor is connected with a 1KΩ resistor in series and an applied AC signal as $v_m(t) = V_0 sin(2\pi f t)$. Considering that only part of the voltage falls on the memristor, V_0 can be taken as 1 V, and the frequency f can be set to 5 Hz. After the volt–ampere data are obtained, the data are imported into MATLAB, and the simulated annealing algorithm is used to set the objective function to (34).

The VTEAM model was used to fit the experimental data, and Figure 8 was obtained. Looking at Figure 8, it can be found that the model fitting is very good in the first quadrant, while there is a little difference between the fitting data and the measured data in the third quadrant. This is mainly due to the insufficient sampling accuracy of the measurement software and hardware provided by Knowm Company (200 time points in total).

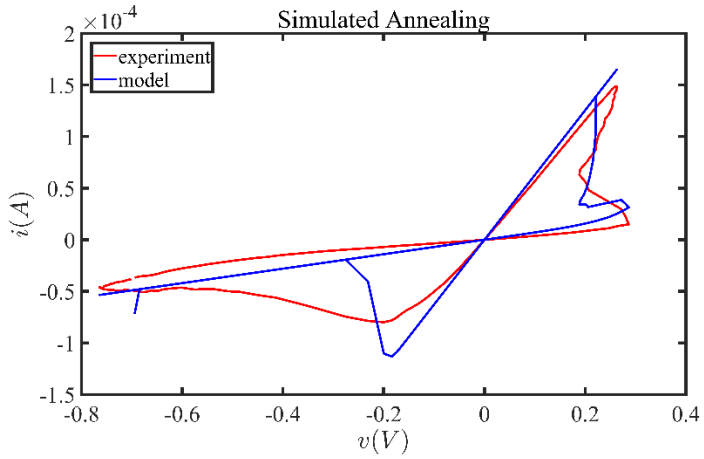


Figure 8. Volt–ampere characteristic curve of memristor. Red is the experimental data, blue is the model fitting data under the optimization algorithm.

According to the computer simulation, the optimal parameters of the model can be determined as shown in Table 1.

Table 1. Model parameters obtained by the simulation of the optimization algorithm.

Parameters	Value
R_{OFF}	14.277 kΩ
R_{ON}	1.5936 kΩ
v_{OFF}	0.02 V
v_{ON}	−0.13 V
k_{OFF}	538,530.50 nm
k_{ON}	−2.6213 m
α_{OFF}	2
α_{ON}	8
w_{ON}	0
w_{OFF}	0.001 m

4.2. Dynamic Routes and AC Response of the SDC Memristor

According to the model parameters, the dynamic routes of the SDC memristor can be drawn in a similar way to that of the HP TiO_2 memristor and shown as Figure 9. It is noted that in Equation (32), dw/dt does not depend on w but only on v_m. Therefore, dw/dt vs. w is a set of horizontal lines.

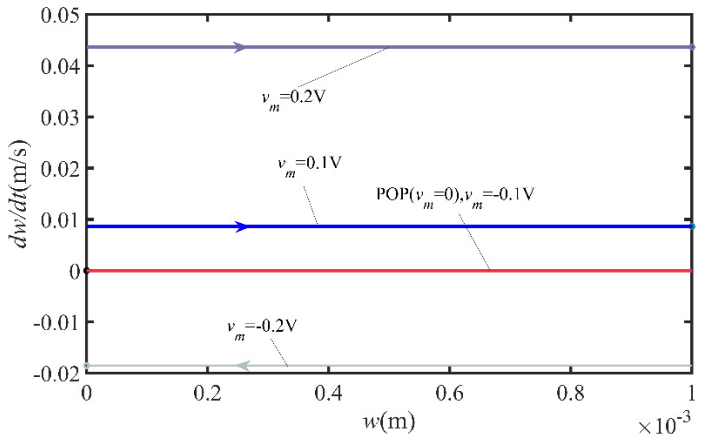
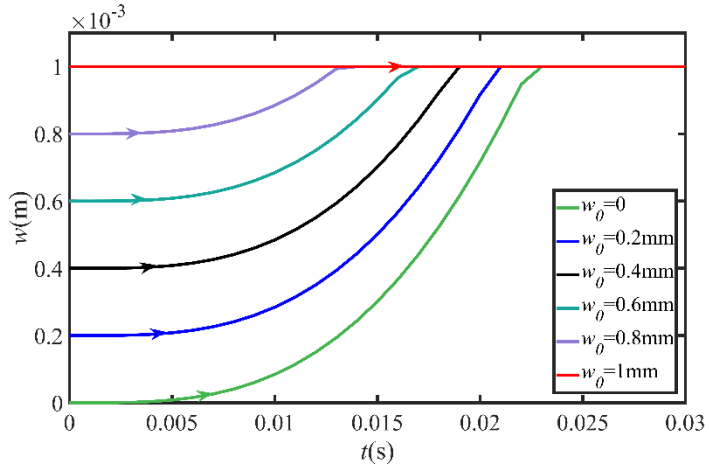
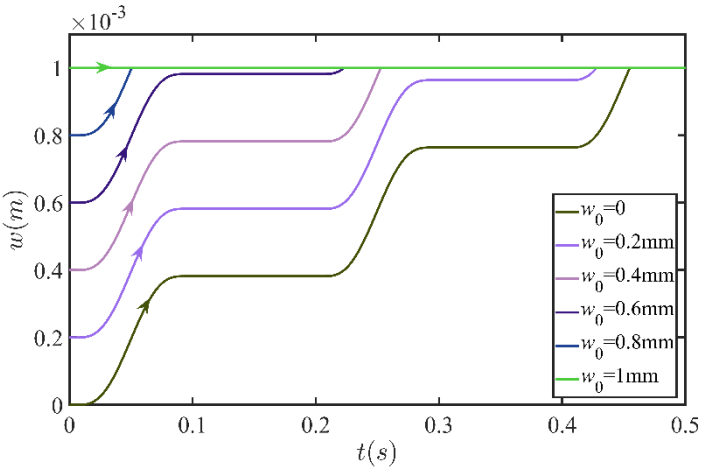


Figure 9. Dynamic routes of the Self-Directed Channel (SDC) memristor. Tote that POP (v_m = 0) and the line corresponding to v_m = 0.1 V are in fact two different lines.

It can be seen from the diagram that the dynamic routes are asymmetric with respect to the horizontal axis, which indicates that the net contribution of dw/dt to w is not zero when the signal amplitude is positive and negative for one cycle under AC excitation. Therefore, it is speculated that under AC excitation, $w(t)$ may gradually tend to a stable value after a period of time under the state of net increase or decrease of $w(t)$, thus it has a history erase effect. We use a sinusoidal signal $v_m(t) = V_0 sin(2\pi ft)$, where f is 5 Hz and with $V_0 = 0.5$ V as the AC excitation and applied to the memristor. Thus, Figure 10 can be obtained. It can be seen from Figure 10 that the SDC memristor has a history erase effect under AC conditions.



(**a**)



(**b**)

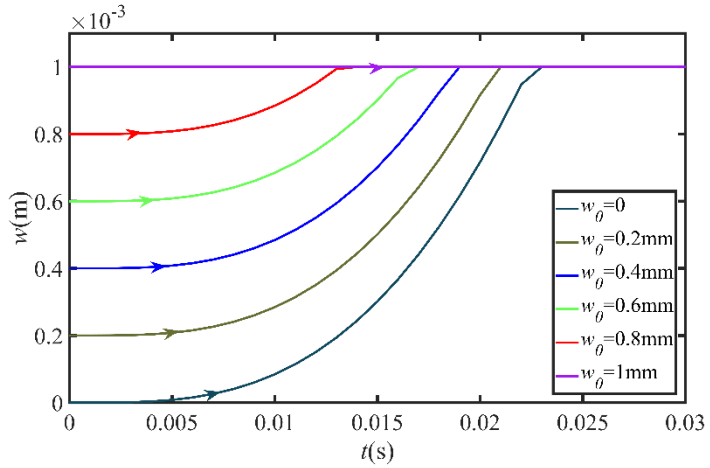
Figure 10. Sinusoidal signal $v_m(t) = V_0 sin(2\pi ft)$, with f = 5 Hz and V_0 = 0.5 V as the AC excitation and applied to the memristor (**a**) can be obtained, (**b**) corresponds to V_0 = 0.1 V.

4.3. Considering the Parasitic Capacitance Effect

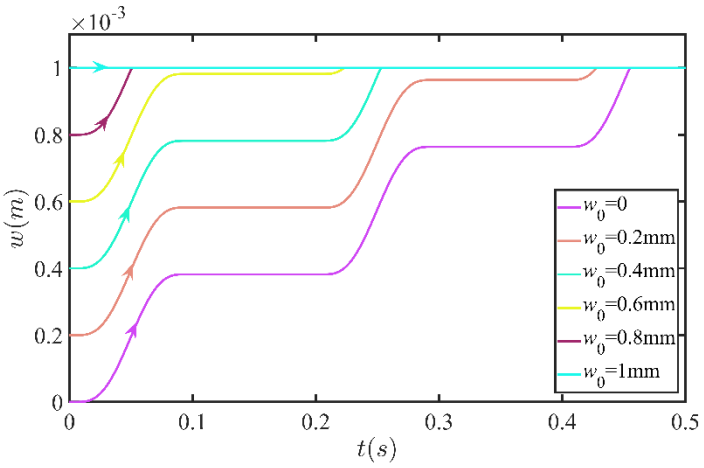
Similar to the case of the HP TiO_2 memristor (refer to Figure 6), considering that the undoped part is also equivalent to a moving parallel plate capacitor, it can be considered to have parallel a small parasitic capacitor on it. Assuming 1nF, the circuit equation becomes:

$$\begin{cases} \frac{dv_C(t)}{dt} = \frac{1}{C}\left[\frac{v_m(t)-v_C(t)}{(1-\frac{w-w_{ON}}{w_{OFF}-w_{ON}})R_{ON}} - \frac{v_C(t)}{\frac{w-w_{ON}}{w_{OFF}-w_{ON}}R_{OFF}}\right] \\ \frac{dw(t)}{dt} = \begin{cases} k_{OFF}\left(\frac{v_m(t)}{v_{OFF}}-1\right)^{\alpha_{OFF}}, & 0 < v_{OFF} < v, \\ 0 & v_{ON} < v_m < v_{OFF}, \\ k_{ON}\left(\frac{v_m(t)}{v_{ON}}-1\right)^{\alpha_{ON}}, & v_m < v_{ON} < 0. \end{cases} \end{cases} \quad (34)$$

The solution of the state variable $w(t)$ can be obtained by numerically solving the above differential equation with MATLAB, as shown in Figure 11.



(**a**)



(**b**)

Figure 11. AC response with parasitic capacitance taken into account. Using sinusoidal signal $v_m(t) = V_0 sin\ (2\pi ft)$, with f = 5 Hz and V_0 = 0.5 V as the AC excitation, (**a**) is obtained. (**b**) corresponds to V_0 = 0.1 V.

Compared with Figures 10 and 11, the parasitic capacitance has little effect on the SDC memristor.

5. Conclusions

In this paper, the history erase effect of the HP TiO_2 memristor is studied. Firstly, the existence of the history erase effect under DC and AC conditions is predicted from the dynamic routes. The historical erase properties of the HP TiO_2 memristor under AC and DC are then verified by a MATLAB numerical simulation. It can be seen that the HP TiO_2 memristor has a DC history erase effect but no AC history erase effect. After the numerical simulation, the closed-form solution of the dynamic equation of the TiO_2 memristor is given. Thus, the history erase properties of the TiO_2 memristor under DC and AC conditions are explained theoretically. Furthermore, the parasitic capacitance effect of the HP TiO_2 memristor is considered, and it is pointed out that the parasitic capacitance effect can cause the HP TiO_2 memristor to have an AC history erase effect. It is worth noting that Menzel et al. pointed out that the resistance of the doping region in the memristor is the origin of history erase effect [13]. From the work of this paper, it seems that the resistance of the doped region and the parasitic memcapacitance of the undoped region work together to form a discharge path, which leads to the history erase effect. As a supplement to the research work on the history erase effect of the HP TiO_2 memristor, we studied the history erase effect of the latest discrete SDC memristor made by Knowm

Company. The DC and AC voltages and parasitic capacitance are considered, respectively. It is worth mentioning that the method of modeling the SDC memristor with the generic voltage-controlled memristor model VTEAM is also given in this paper. This method uses a simulated annealing algorithm to fit the actual measured data, which solves the problem that Knowm Company's discrete SDC memristor still lacks an accurate mathematical model. It can be seen that no matter with and without the parasitic capacitance, the SDC memristor has an AC history erase effect.

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