

Article

A Bootstrap Structure Directly Charged by BUS Voltage with Threshold-Based Digital Control for High-Speed Buck Converter

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Abstract: This article proposes a high-frequency, area-efficient high-side bootstrap circuit with threshold-based digital control (TBDC) that is directly charged by BUS voltage (DCBV). In the circuit, the voltage of the bootstrap is directly obtained from the BUS voltage instead of the on-chip low dropout regulator (LDO), which is more suitable for a high operating frequency. An area-efficient threshold-based digital control structure is used to detect the bootstrap voltage, thereby effectively preventing bootstrap under-voltage or over-voltage that may result in insufficient driving capability, increased loss, or breakdown of the power device. The design and implementation of the circuit are based on CSMC 0.25 μm 60 V BCD technology, with an overall chip area of $1.4 \times 1.3 \text{ mm}^2$, of which the bootstrap area is 0.149 mm^2 and the figure-of-merit (FOM) is 0.074. The experimental results suggest that the bootstrap circuit can normally operate at 5 MHz with a maximum buck converter efficiency of 83.6%. This work plays a vital role in promoting the development of a wide range of new products and new technologies, such as integrated power supplies, new energy vehicles, and data storage centers.

Keywords: bootstrap circuit; high voltage; buck converter; high frequency; area-efficient



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1. Introduction

With the continuous development of modern electronic equipment power supplies, miniaturized and high-performance power drivers have become a current research hotspot [1–6]. Regarding traditional silicon complementary metal-oxide-semiconductor (CMOS) technology, NMOS (n-channel metal-oxide-semiconductor) is usually selected as the power device [7–9], which is mainly attributed to its high carrier mobility and desirable device area [10]. Additionally, third-generation semiconductor power devices with the characteristics of high speed and low on-resistance, such as GaN HEMTs (gallium nitride high-electron-mobility transistors) [11–14], are also dominated by N-type devices.

LDOs [15], dc-dc converters (such as charge pumps [16–18]) and pre-regulators [19] are mainly employed in a low-side N-Type power MOS structure with the power supply relative to ground. Regarding a high-side N-type power device, the floating source demonstrates the high-side driving problem of the device [20,21], which is usually solved by bootstrap charging circuits [22–24]. The principle of these circuits is to provide a voltage that is relative to the floating source, namely the switching node (V_{SW}), for driver and power MOS [25]. Although the traditional bootstrap charging circuit shown in Figure 1 has a simple structure, there are still a series of problems to be solved.

The traditional bootstrap charging circuit needs a fixed charging voltage V_{DD} , which is generally set between 5 and 6 V, and it is generated by the on-chip power supply. In the case of a large driving capability and high switching frequency, the requirements for

the load current, bandwidth, and stability of the on-chip regulator are relatively high, which increases the design difficulty of the LDO. On the other hand, the change in the V_{DD} will cause a certain offset in the V_{boot} voltage of the traditional bootstrap circuit. When the bootstrap voltage is too high, the gate of the power device, especially the GaN HEMT, easily breaks down. Conversely, a bootstrap voltage that is too low will affect the driving capability of the circuit, resulting in excessive on-resistance of the power device and increasing power loss. Li, S.T. et al., proposed the theory of active bootstrap control (ABC) [26], that is, the logic control of the high-side signal, low-side signal, and dead time ensures that the bootstrap capacitor is charged only when the low-side power device is turned on. Ke, X. et al., proposed an active BST balancing (ABB) method to achieve bootstrap voltage control [27].

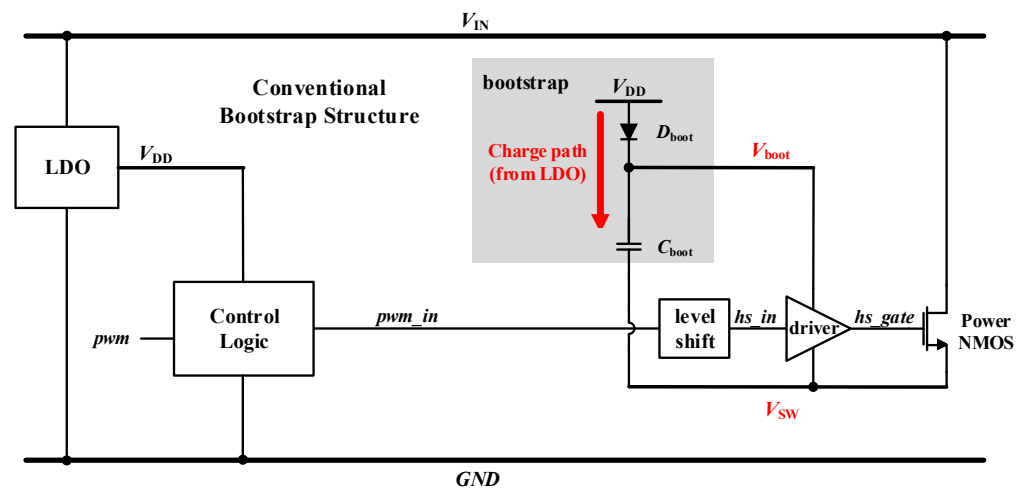


Figure 1. Traditional bootstrap structure charging from an LDO, which brings bandwidth and stability pressure to LDO.

Although a series of considerable research results have been achieved in bootstrap voltage control, there are still certain challenges in reducing the pressure on LDO design. Ming, X. et al., proposed an advanced bootstrap circuit structure that does not depend on the voltage of the on-chip low dropout linear regulator, which also ensures the stability of the high-side power rail by using the directly sensed bootstrap voltage (DSBV) [28]. A bootstrap structure is proposed by Liu, Y. et al., the bootstrap voltage of which is charged by input power and regulated by a feedback loop [29]. The conventional structure employs an analog feedback loop, the speed of which is influenced by the loop bandwidth, while high bandwidth and high stability are hard to achieve at the same time. Herein, based on the above-mentioned research, this paper presents a bootstrap circuit structure with the following advantages: a small area, high frequency, and good figure-of-merit (FOM). Without an analog loop, the speed of the structure is only determined by the threshold-based detection circuit, avoiding the trade-off between bandwidth and stability. The DCBV circuit is used to directly charge the bootstrap capacitor from the BUS voltage V_{IN} , which greatly reduces the design difficulty of the low dropout linear regulator. The TBDC circuit is used to detect the voltage of the high-side bootstrap power rail, which can control the on-off of the PMOS switch in the DCBV circuit, thereby ensuring that the bootstrap voltage is within the required range.

2. Materials and Methods

2.1. Concept of the Proposed Bootstrap Architecture

As shown in Figure 2, the DCBV is directly used in the bootstrap charging of the proposed structure, which reduces the pressure on the bandwidth and load capacity of the on-chip LDO at high frequency. The TBDC circuit is used to detect the bootstrap voltage, which is mainly composed of isolated MOSFETs instead of high-voltage devices, and

controls the charging path of the bootstrap. Moreover, the logic control module is related to the detection result of the TBDC.

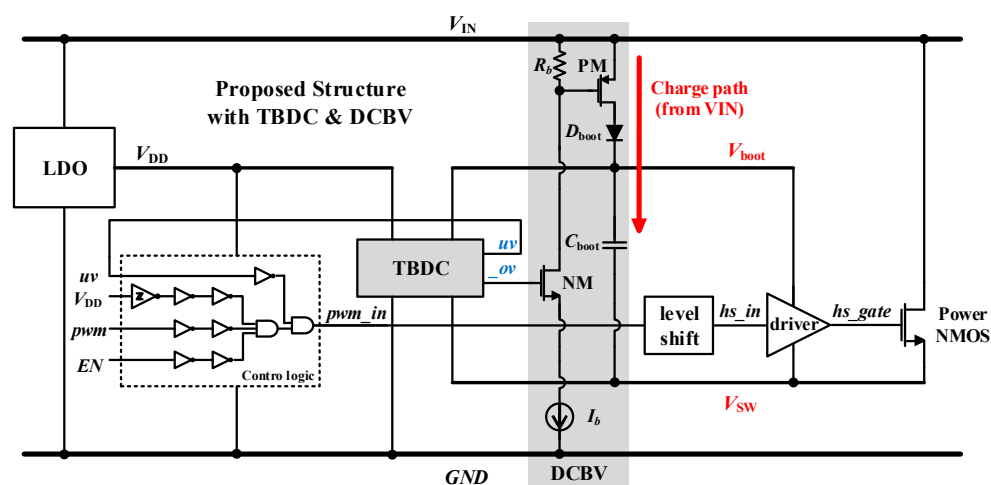


Figure 2. Proposed bootstrap structure with TBDC and DCBV.

When the TBDC detects that the bootstrap voltage is lower than the under-voltage threshold V_{THL} , the under-voltage signal uv will pull down the driving signal in the control logic circuit to turn off the power device, thereby avoiding the efficiency loss caused by insufficient driving voltage.

When the TBDC detects that the bootstrap voltage exceeds the over-voltage threshold V_{THH} , the non-over-voltage signal $_ov$ is set to 0, and the gate of the PMOS switch (PM) is pulled up to V_{IN} by the bias resistor R_b , resulting in the shutdown of PM and charging path. Moreover, the bootstrap voltage slowly decreases until the TBDC detects that the bootstrap is lower than the over-voltage threshold V_{THH} . Additionally, the $_ov$ signal remains high. The high-voltage NMOS (NM) is turned on, and the bias current I_b causes a voltage drop on the bias resistor R_b . Next, the PM is turned on, and the BUS voltage V_{IN} charges the bootstrap capacitor C_{boot} through the bootstrap diode D_{boot} . The charging path is shown as a red arrow, and the bootstrap voltage increases immediately. The above processes are repeated during normal operation. Due to a slight delay in the DCBV circuit, the bootstrap voltage is controlled within a voltage range with a small ripple ($V_{THH} \pm \Delta V$).

In the case of high-frequency operation, the traditional structure has relatively high requirements for the bandwidth and load regulation rate of the LDO. However, the structure designed in this work does not rely on an LDO power supply, which is more suitable for higher frequency.

The working sequence of this circuit is shown in Figure 3.

2.1.1. Power on (Under-Voltage)

When the BUS voltage V_{IN} is powered on, the LDO starts to work, and then the low-voltage power supply V_{DD} increases to 5 V as shown in Figure 3, status ①. The enable signal EN then turns from low to high. At this time, the external input signal pwm is low. The high-side power NMOS remains off, and the switch node V_{SW} is 0. Moreover, the bootstrap voltage is lower than the under-voltage threshold V_{THL} , and the under-voltage signal uv is the V_{DD} . The uv signal turns off the high-side N-type power device in the control logic circuit.

The $_ov$ signal is also the V_{DD} , so the bootstrap charging path is opened, and the bootstrap voltage increases.

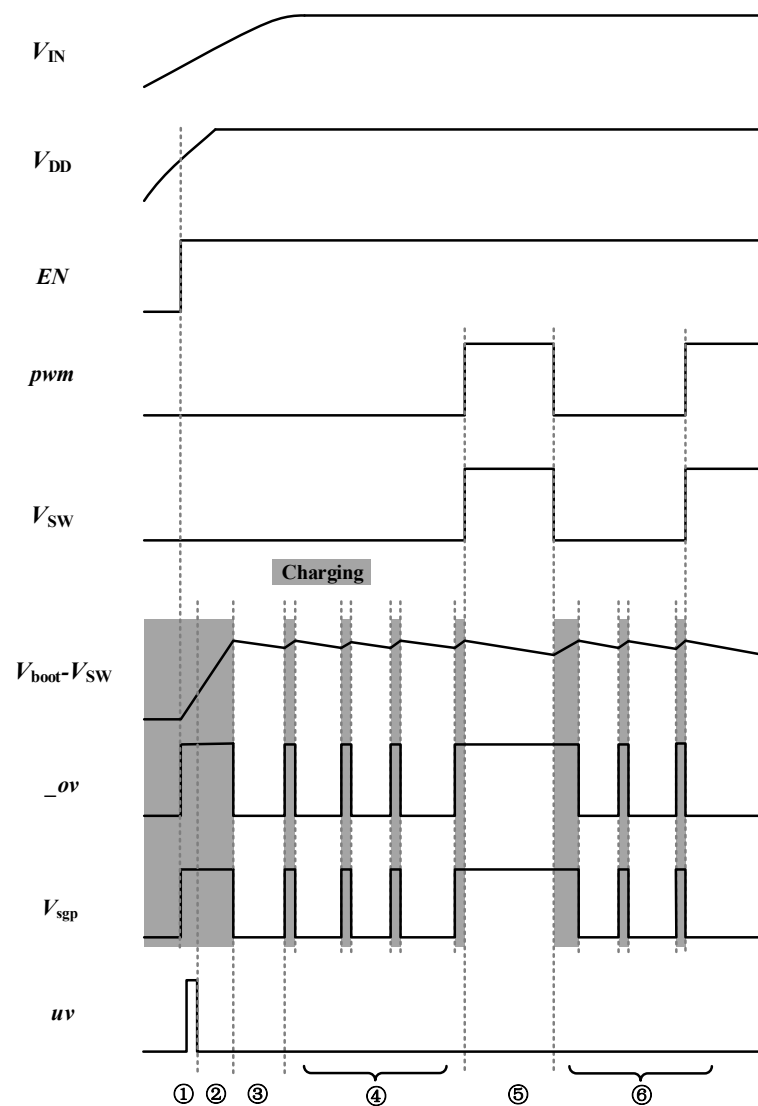


Figure 3. Working sequence of the proposed bootstrap structure.

2.1.2. Charging

When the bootstrap voltage increases to the under-voltage threshold V_{THL} as shown in Figure 3, status ②, the under-voltage signal uv reverses from the V_{DD} to the GND , and the pwm signal can normally control the high-side power NMOS.

Additionally, the $_ov$ signal is still the V_{DD} , and the bootstrap charging path remains open, causing the bootstrap voltage to continue increasing.

2.1.3. Discharging (Over-Voltage)

When the bootstrap voltage exceeds the over-voltage threshold V_{THH} as shown in Figure 3, status ③, the $_ov$ signal is flipped from the V_{DD} to the GND . Therefore, the charging path is turned off, and the bootstrap voltage slowly decreases.

2.1.4. Repeating (pwm Remains Low)

When the external input signal pwm continues to be low and the bootstrap voltage decreases to less than the over-voltage threshold V_{THH} as shown in Figure 3, status ④, processes Charging (status ②) and Discharging (status ③) are repeated.

2.1.5. *pwm* Becoming High

When the external input signal *pwm* becomes high, the high-side power NMOS is turned on, and the switch node V_{SW} voltage is pulled up to the BUS voltage V_{IN} as shown in Figure 3, status ⑤. At this time, since the voltage at the anode of the bootstrap diode D_{boot} is the BUS voltage V_{IN} and the voltage at the negative terminal of D_{boot} is the high-side bootstrap power rail voltage V_{boot} , the charging path cannot be charged. Additionally, the high-side bootstrap power rail slowly decreases due to the power supply to the high-side driver and the leakage of the bootstrap capacitor C_{boot} .

2.1.6. *pwm* Becoming Low

As status ⑥ shows in Figure 3, after the input signal *pwm* becomes low, processes *Charging* and *Discharging* are repeated, which behaves the same as status ④.

2.2. Circuit Realization

The TBDC circuit is used to detect the over-voltage and under-voltage conditions of the bootstrap voltage, which is composed of three parts as shown in Figure 4, including a current bias and start-up circuit, an under-voltage detection circuit, and an over-voltage detection circuit. In addition, level shifter and driver are shown in Figures 5 and 6, respectively.

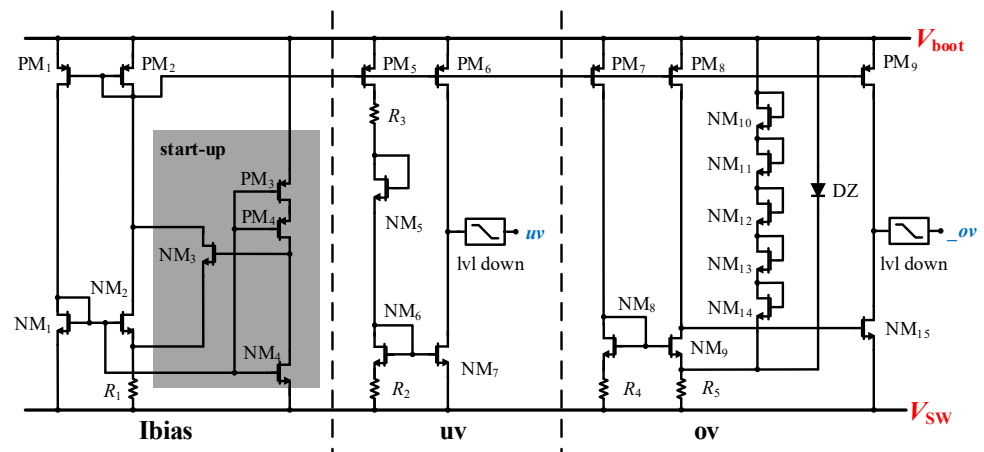


Figure 4. Circuit realization of the proposed TBDC with fully isolated devices.

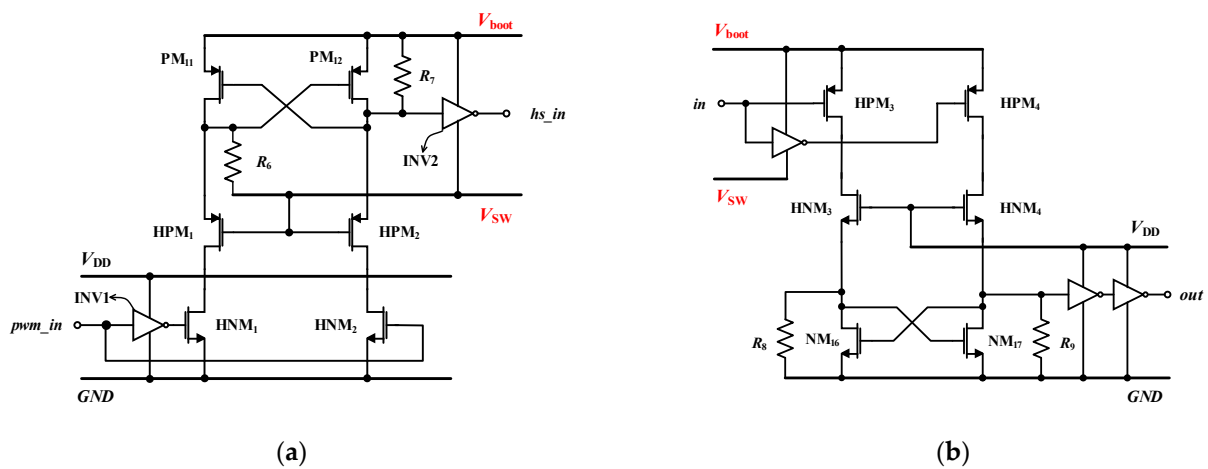


Figure 5. Circuit realization of (a) level-up shifter and (b) level-down shifter employed in proposed structure.

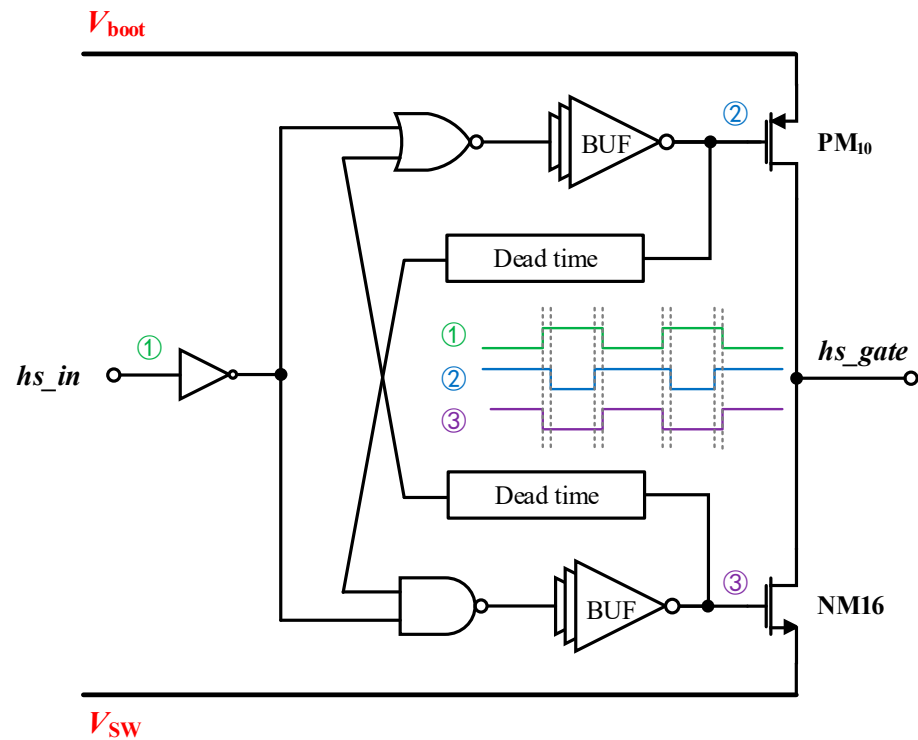


Figure 6. Circuit realization of driver and waveforms of hs_in , gate of PM_{10} and NM_{16} .

2.2.1. TBDC Circuit

- Current bias and start-up circuit

The current bias and start-up circuit are shown in the left part in Figure 4, which are composed of isolated PMOS PM_1 – PM_2 , isolated NMOS NM_1 – NM_2 , and a resistor R_1 . PM_1 mirrors the current of PM_2 , and resistor R_1 is used to control the magnitude of the bias current. The bias current increases as the bootstrap voltage increases until it stabilizes. The stable bias current is [30]:

$$I_{out} = \frac{2}{\mu_n C_{ox} (W/L)_1} \times \frac{1}{R_1^2} \times \left(1 - \frac{1}{\sqrt{K}}\right)^2 \quad (1)$$

where μ_n is the electron mobility of NM_1 , C_{ox} is the gate-oxide capacitance per unit area, $(W/L)_1$ is the ratio of width and length of NM_1 , and K is the ratio of NM_2 and NM_1 . The value of I_{out} is set to 1 μA to balance the power consumption and area. The length of NM_1 is set to 2 μm so that the channel length modulation effect can be reduced. The value of K is set to 32 and resistance of R_1 is about 170 $k\Omega$ by calculation. To avoid the degenerate state when the current is 0, a start-up structure is introduced with isolated NMOS NM_3 – NM_4 and isolated PMOS PM_3 – PM_4 . When the bias current is 0, the gate-source voltage V_{GS2} of NM_2 is 0 V. At this time, the gate voltages of PM_3 and PM_4 are 0 V, and they are turned on. Then, the gate of NM_3 is pulled high and turned on, and there is current that flows through resistor R_1 . Therefore, the bias current is not 0, and the degenerate state is eliminated. Once there is flowing current, the gate-source voltage V_{GS2} of NM_2 increases to a value greater than the threshold voltage V_{THN} , and then NM_4 is turned on. Moreover, the gate voltage of NM_3 is pulled down, and the start-up circuit is turned off.

- Under-voltage detection circuit

The under-voltage detection circuit is shown in the middle part of Figure 4, which is composed of isolated PMOS PM_5 – PM_6 , isolated NMOS NM_5 – NM_7 , resistors R_2 – R_3 , and a level shifter circuit.

As the bootstrap voltage gradually increases from 0, the bias current I_{out} rises. PM₅ mirrors the current of PM₂, and the gate-source voltage V_{GS5} of PM₅ is equal to the V_{GS2} of PM₂. Due to the existence of R_3 and PM₅, NM₆ cannot be turned on immediately at a low current. At this time, the drain voltage of PM₆ is pulled up to V_{boot} . After the first level shifter circuit, the output of the under-voltage signal uv is V_{DD} .

By adjusting the size of PM₅, NM₅, R_2 , and R_3 , the under-voltage threshold V_{THL} voltage can be set to 2.2 V to ensure a low on-resistance of the power NMOS. When the bootstrap voltage reaches V_{THL} , which can be expressed as:

$$V_{THL} = V_{DSP5} + V_{GSN5} + I_{out} \times (R_2 + R_3) + V_{THN} \quad (2)$$

NM₆ and NM₇ are turned on, and the drain voltage of NM₇ gradually decreases until it is lower than the threshold of the level shifter. At this time, the output of the under-voltage signal uv is GND . In this case, NM₅ is assumed to be critical saturation, and V_{DSP5} could be set to the overdrive voltage (about 200 mV to 300 mV). V_{THN} is about 900 mV, and V_{GSN5} should be larger than threshold voltage. The above data are substituted in equation 2, and then the value of R_2 and R_3 is estimated at about 200 K Ω .

- Over-voltage detection circuit

Isolated PMOS PM₇-PM₉, isolated NMOS NM₈-NM₁₅, resistors R_4 - R_5 , Zener diode DZ, and another level shifter circuit constitute an over-voltage detection circuit, as shown in the right part of Figure 4.

The gate voltage of NM₉ is a fixed value when the bias current I_{out} is determined, which is:

$$V_{GN9} = I_{out} \times R_4 + V_{GSN8} \quad (3)$$

The source voltage of NM₉ is:

$$V_{SN9} = V_{boot} - (V_{GSN10} + V_{GSN11} + V_{GSN12} + V_{GSN13} + V_{GSN14}) = V_{boot} - 5 \times V_{GSN} \quad (4)$$

Therefore, the gate-source voltage of NM₉ is:

$$V_{GSN9} = I_{out} \times R_4 + V_{GSN8} + 5 \times V_{GSN} - V_{boot} \quad (5)$$

When the gate-source voltage of NM₉ is lower than V_{THN} , NM₉ will be turned off, and the gate voltage of NM₁₅ will be pulled up to V_{boot} , while the drain voltage will be pulled low. Therefore, the output of ov signal is GND after the level shifter circuit. Therefore, the over-voltage threshold is deduced as:

$$V_{THH} = I_{out}R_4 + 5 \times V_{GSN} + V_{GS8} - V_{THN} \quad (6)$$

However, there is another device, a Zener diode DZ, used in the over-voltage circuit, which double guarantees ov signal to be low during its over-voltage. DZ will clamp the source voltage of NM₉ through providing enough current when the bootstrap voltage reaches its threshold. At this time, the threshold voltage is:

$$V'_{THH} = V_{DZ} + I_{out}R_4 \quad (7)$$

where V_{DZ} is the clamp voltage of Zener diode.

The constant current of this circuit is set to 1 μA each branch, and the size of PM₇ and PM₈ is the same as PM₁ and PM₂. By adjusting the size of NM₈, NM₁₀-NM₁₄, and R_4 , the V_{THH} voltage is set to 6 V, thereby avoiding the breakdown of the power NMOS.

The TBDC circuit is designed with fully isolated devices due to area consideration, and the bootstrap capacitor is directly charged from the BUS voltage with the DCBV circuit, which can be used for higher frequency. Due to the usage of a digital control method, the bootstrap voltage is stable when V_{IN} varies from 6 V to 48 V; therefore, the line regulation of this circuit can be considered close to 0.

2.2.2. Level Shifters

There are two types of level shifters employed in the proposed bootstrap structure. One is a level-up shifter used to control the power NMOS, and the other is a level-down shifter in the TBDC circuit.

- Level-up shifter

The *pwm_in* signal is the output of control logic, and it is 3.3 V or 5 V relative to ground, which is not suitable to control the driver directly. Therefore, the level-up shifter is adopted to shift the voltage relative to ground to the voltage relative to V_{SW} . The level-up shifter used in the proposed structure is illustrated in Figure 5a. HPM_1 , HPM_2 , HNM_1 , and HNM_2 are the only high-voltage devices in this circuit, and other devices are low-voltage devices (INV1) or isolated devices (PM_{11} , PM_{12} and INV2). R_7 is a pull-up resistor to ensure the initial condition of *hs_in*, preventing from floating gate of INV2.

- Level-down shifter

A level-down shifter is used in the TBDC circuit to shift the *uv* and *_ov* signal from floating voltage to voltage relative to ground, so that *uv* can be an input of control logic and *_uv* is appropriate for controlling NM in the DCBV. The principle of the level-down shifter is similar to that of the level-up shifter, and the circuit is shown in Figure 5b.

2.2.3. Driver

The driver circuit shown in Figure 6 provides sufficient driving current for the power device through PM_{10} and NM_{16} . The source and sink current are determined by the gate capacitance C_{GS} of the power device, turn-on/off voltage of the power device and required rising/falling time, and can be adjusted by changing the size of PM_{10} and NM_{16} . Deadtime is used to prevent the power rail from shooting through, and the waveforms of *hs_in*, gate of PM_{10} , and NM_{16} are also shown in Figure 6.

3. Results

The circuit is implemented by the CSMC 0.25 μm 60 V BCD process. Figure 7 shows the micrograph and testbench photos using the proposed bootstrap structure. The chip area is $1.4 \times 1.3 \text{ mm}^2$, of which the bootstrap circuit only occupies 0.149 mm^2 . The maximum input voltage can be up to 48 V, and the operating frequency can reach 5 MHz.

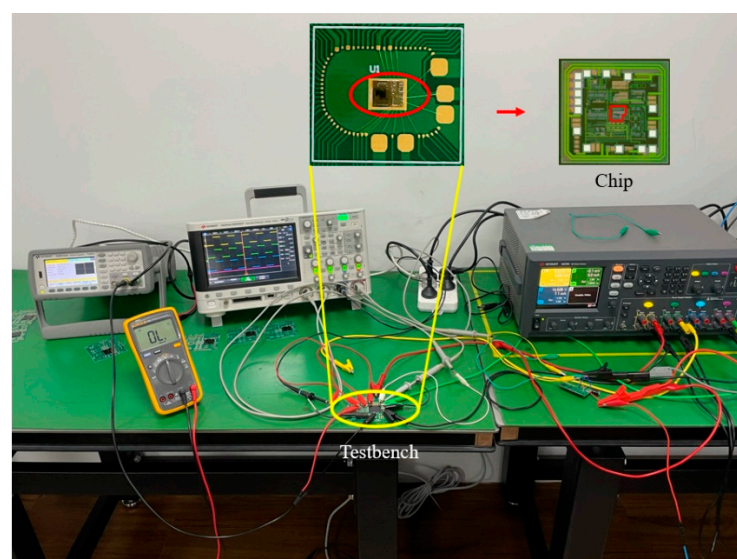


Figure 7. Chip micrograph and testbench of the buck converter with the proposed bootstrap circuit.

3.1. Simulation Results

Figure 8 shows the DC simulation result of the TBDC circuit. When the bootstrap voltage is lower than V_{THL} (2.101 V), uv and ov are high. When the voltage is between the V_{THL} and V_{THH} (2.101–6.099 V), the uv output is low and the ov output is high. When the voltage between V_{boot} and V_{SW} is higher than the V_{THH} (6.099 V), the uv output is low and the ov output is low.

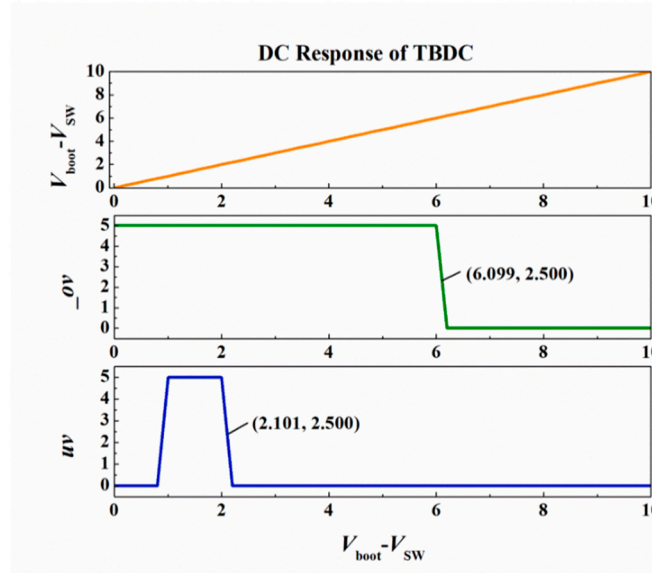


Figure 8. Simulated DC under-voltage and over-voltage threshold of TBDC.

The overall and enlarged simulation results are shown in Figure 9a,b. When the pwm is 0 and the bootstrap voltage is higher than V_{THH} (6 V), the output of the ov signal is 0 V and NM is turned off. Therefore, there is no voltage drop on the bias resistor R_b , and the voltage of V_{SGP} is 0 V, which causes the charging path to be turned off. When the bootstrap voltage is lower than V_{THH} , the output of the ov signal is 5 V and NM is turned on. A voltage drop can be formed on the bias resistor R_b , and the voltage of V_{SGP} can increase to 3 V, causing the charging path to be opened. However, the voltage of V_{SGP} only increases to 3 V instead of 5 V, which can be attributed to the fact that the bootstrap voltage is quickly charged to 6 V by the V_{IN} when the PM is turned on. During this period, the ripple of $V_{boot} - V_{SW}$ is only 1.583 mV.

The temperature simulation result is shown in Figure 10a. The minimum bootstrap voltage is 5.866 V at -40°C , and the maximum bootstrap voltage is 6.210 V at 120°C . The bootstrap voltage is positively correlated with the temperature, and the temperature coefficient is calculated as:

$$TC = \frac{\Delta V_{out}}{(T_{max} - T_{min}) \times V_{nom}} \times 10^6 = 348 \text{ ppm}/^\circ\text{C} \quad (8)$$

The simulation results for different load currents are shown in Figure 10b, indicating a good load regulation. The maximum bootstrap voltage is 6.210 V at 1 A, and the minimum voltage is 6.208 V at 1 mA. The load regulation S_v can be calculated as:

$$S_v = \frac{\Delta V_{out}}{V_{nom} \times \Delta I_{out}} = 0.03\%/mA \quad (9)$$

The simulated result of the buck converter at $I_{load} = 1 \text{ A}$ configured by this bootstrap structure is shown in Figure 11. The input and output voltages are 14.5 V and 5 V, respectively. The ripple of the output voltage is 2.612 mV with an efficiency of 92.7%. The highest simulated efficiency is 94.87% at 600 mA.

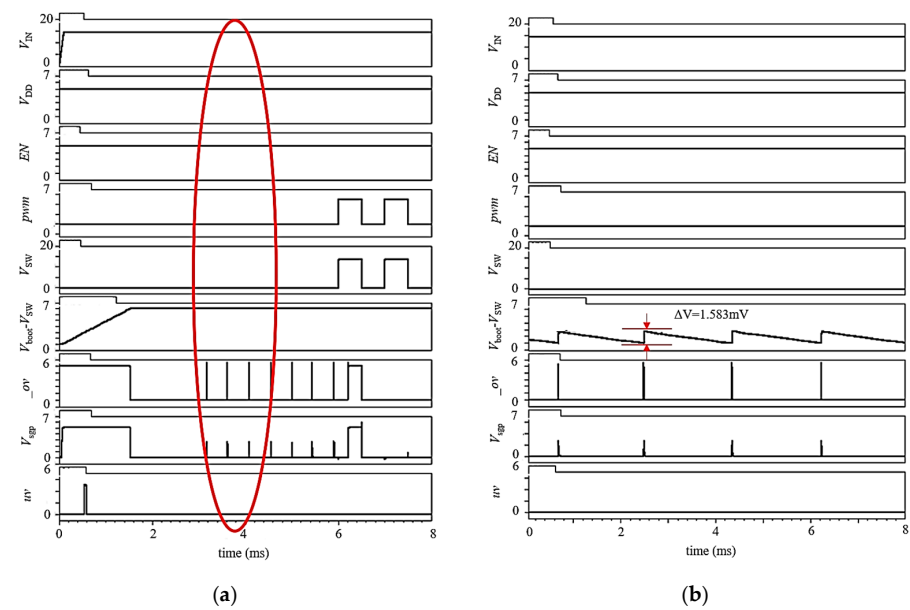


Figure 9. Simulated results of the proposed bootstrap structure: (a) overall result and (b) enlarged result.

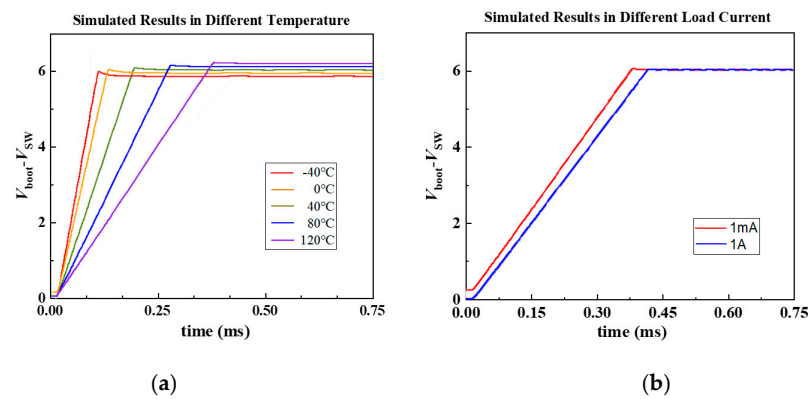


Figure 10. Simulation result at (a) different temperature ($T = -40^\circ\text{C}$, 0°C , 40°C , 80°C and 120°C) and (b) different load current ($1\text{ }\mu\text{A}$ and 1 mA).

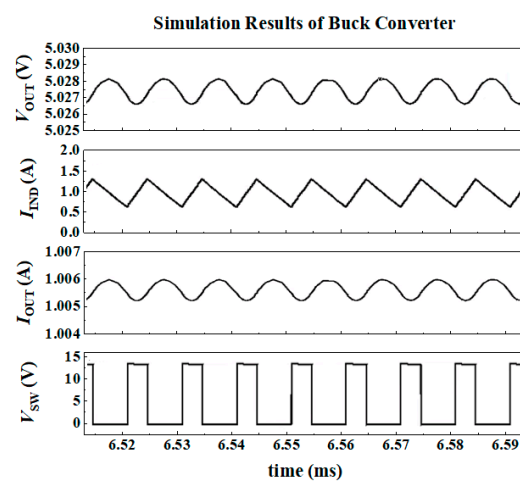


Figure 11. Simulation results of buck converter ($V_{IN} = 14.5\text{ V}$, $V_{OUT} = 5\text{ V}$, $I_{load} = 1\text{ A}$).

3.2. Test Results

The test result, as shown in Figure 12a, indicates that the voltage power-up time of bootstrap voltage is approximately 170 μ s, and the stable voltage is approximately 6 V, which are consistent with the simulation result. The results of different operation frequencies are shown in Figure 12b, indicating good support over a wide frequency range.

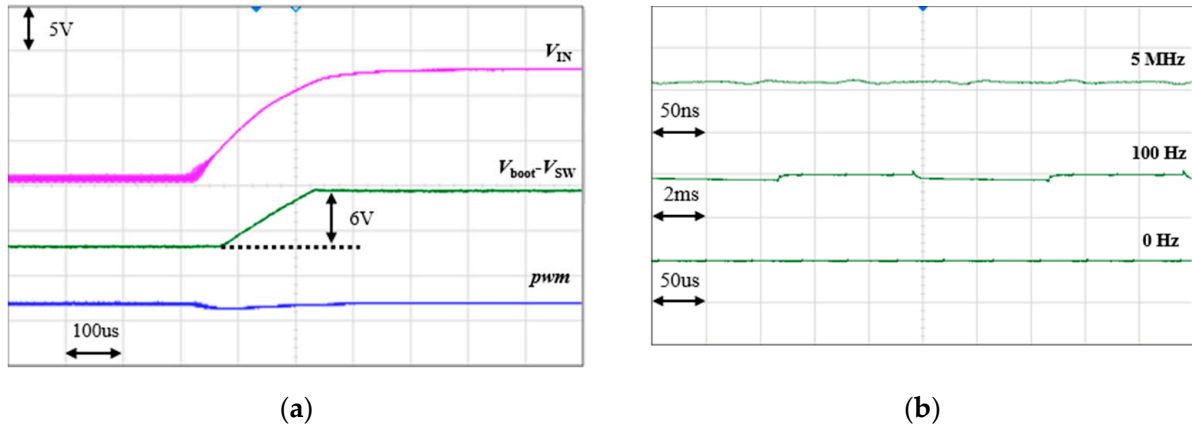


Figure 12. Measured bootstrap circuit (external $C_{boot} = 1 \mu F$) (a) power on and stable state, and (b) bootstrap voltage at $pwm = 0$ Hz, 1 MHz, and 5 MHz.

A comparison of the simulation and actual measurement results of the buck converter are shown in Figure 13. Under the following conditions, $V_{IN} = 14.5$ V and $V_{OUT} = 5$ V, the highest tested efficiency of the circuit is 83.6% ($I_{load} = 400$ mA). The figure-of-merit (FOM) is defined as:

$$FOM = \frac{A}{I_{load,max} \times \eta^{0.5}} \quad (10)$$

where A is the silicon area, $I_{load,max}$ is the maximum load, and η is the efficiency at maximum load [31]. For this definition, a low value indicates a better performance and the circuit achieves a good FOM of 0.074. Due to diode conduction loss, MOS conduction loss, and MOS switching loss, there is a certain gap between the simulation results and the actual measurement results.

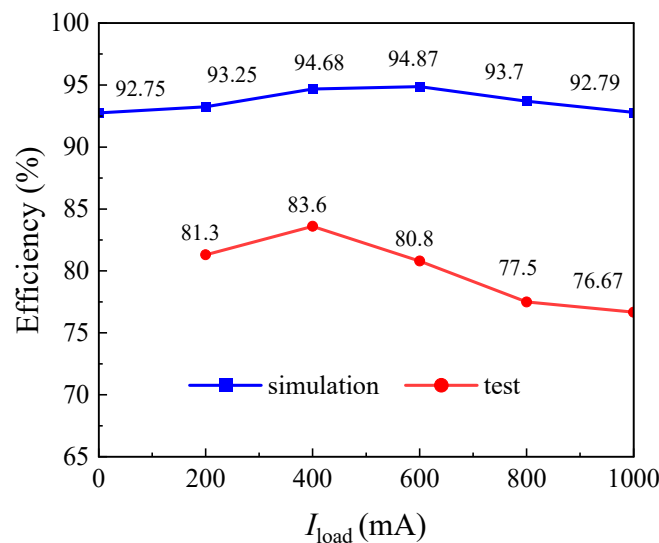


Figure 13. Comparison between the simulated and test results of the buck converter efficiency at different currents ($V_{IN} = 14.5$ V, $V_{OUT} = 5$ V).

4. Discussion

Table 1 shows the comparison results between the structure designed in this paper and those reported in previous literature. Compared with the previous research, this work has the advantages of a wider input voltage from 3.6 V to 48 V, higher switching frequency up to 5 MHz, larger output current of 2.7 A, and a smaller chip area of 1.82 mm² with a good FOM of 0.074 while maintaining the same efficiency. With the digital control method being different from previous research, the simulation and test result implicate that the novel DCBV and TBDC methods in the proposed bootstrap structure is feasible and stable. The proposed circuit can be applied to some power areas such as dc–dc converters.

Table 1. Comparison with previously published works is shown, indicating wider input voltage, higher switching frequency, larger output current, and smaller chip area with a good FOM while maintaining the same efficiency.

Parameter	This Work	Ref [23]	Ref [32]	Ref [22]
Technology (μm)	0.25 μm 60 V BCD	0.35 μm 40 V CMOS	0.18 μm HV BiCMOS	0.35 μm HV BCD
Input voltage V_{IN} (V)	3.6–48	3.6–36	15	3–40
Switching frequency (MHz)	0.1–5	0.2–2.4	2	10–30
Output current (A)	2.7	2	2.6	1.2
Efficiency η (%)	83.6	85.98	N/A	N/A
Chip area A (mm ²)	1.82	4.78	N/A	N/A
Bootstrap circuit area (mm ²)	0.149	0.062	0.42	0.48
Dropout voltage (mV)	1.583 (simulation)	4.6 (simulation)	N/A	N/A
LDO type	Capless	Capless	External cap	N/A
FOM ($A/I_{load,max} \times \eta^{0.5}$)	0.074	0.258	N/A	N/A
Bootstrap rail control	TBDC	DVS	N/A	ABB

However, due to the lack of research on temperature compensation, the temperature coefficient of this structure is not as low as traditional LDOs. Therefore, future research on this circuit include decreasing the temperature coefficient and scaling higher power.

5. Conclusions

Bootstrap is a key structure for driving and protecting a high-side N-type power device. In this paper, a novel bootstrap circuit has been proposed, which is directly charged by the BUS voltage and employs a digital method to achieve a stable output. With an area of 1.82 mm², this structure exhibits strict voltage control in a wide range of input voltages and frequencies. It is found that when using the dc–dc asynchronous buck converter, the maximum efficiency of the prototype is 83.6%, and the FOM is 0.074, showing its future potential in a wide range of scenarios, such as in power converters, motor drivers, and automobiles.

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