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Modeling of Average Current in Non-Ideal Buck and Synchronous Buck Converters for Low Power Application

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Abstract: In this paper, a comparative analysis of the average switch/inductor current between ideal and non-ideal buck and synchronous buck converters is performed and verified against a standard LTspice model. The mathematical modeling of the converters was performed using volt-sec and amp-sec balance equations and analyzed using MATLAB/Simulink. The transients in the output voltage and the inductor current were observed. The transfer function of the switch current to the duty cycle (G_{id}) in open loop configuration for low-power converters operating in continuous conduction mode (CCM) was modeled using thestate space averaging (SSA) technique and analyzed using MATLAB/Simulink. Initially, using the volt-sec and amp-sec, balance equations for the converters were modeled. The switch current to duty ratio (G_{id}) was derived using the SSA technique and verified using standard average models available in LTspice software. Though the G_{id} was derived using various methods in earlier works, the analyses of parameters such as low frequency gain, stability, resonant frequency and the location of poles and zeros were not presented. It was observed that the converters were stable, and the non-ideal converter showed smaller resonant frequency than the ideal converter due to the equivalent series resistances (ESR) of the inductor and the capacitor. The non-ideal converters showed higher stability than the ideal converters due to the placement of the poles closer to the s-plane. However, the G_{id} of the non-ideal converters remained the same in the open loop configuration.

Keywords: average current control; continuous conduction mode; LTspice; MATLAB/Simulink; mathematical modeling; non-ideal buck converter; non-ideal synchronous buck converter

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1. Introduction

The average current control (ACC) of DC–DC converters plays a vital role in designing PFC (power factor correction) converters, DC–AC inverters, electric vehicle (EV) chargers, LED lighting, etc. The most popular control methods for maintaining the unity power factor for DC–DC converters are shown in Figure 1.

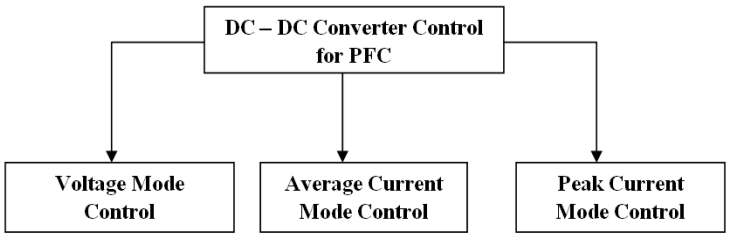

Figure 1. DC–DC converter control for PFC.

The current control of DC–DC converters consists of two categories, namely ACC and peak current mode (PCM) control. In ACC, variation in the perturbed inductor current with respect to the perturbed duty ratio is considered. Though ACC cannot provide instantaneous control, some of the advantages of ACC over PCM include (a) better noise immunity and (b)possible control for a wide range of applications. In the past, multiple attempts have been made in modeling the open loop transfer function of average current for different converters operating in CCM and discontinuous conduction mode (DCM) operations. The modeling approach for CPM (Current Programmed Mode) was clearly shown for buck and boost regulators using the generalized small signal model. The small signal modeling approach for the basic converters and the modeling approach of the ACC for an ideal boost converter was presented in [1–3].

Electric vehicle (EV) charging systems, power factor correction (PFC) circuits, LED drivers, power supplies for processors etc., are some of the applications of DC–DC converters. The various AC–DC and DC–DC converters used in EVs are shown in [4]. Zero voltage (ZV) and zero current (ZC) switched DC–DC converters are the most popular converters used in the EV industry. For the generation of high gain, a KY converter integrated with the boost converter is used as it provides low current ripple and high efficiency.

In the average current control, capturing the inductor or the switch current is extremely critical. One of the major applications of the ACC is power factor control [5]. In [6], a novel method for measuring the inductor current is proposed for digitally controlled synchronous buck converters based on switch node voltage. To estimate the inductor current, switch node voltage is measured using a digital comparator. The inductor average current and the current ripple contents are simultaneously estimated as having independent gains. The estimation of the current ripple was validated against the hysteretic current mode control ofthe synchronous buck converter. However, no information on the low frequency gain during the open loop configuration was discussed.

In order to study the dynamics of the converter, modeling and simulation are extremely important. Transient values obtained through modeling help in designing the critical elements such as the inductor and the capacitor [7]. This type of modeling provides an insight on steady-state and transient behaviors.

The DC–DC converters used for battery charging applications are Cuk and Single Ended Primary Converter (SEPIC). The functioning of such switched converters under CCM and DCM conditions was modeled using the LTspice software tool [8]. These switch models require less computation time and memory for estimating frequency responses such as the G_{id}, G_{vd} and G_{vg}. The converters showed instability during the CCM operation. However, they showed high stability during DCM operation.

In [9], a synchronous buck converter operating in CCM was used as a battery charging application. A PID controller was implemented instead of a maximum power point tacking (MPPT) algorithm to observe the charging of a lead acid battery at various irradiance levels. Though simulations show that MPPT provides better results, the PID controller has faster charging and lower costs. In [10], the DCM analysis for the Cuk and SEPIC converter operating in DCM was carried out. It was shown that the converter was unstable for G_{vd} operations in an open loop. Hence, during the closed loop operation the controller should (a) stabilize the system and (b) provide enough phase margin (PM) to achieve stability in closed loop configuration.

The modeling of an ideal and non-ideal buck converter operating in CCM was performed for an open loop configuration [11]. The output voltage and the inductor current were smaller in the non-ideal buck converter. The non-ideal buck converter showed a greater number of zeros than the ideal buck converter. However, the modeling and analysis of the synchronous buck converter were not discussed.

The modeling of the G_{id} in open loop configuration for boost and synchronous boost converters is presented in [12]. It was shown that the G_{id} for the non-ideal synchronous boost converter showed higher resonance than the non-ideal boost converter.

Frequency control techniques have been employed in DC–DC converters to keep the switching frequency constant, instead of a phase-locked loop (PLL) [13]. The objective of frequency response identification for DC–DC converters is to ensure high accuracy, flexible operation in open or closed loop modes, and the optimal performance of the converter [14]. In [15], the authors proposed a wide input voltage range DC–DC converter for auxiliary power supplies on solar power conversion circuits or railway vehicles, making use of the buck/boost and resonant circuits to realize this wide range. The authors in [16] designed a four-switch buck–boost (FSBB) converter with a wide input voltage range voltage conversion, catering to variable-speed energy storage systems with AC inputs and DC outputs. The switching average model is used to establish the small signal model of a non-ideal FSBB converter in all working conditions. A digital control strategy [17] is modeled and implemented for a multi-leg interleaved DC–DC buck converter for electrical vehicle (EV) charging based on a discrete averaged model. The control system objective is the current flow regulation in each leg of the converter. Point-of-load applications require a lower-level distribution voltage. However, the control is not easy, which is why there is a need to choose the right fixed frequency for the buck regulator control [18,19]. Moreover, the control loop compensation [20,21] cannot be overlooked, and the impact of the phase margin is significant. The crossover frequency affects the output impedance. In some cases [22], small signal averaging for variable switching frequency DC–DC converters is derived by separately considering the on-time and the off-time of the switching period. This is used to ensure very good voltage regulation and optimal dynamic performance. The converters used in EV industry and cyber security are shown in [23–26] and closed loop control using classical controllers is shown in [27]

- The existing works featured on steady-state and transient performance analysis of the DC–DC ideal and non-ideal converters for low-power application based on the specifications shown in [11].
- The G_{id} for a current loop is considered. However, the outer voltage loop is not taken into account.
- The G_{id} of a non-ideal buck converter was compared with a non-ideal synchronous buck converter. Sensitivity analysis of the G_{id} was carried out by analyzing the bode plots for varying ESR.
- The modeling of the converters was presented considering all the non-idealities such as the switch and diode resistances and ESRs of inductor and capacitor.
- However, very few works have focused on the mathematical modeling of the average current control strategy for the same.

In this paper,

- The average current model for ideal and non-ideal buck and synchronous buck converters is modeled using the SSA technique.
- The emphasis is on modeling the G_{id} and observations are made on low frequency gain, crossover frequency, resonant frequency, location of poles and zeros, and gain and phase margins.
- The objective of the work is to aid the understanding and significance of mathematical modeling and the effect of the G_{id} on this proposed strategy and its significance in stability and control.

The paper is organized as follows: Section 1 provides the motivation and background of the proposed work. Sections 2 and 3 establish the mathematical foundation of the average current control strategy for the non-ideal buck and the non-ideal synchronous buck converter. Section 4 provides the specifications of the converter. Section 5 shows the mathematical modeling of the converters. Section 6 shows the analyses of the results obtained for the ACC in open-loop mode for both converters. Section 7 provides the validation of the same in the LTspice platform followed by the conclusion and future scope.

2. Average Current Modeling in Non-Ideal Buck Converter

Figure 2 shows the block diagram representation of the ACC in an ideal buck converter where $\hat{i}_L$ and $\hat{d}$ represent perturbed indictor current and duty cycle. The gate driver supplies the gate pulses to control the switching of MOSFET.

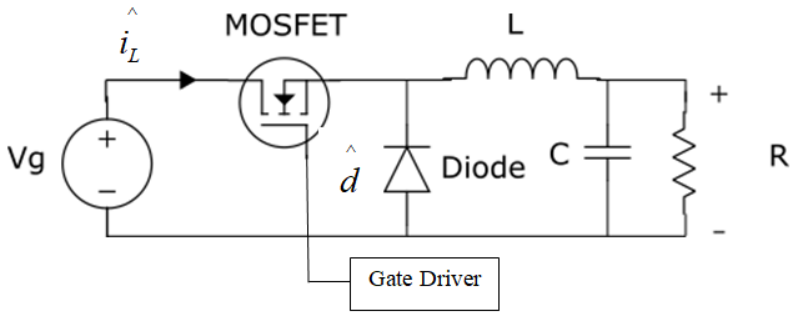

Figure 2. Schematic of ACC in open loop [3].

Figure 3 shows a non-ideal/practical buck converter. The operation of the converter can be defined when the switch is closed and opened. The output voltage of the converter is V_0. The working of the converter and the mathematical model of the ideal converter are presented in [7].

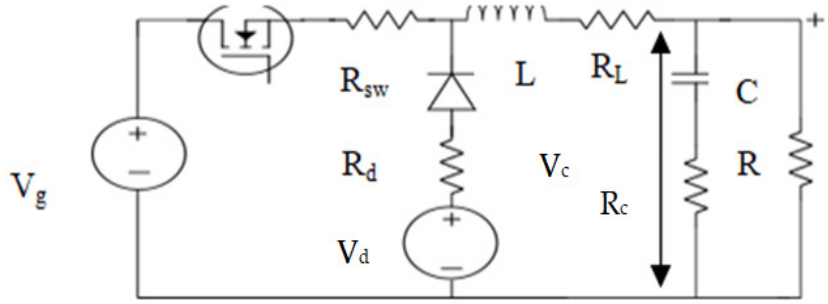

Figure 3. Schematic of the converter.

Switch closed condition,

$$V_g - i_L(R_{sw} + R_L) - V_c = V_L \tag{1}$$

$$i_L - \frac{V_0}{R} = i_c \tag{2}$$

$$V_0 = V_c + i_c R_c \tag{3}$$

(2) in (3),

$$V_0 = \frac{V_c R}{R + R_c} + \frac{i_L R R_c}{R + R_c} \tag{4}$$

(4) in (2),

$$i_c = i_L(1 - \frac{R_c}{R + R_c}) - V_c(\frac{1}{R + R_c}) \tag{5}$$

The state space representation is given by (6) and (7),

$$\overset{\circ}{X} = AX + BU \tag{6}$$

$$Y = CX + DU \tag{7}$$

Representing (1) and (2) in the form of (3) and (4),

$$\begin{bmatrix} di_L/dt \\ dV_c/dt \end{bmatrix} = \begin{bmatrix} \frac{-\left(R_L+R_{sw}+\frac{RR_c}{R+R_c}\right)}{L} & \frac{-R}{L(R+R_c)} \\ \frac{R}{C(R+R_c)} & \frac{-1}{C(R+R_c)} \end{bmatrix} \begin{bmatrix} i_L \\ V_c \end{bmatrix} + \begin{bmatrix} \frac{1}{L} & 0 \\ 0 & 0 \end{bmatrix} \begin{bmatrix} V_g \\ V_d \end{bmatrix} \tag{8}$$

The output considered is the inductor current i_L. Hence,

$$[i_L] = [1\ 0] \begin{bmatrix} i_L \\ V_c \end{bmatrix} \tag{9}$$

where

$$A_1 = \begin{bmatrix} \frac{-\left(R_L+R_{sw}+\frac{RR_c}{R+R_c}\right)}{L} & \frac{-R}{L(R+R_c)} \\ \frac{R}{C(R+R_c)} & \frac{-1}{C(R+R_c)} \end{bmatrix} \tag{10}$$

$$B_1 = \begin{bmatrix} \frac{1}{L} & 0 \\ 0 & 0 \end{bmatrix} \tag{11}$$

$$C_1 = \begin{bmatrix} 1 & 0 \end{bmatrix} \tag{12}$$

$$U = \begin{bmatrix} V_g \\ V_d \end{bmatrix} \tag{13}$$

$$D_1 = 0 \tag{14}$$

Switch opened condition,

$$-i_L R_d - V_d - V_L - i_L R_L - V_0 = 0 \tag{15}$$

$$i_c = i_L - \frac{V_0}{R} \tag{16}$$

$$V_0 = i_c R_c + V_c \tag{17}$$

$$V_L = -i_L(R_d + R_L + \frac{RR_c}{R+R_c}) - V_d - \frac{RV_c}{R+R_c} \tag{18}$$

$$i_c = i_L(1 - \frac{R_c}{R+R_c}) - \frac{V_c}{R+R_c} \tag{19}$$

Reducing it to the form shown in (6) and (7),

$$A_2 = \begin{bmatrix} \frac{-\left(R_d+R_L+\frac{RR_c}{R+R_c}\right)}{L} & \frac{-R}{L(R+R_c)} \\ \frac{R}{C(R+R_c)} & \frac{-1}{C(R+R_c)} \end{bmatrix} \tag{20}$$

$$B_2 = \begin{bmatrix} 0 & \frac{-1}{L} \\ 0 & 0 \end{bmatrix} \tag{21}$$

$$C_2 = \begin{bmatrix} 1 & 0 \end{bmatrix} \tag{22}$$

$$A = A_1 D + A_2(1-D) \tag{23}$$

$$A = \begin{bmatrix} \frac{-\left(DR_{sw}+R_d(1-D)+R_L+\frac{RR_c}{R+R_c}\right)}{L} & \frac{-R}{L(R+R_c)} \\ \frac{R}{C(R+R_c)} & \frac{-1}{C(R+R_c)} \end{bmatrix} \tag{24}$$

$$B = (A_1 - A_2)X + (B_1 - B_2)U \tag{25}$$

$$\frac{\hat{i_L}}{\hat{d}} = C[sI - A]^{-1}B \tag{26}$$

$$(sI - A)^{-1}\Delta = \begin{bmatrix} s + \frac{1}{C(R+R_c)} & \frac{-R}{L(R+R_c)} \\ \frac{R}{C(R+R_c)} & s + \frac{DR_{sw}+R_d(1-D)+R_L+\frac{RR_c}{R+R_c}}{L} \end{bmatrix} \quad (27)$$

where

$$\Delta = s^2 + \frac{s}{C(R+R_c)} + \frac{s(DR_{sw}+R_d(1-D)+R_L+\frac{RR_c}{R+R_c})}{L} + \frac{1}{LC(R+R_c)}\left\{DR_{sw} + R_d(1-D) + R_L + \frac{RR_c}{R+R_c}\right\} + \frac{R^2}{LC(R+R_c)^2} \quad (28)$$

$$\frac{\hat{i_L}}{\hat{d}} = \frac{(s + \frac{1}{C(R+R_c)})[(\frac{I_L(R_d-R_{sw})}{L}) + \frac{V_g+V_d}{L}]}{\Delta} \quad (29)$$

where

$$I_L = V_0/R \quad (30)$$

3. Average Current Modeling in Non-Ideal Synchronous Buck Converter

Figure 4 shows a non-ideal/practical synchronous buck converter. In such converters, the conduction losses are reduced as $V_{MOSFET} < V_{Diode}$.

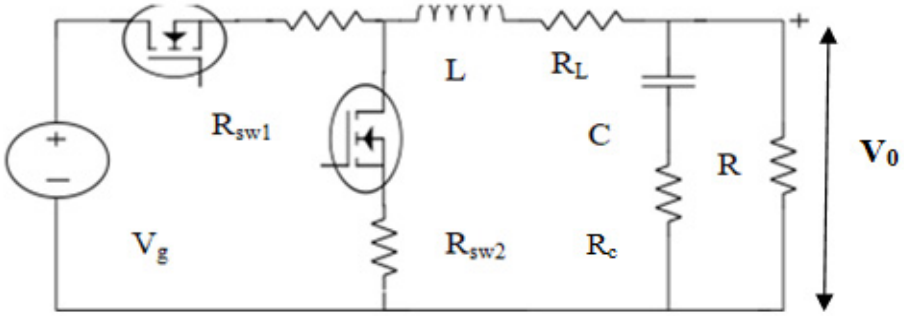

Figure 4. Schematic of the converter.

Switch closed condition,

$$V_L = V_g - i_L(R_{sw1} + R_L + \frac{RR_c}{R+R_c}) - \frac{RV_c}{R+R_c} \quad (31)$$

$$i_c = i_L\frac{R}{R+R_c} - \frac{V_c}{R+R_c} \quad (32)$$

$$\begin{bmatrix} di_L/dt \\ dV_c/dt \end{bmatrix} = \underbrace{\begin{bmatrix} \frac{-(R_L+R_{swl}+\frac{RR_c}{R+R_c})}{L} & \frac{-R}{L(R+R_c)} \\ \frac{R}{C(R+R_c)} & \frac{-1}{C(R+R_c)} \end{bmatrix}}_{A_1} \begin{bmatrix} i_L \\ V_c \end{bmatrix} + \underbrace{\begin{bmatrix} \frac{1}{L} & 0 \\ 0 & 0 \end{bmatrix}}_{B_1} \begin{bmatrix} V_g \\ 0 \end{bmatrix} \quad (33)$$

Switch opened condition,

$$V_L = -i_L(R_{sw2} + R_L + \frac{RR_c}{R+R_c}) - \frac{RV_c}{R+R_c} \quad (34)$$

$$i_c = i_L(\frac{R}{R+R_c}) - \frac{V_c}{R+R_c} \quad (35)$$

$$\begin{bmatrix} di_L/dt \\ dV_c/dt \end{bmatrix} = \underbrace{\begin{bmatrix} \frac{-(R_L+R_{swl}+\frac{RR_c}{R+R_c})}{L} & \frac{-R}{L(R+R_c)} \\ \frac{R}{C(R+R_c)} & \frac{-1}{C(R+R_c)} \end{bmatrix}}_{A_2} \begin{bmatrix} i_L \\ -V_c \end{bmatrix} + \underbrace{\begin{bmatrix} 0 & 0 \\ 0 & 0 \end{bmatrix}}_{B_2} \begin{bmatrix} V_g \\ 0 \end{bmatrix} \quad (36)$$

$$A = A_1D + A_2(1-D) \quad (37)$$

$$A = \begin{bmatrix} \frac{-\left(DR_{swl}+R_L+R_{sw2}(1-D)+\frac{RR_c}{R+R_c}\right)}{L} & \frac{-R}{L(R+R_c)} \\ \frac{R}{C(R+R_c)} & \frac{-1}{C(R+R_c)} \end{bmatrix} \quad (38)$$

$$\Delta(sI-A)^{-1} = \Delta \begin{bmatrix} s+\frac{1}{C(R+R_c)} & \frac{-R}{L(R+R_c)} \\ \frac{R}{C(R+R_c)} & s+\frac{DR_{swl}+R_L+R_{sw2}(1-D)+\frac{RR_c}{R+R_c}}{L} \end{bmatrix} \quad (39)$$

$$\Delta = s^2 + \frac{s}{C(R+R_c)} + \frac{s}{L}(DR_{sw1}+R_L+R_{sw2}(1-D)+\frac{RR_c}{R+R_c})+ \frac{1}{LC(R+R_c)}(DR_{sw1}+R_L+R_{sw2}(1-D)+\frac{RR_c}{R+R_c})+\frac{R^2}{LC(R+R_c)^2} \quad (40)$$

$$U = \begin{bmatrix} V_g \\ 0 \end{bmatrix} \quad (41)$$

$$\frac{\hat{i_L}}{\hat{d}} = C\{sI-A\}^{-1} * ([A_1-A_2]X+[B_1-B_2]U) \quad (42)$$

$$= \frac{(s+\frac{1}{C(R+R_c)})(\frac{V_0}{RL} * (R_{sw2}-R_{sw1})+\frac{V_g}{L})}{\Delta} \quad (43)$$

4. Specifications of the converter

Table 1 shows the specifications of the converters.

Table 1. Specifications of the converters.

SL.NO	Specifications	Value
1	Input Voltage, V_g	16 V
2	Output Voltage, V_0	12 V
3	Output Resistance, R	11 Ω
4	Inductance, L	1.1 mH
5	Inductor ESR, R_L	0.18 Ω
6	Capacitance, C	84 μF
7	Capacitor ESR, R_c	0.3 Ω
8	Switch Resistance, R_{sw}	0.044 Ω
9	Diode Resistance, R_d	0.024 Ω
10	Diode Forward Voltage, V_d	0.7 V
11	Duty Cycle, D	0.75
12	Switching Frequency, f_s	25 kHz

5. Mathematical Modeling of the Converters

The mathematical model can be obtained using the volt-sec and amp-sec balance equations, as shown in [7]. Figure 5 shows the results of mathematical modeling built and analyzed using Simulink for a non-ideal buck converter using appropriate step size and solver. As seen from Figure 5, the initial transient in output voltage and inductor current are 18 V and 3.6 A. Hence, while designing the capacitor and inductor, these values play a vital role. Equations (44) and (45) were used for modeling the converter.

$$L\frac{di_L}{dt} = s(V_g - i_L(R_{sw}+R_L)-V_0) + (1-s)*(-i_L(R_d+R_L+\frac{RR_c}{R+R_c})-V_d-\frac{RV_0}{R+R_c}) \quad (44)$$

$$C\frac{dv_0}{dt} = s(i_L(\frac{R}{R+R_c})-\frac{V_0}{R+R_c})+(1-s)*(i_L(\frac{R}{R+R_c})-\frac{V_0}{R+R_c}) \quad (45)$$

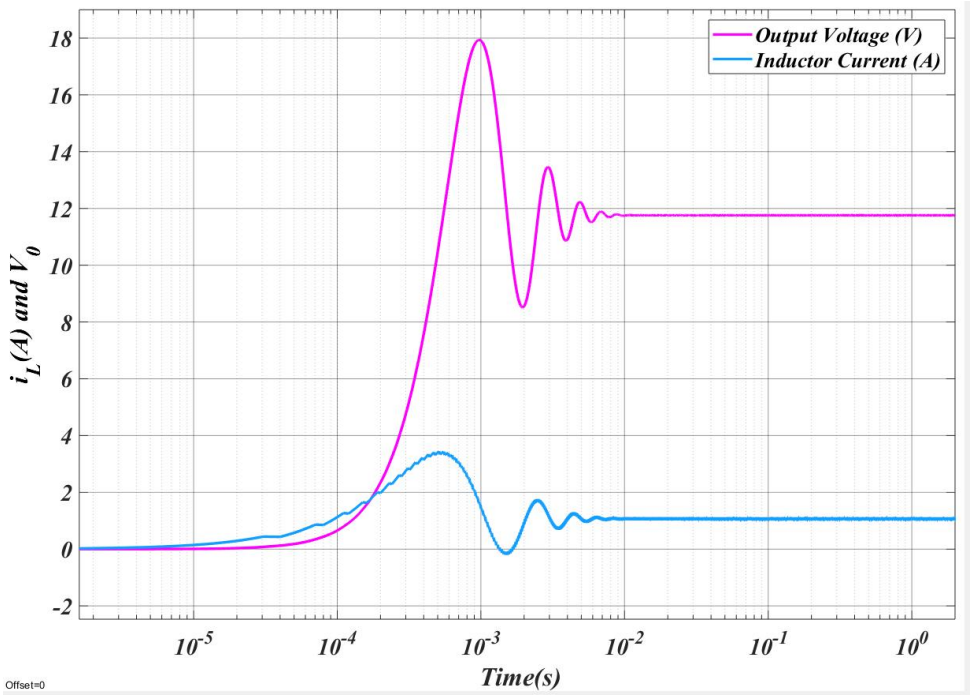

Figure 5. i_L and V_0 vs. time.

The modeling of the non-ideal synchronous buck converter is performed by making $V_d = 0$ and replacing R_d with $R_{sw2.}$ It is observed that the duty cycle of the synchronous converter is slightly smaller than that of the buck converter. This is mainly due to the lesser conduction loss in the MOSFET.

6. Results of ACC in Open Loop Configuration

Figure 6 shows the bode plot of the G_{id} for ideal and non-ideal buck converters operating in CCM. The plots were obtained using MATLAB software. It is observed that the ideal and the non-ideal converters are stable with the phase margin (PM) equal to 90.2° and 91.9°. It is observed that the ideal converter showed higher resonant frequency than the non-ideal converter. This is due to the presence of the ESRs of inductor and capacitor. Figure 7 shows the bode plot of the converters when $R_c = R_L = 0$. It is observed that the resonant frequency of the converters matched.

However, the non-ideal converter showed higher stability, which is due to the placement of poles closer to the left-hand side (LHS) of the s-plane. This is evident from the root locus plot shown in Figure 8. Equations (46) and (47) show the transfer functions of the G_{id} for ideal and non-ideal buck converters.

$$G_{id} = \frac{14545(s + 1082)}{s^2 + 1082s + 1.082 * 10^7} \tag{46}$$

$$G_{id} = \frac{15162(s + 1054)}{s^2 + 1518s + 1.074 * 10^7} \tag{47}$$

Figure 9 shows the bode plot of the G_{id} for ideal and non-ideal synchronous buck converters. It is observed that the ideal and the non-ideal converters are stable with the phase margin (PM) equal to 90.2° and 92°. As observed in Figure 7, the ideal converter showed higher resonant frequency than the non-ideal converter. This is due to the presence of ESRs in the inductor and the capacitor. Figure 10 shows the bode plot of the converters

when $R_c = R_L = 0$. Figure 11 shows the root locus of the converters. Equations (48) and (49) show the G_{id} for ideal and non-ideal synchronous buck converters.

$$G_{id} = \frac{14545(s + 1082)}{s^2 + 1082s + 1.082 * 10^7} \tag{48}$$

$$G_{id} = \frac{14545(s + 1054)}{s^2 + 1523s + 1.075 * 10^7} \tag{49}$$

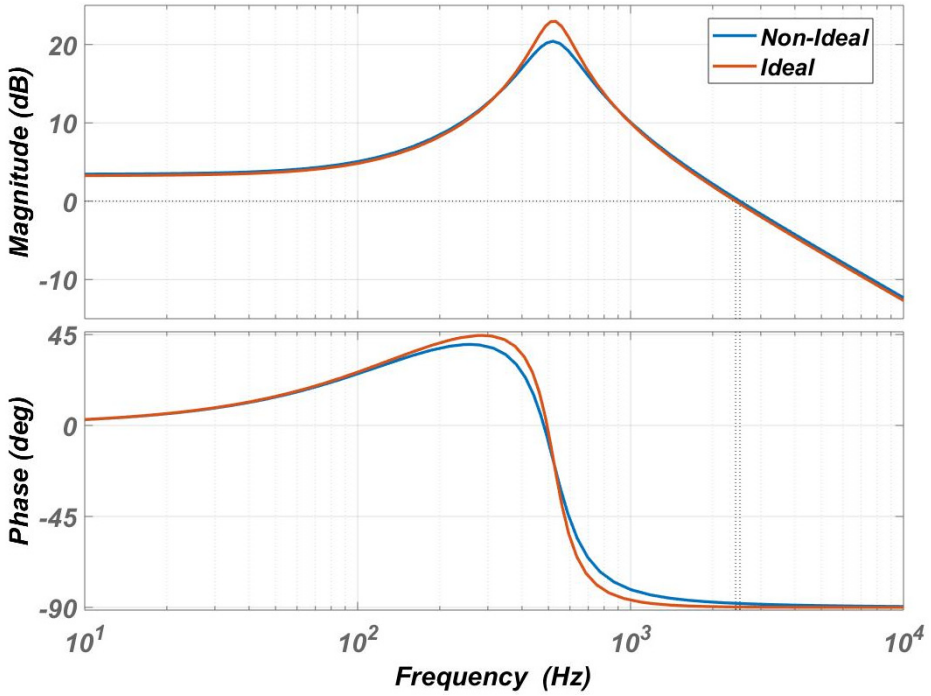

Figure 6. G_{id} for ideal and non-ideal buck converters.

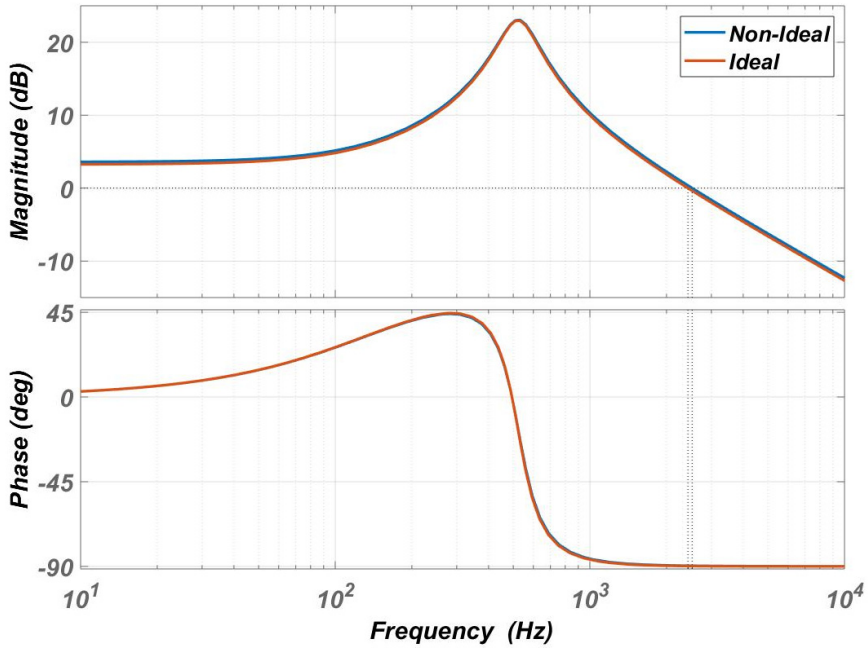

Figure 7. G_{id} for ideal and non-ideal buck converters for when $R_c = R_L = 0$.

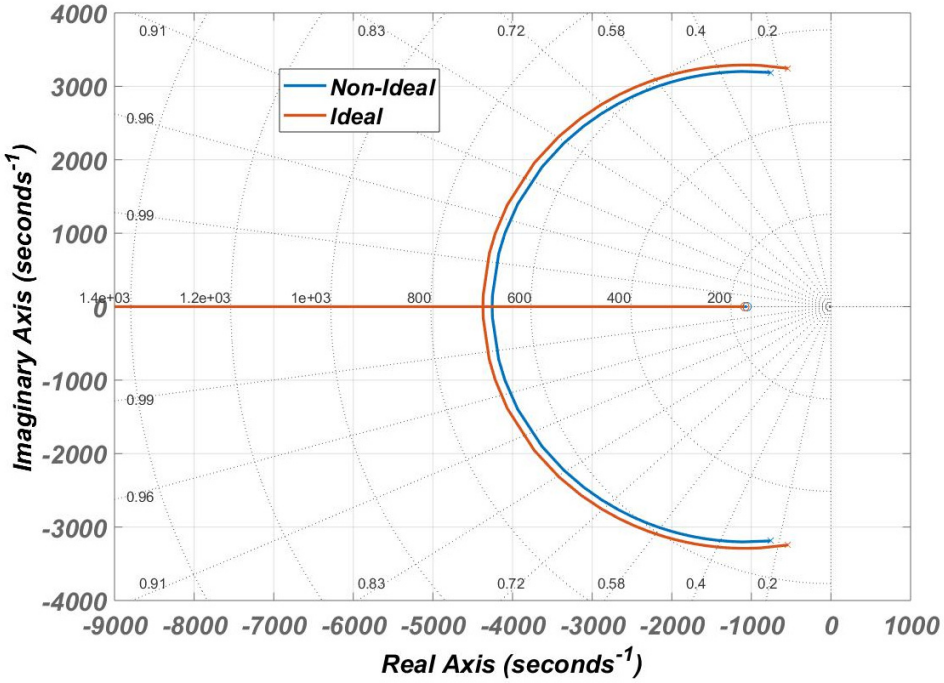

Figure 8. Root locus of G_{id} for ideal and non-ideal buck converters.

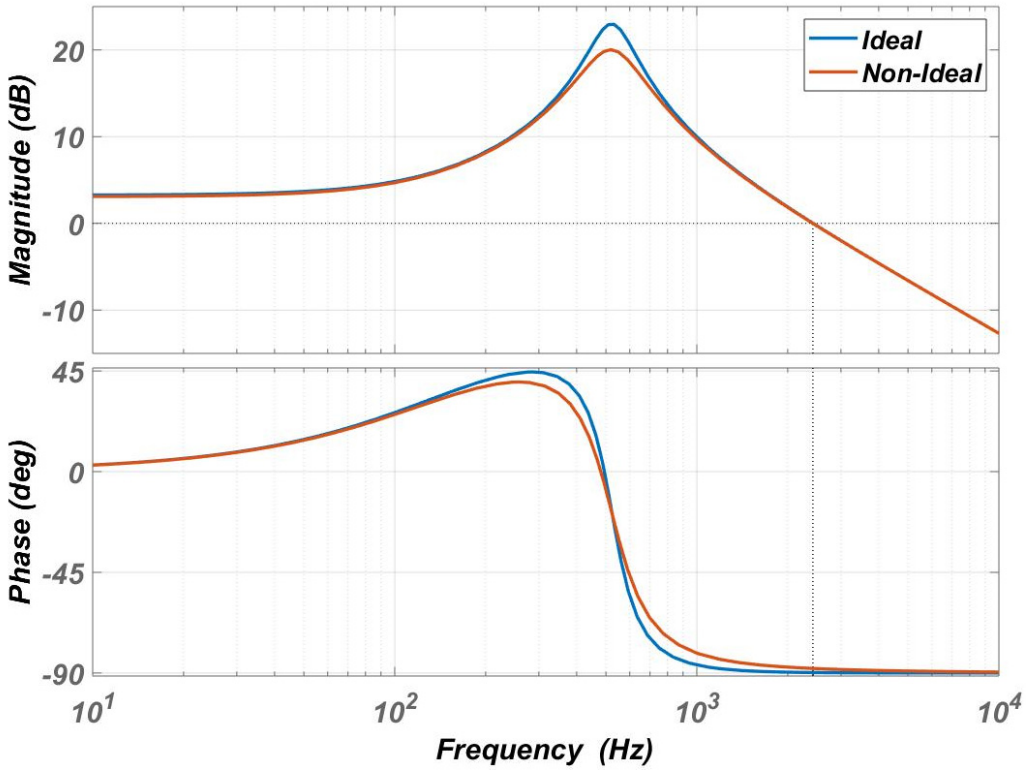

Figure 9. Bode plot of G_{id} for ideal and non-ideal synchronous buck converters.

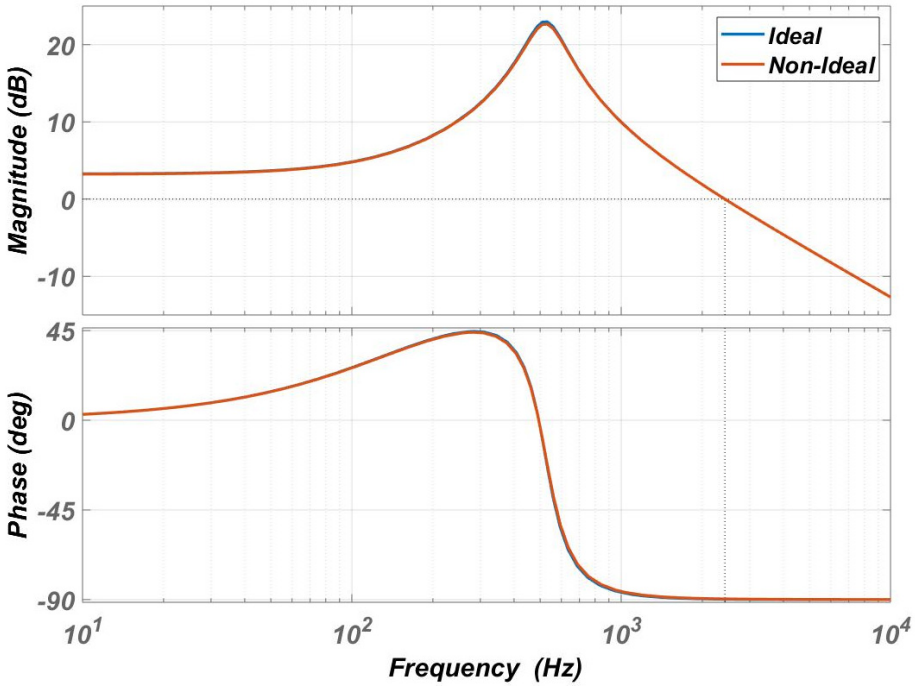

Figure 10. Bode plot of G_{id} for ideal and non-ideal synchronous buck converters for $R_c = R_L = 0$.

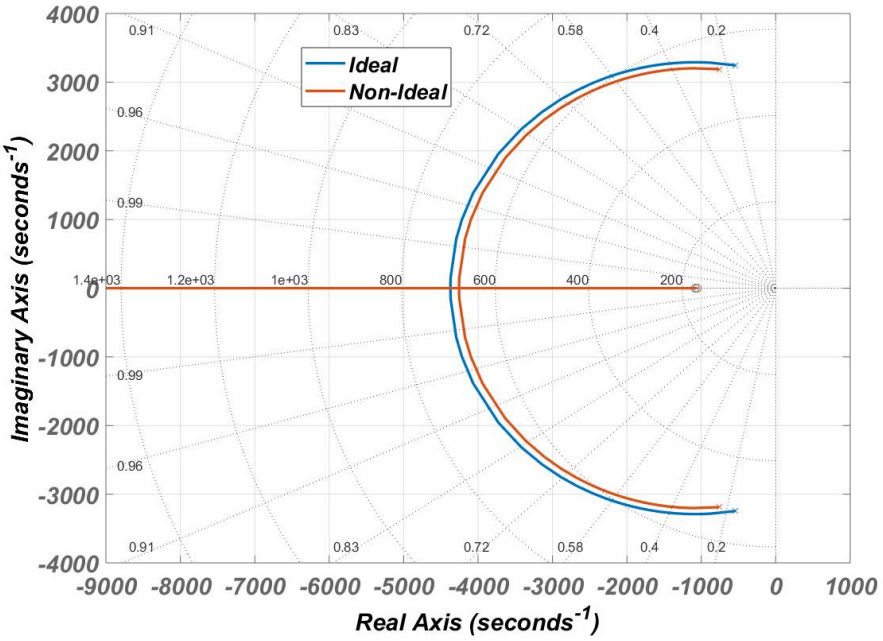

Figure 11. Root locus of G_{id} for ideal and non-ideal synchronous buck converters.

The bode plot of the G_{id} is analyzed for non-ideal buck and synchronous buck converters and is shown in Figure 12. The phase margins for the converters were 91.9° and 92°, respectively. It is observed from the frequency response of the converters that there is no change in the characteristics of the G_{id}. Hence, the placement of poles and zeros also remains the same. This is evident from Figure 13.

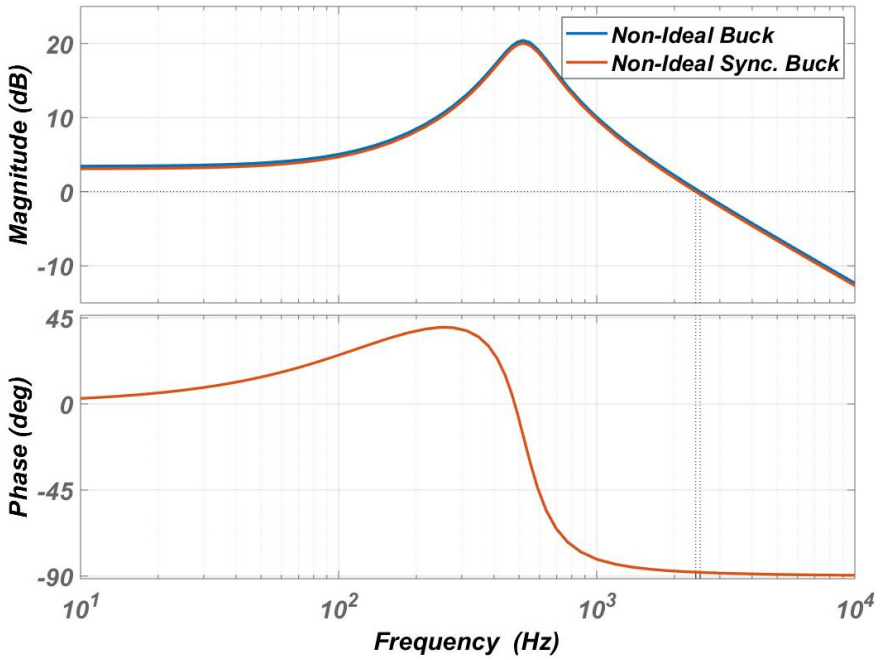

Figure 12. Bode plot for non-ideal buck and synchronous buck converters.

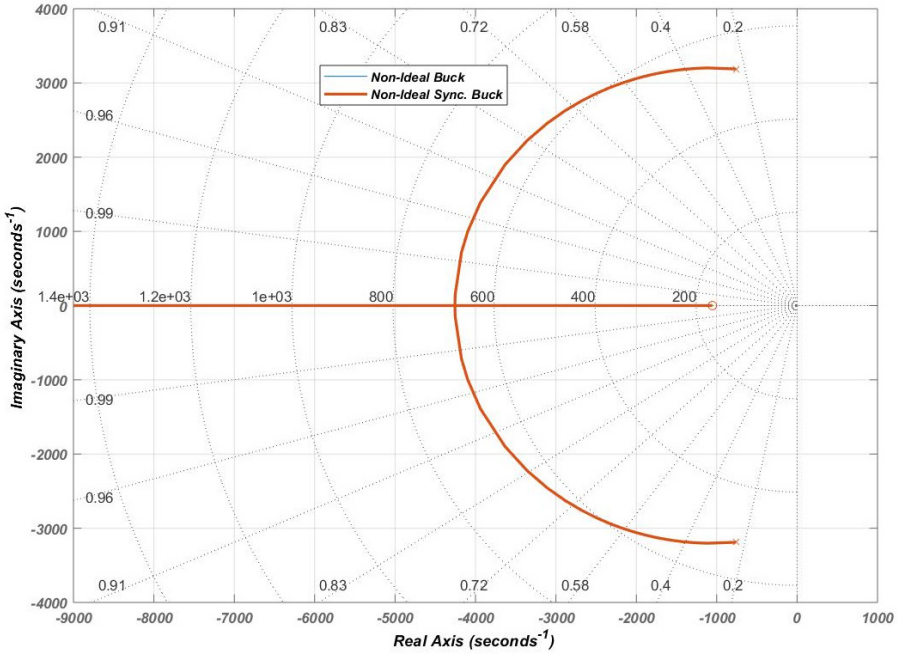

Figure 13. Root locus for non-ideal buck and synchronous buck converters.

7. Validation Using LTspice

The G_{id} derived using SSA was verified using standard switch models provided in the LTspice software tool. Figure 14 shows the average model of the non-ideal buck converter; the CCM2 library model was used for validation [16]. Figure 15 shows the frequency response of the G_{id} of the practical buck converter. It is observed that the low frequency gain, resonant frequency, and the cut-off frequency match with Figure 6.

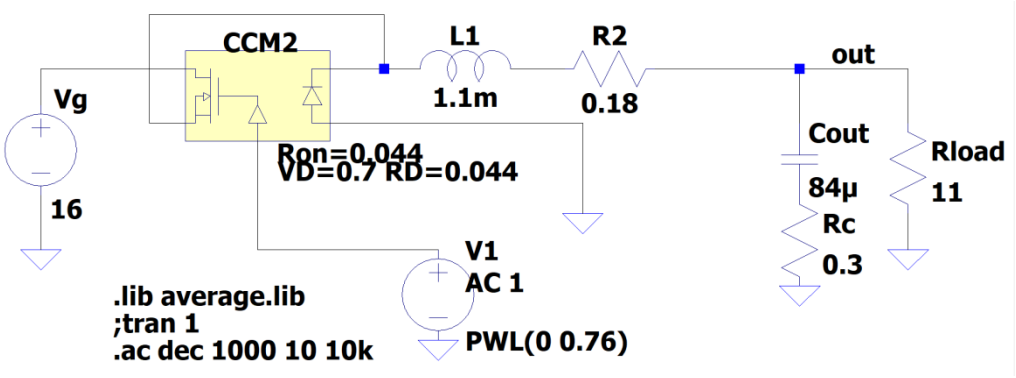

Figure 14. Averaged model of a practical buck converter.

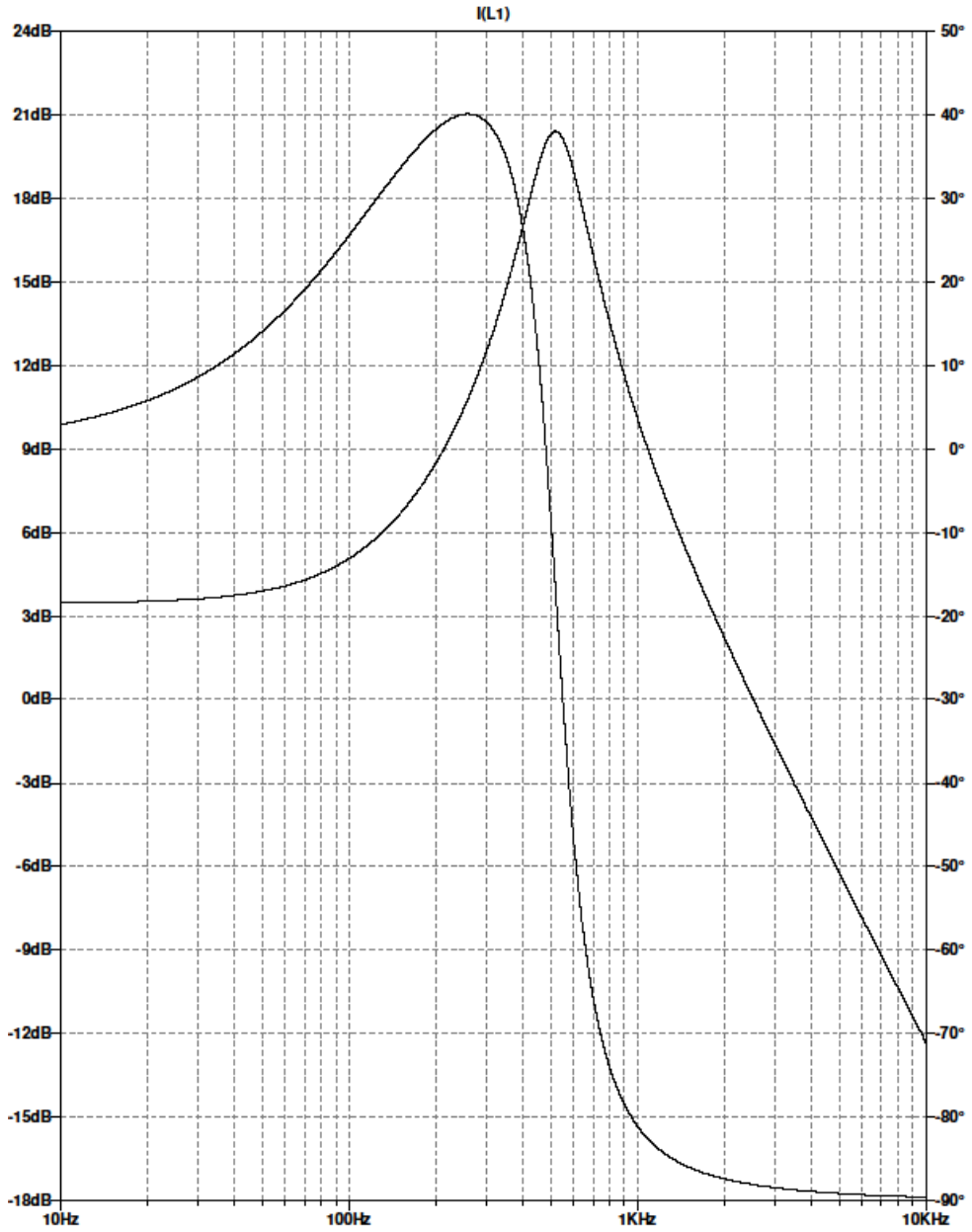

Figure 15. Bode plot of G_{id} for a non-ideal buck converter.

Figure 16 shows the bode plot of the non-ideal synchronous buck converter obtained using the average model. This perfectly matches with Figure 12.

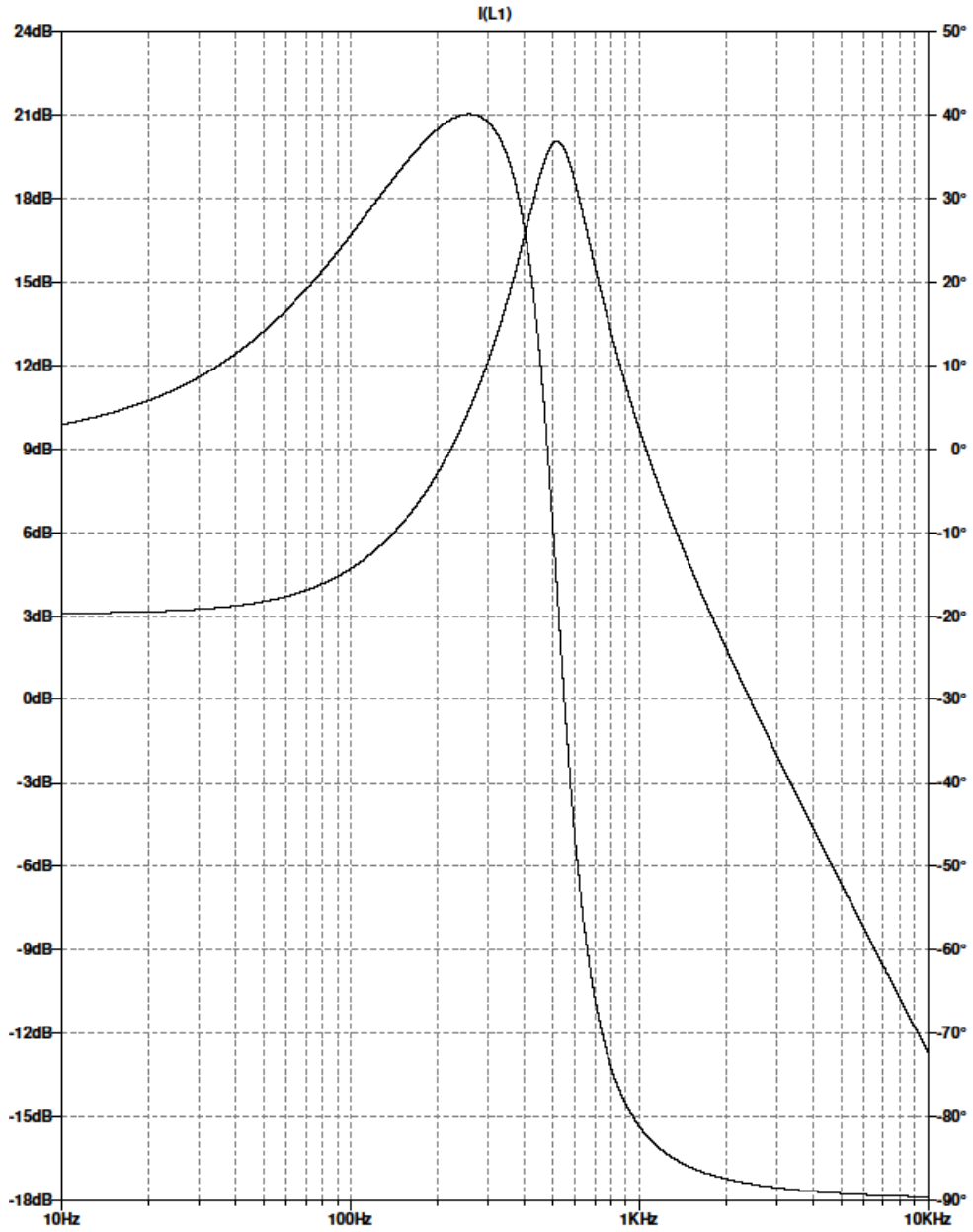

Figure 16. Frequency response of G_{id} for the practical synchronous buck converter using LTspice.

8. Conclusions

Low-power DC–DC converters are mainly used in mobile chargers and electric vehicle applications. In such converters, the voltage and current ripples are precise. In this paper:

- ACC modeling for ideal and non-ideal buck and synchronous buck converters operating in CCM is carried out from basic equations of volt-sec and amp-second balance equations for a single current loop.
- The converters were initially modeled using volt-sec and amp-sec balance equations. Using MATLAB/Simulink software, the mathematical model was analyzed and the transients in output voltage and inductor current were clearly seen.
- Later, using the state space averaging technique, the average current transfer function Gid was derived for the ideal and non-ideal converters.

- The ideal and non-ideal converters were highly stable. However, the ideal buck converter showed higher resonant frequency than the non-ideal converter. This is due to the presence of ESRs in the inductor and the capacitor. A similar phenomenon was observed in ideal and non-synchronous converters.
- The derived transfer function was validated against standard switch models using the LTspice software. The plots show a perfect match between the derived transfer function and the actual switch model.
- The ACC modeling with closed loop control is to be carried out for different converter CCM/DCM configurations with inner current and outer voltage loops, and the effect of the capacitor ESR in the closed loop configuration is to be analyzed. The input current and the voltage can be controlled in order to achieve a power factor close to unity.

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References

1. Middlebrook, R.D. Modeling current-programmed buck and boost regulators. *IEEE Trans. Power Electron.* **1989**, *4*, 36–52. [CrossRef]
2. Sun, C.; Lehman, B. Modeling of Average Current Mode Control in PWM DC/DC Converters. *IFAC Proc. Vol.* **1999**, *32*, 7421–7426. [CrossRef]
3. Erickson, R.W.; Maksimovic, D. *Fundamentals of Power Electronics*; Springer Science & Business Media: Berlin, Germany, 2007.
4. Sumukh, S.; Surpiya, P.; Williamson, S. A Comprehensive Study on DC–DC and DC–AC Converters in Electric and Hybrid Electric Vehicles. In *Accepted for Publication E-Mobility—A New Era in Automotive Technology*; Springer: Berlin/Heidelberg, Germany, 2021.
5. Sharifi, S.; Babaei, M.; Monfared, M. A high gain buck PFC synchronous rectifier. In Proceedings of the Electrical Engineering (ICEE), Iranian Conference on, Mashhad, Iran, 8–10 May 2018; IEEE: Piscataway, NJ, USA, 2018.
6. Channappanavar, R.; Mishra, S.K.; Singh, R.K. An inductor current estimator for digitally controlled synchronous buck converter. *IEEE Trans. Power Electron.* **2018**, *34*, 4883–4894. [CrossRef]
7. Surya, S.; Arjun, M.N. Mathematical Modeling of Power Electronic Converters. *SN Comput. Sci.* **2021**, *2*, 1–9. [CrossRef]
8. Surya, S.; Williamson, S. Generalized circuit averaging technique for two-switch PWM DC-DC converters in CCM. *Electronics* **2021**, *10*, 392. [CrossRef]
9. Chakraborty, S.; Hasan, M.M.; Worighi, I.; Hegazy, O.; Razzak, M.A. Performance evaluation of a PID-controlled synchronous buck converter based battery charging controller for solar-powered lighting system in a fishing trawler. *Energies* **2018**, *11*, 2722. [CrossRef]
10. Surya, S.; Channegowda, J.; Naraharisetti, K. Generalized Circuit Averaging Technique for Two Switch DC-DC Converters. In Proceedings of the 2020 8th International Conference on Power Electronics Systems and Applications (PESA), Hong Kong, China, 7–10 December 2020; IEEE: Piscataway, NJ, USA, 2020.
11. Garg, M.M.; Pathak, M.K. Performance comparison of non-ideal and ideal models of DC-DC Buck converter. In Proceedings of the 2018 8th IEEE India International Conference on Power Electronics (IICPE), Jaipur, India, 13–15 December 2018; IEEE: Piscataway, NJ, USA, 2018.
12. Surya, S.; Williamson, S. Modeling of Average Current in Ideal and Non-Ideal Boost and Synchronous Boost Converters. *Energies* **2021**, *14*, 5118. [CrossRef]
13. Chou, H.H.; Chen, H.L. A Novel Buck Converter with Constant Frequency Controlled Technique. *Energies* **2021**, *14*, 5911. [CrossRef]
14. Granda, M.; Fernandez, C.; Barrado, A.; Zumel, P. Nonparametric Frequency Response Identification for Dc-Dc Converters Based on Spectral Analysis with Automatic Determination of the Perturbation Amplitude. *Sensors* **2021**, *21*, 3234. [CrossRef] [PubMed]
15. Lin, B.-R.; Goh, A.P.I.; Wang, K.-W. Analysis of a Resonant Converter with Wide Input Voltage. *Electronics* **2021**, *10*, 1110. [CrossRef]
16. Tai, L.; Lin, M.; Wang, J.; Hou, C. Synchronous Control Strategy with Input Voltage Feedforward for a Four-Switch Buck-Boost Converter Used in a Variable-Speed PMSG Energy Storage System. *Electronics* **2021**, *10*, 2375. [CrossRef]
17. Cuoghi, S.; Mandrioli, R.; Ntogramatzidis, L.; Gabriele, G. Multileg Interleaved Buck Converter for EV Charging: Discrete-Time Model and Direct Control Design. *Energies* **2020**, *13*, 466. [CrossRef]

18. Xie, H.; Guo, E. How the Switching Frequency Affects the Performance of a Buck Converter. Available online: https://www.ti.com/lit/an/slvaed3/slvaed3.pdf?ts=1635120058978&ref_url=https%253A%252F%252Fwww.google.co.in%252F (accessed on 25 October 2021).
19. Available online: https://www.onsemi.cn/pub/collateral/tnd352-d.pdf (accessed on 25 October 2021).
20. Rahimi, B.A.M.; Parto, P.; Asadi, P. Compensator Design Procedure for Buck Converter with Voltage-Mode Error-Amplifier. Available online: https://www.infineon.com/dgdl/an-1162.pdf?fileId=5546d462533600a40153559a8e17111a (accessed on 25 October 2021).
21. Available online: https://www.ti.com/seclit/ml/slup341/slup341.pdf (accessed on 25 October 2021).
22. Priewasser, R.; Agostinelli, M.; Unterrieder, C.; Marsili, S.; Huemer, M. Modeling, control, and implementation of DC–DC converters for variable frequency operation. *IEEE Trans. Power Electron.* **2014**, *29*, 287–301. [CrossRef]
23. Lionel, F.D.J.; Dias, J.; Srinivasan, M.K.; Parandhaman, B.; Prabhakaran, P. A Novel Non-Isolated Dual-Input DC-DC Boost Converter for Hybrid Electric Vehicle Application. *Int. J. Emerg. Electr. Power Syst.* **2021**, *22*, 191–204.
24. Sreelakshmi, S.; Krishna, M.; Deepa, K. Bidirectional Converter Using Fuzzy for Battery Charging of Electric Vehicle. In Proceedings of the 2019 IEEE Transportation Electrification Conference (ITEC-India), Bengaluru, India, 17–19 December 2019.
25. Lionel, F.D.J.; Jayan, J.; Srinivasan, M.K.; Prabhakaran, P. DC-Link Current Based Position Estimation and Speed Sensorless Control of a BLDC Motor Used for Electric Vehicle Applications. *Int. J. Emerg. Electr. Power Syst.* **2021**, *22*, 269–284.
26. Surya, S.; Srinivasan, M.K.; Williamson, S. Technological Perspective of Cyber Secure Smart Inverters Used in Power Distribution System: State of the Art Review. *Appl. Sci.* **2021**, *11*, 8780. [CrossRef]
27. Surya, S.; Singh, D.B. Comparative study of P, PI, PD and PID controllers for operation of a pressure regulating valve in a blow-down wind tunnel. In Proceedings of the 2019 IEEE International Conference on Distributed Computing, VLSI, Electrical Circuits and Robotics (DISCOVER), Manipal, India, 11–12 August 2019.