



Article A 9-Bit 1-GS/s Hybrid-Domain Pseudo-Pipelined SAR ADC Based on Variable Gain VTC and Segmented TDC

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Abstract: This paper presents a 9-bit 1 GS/s successive approximation register (SAR) analog-todigital converter (ADC). In this hybrid architecture, the pseudo-pipeline operation is realized, which increases the sampling rate effectively. The ADC adopts two key technologies: the variable gain voltage-to-time converter (VTC), which ensures the linearity is not sacrificed; the segmented time-todigital converter (STDC), which further improves the linearity of time domain quantization. The prototype ADC is simulated in a standard 65-nm CMOS process with an active area of 0.038 mm². The simulated SNDR and SFDR are 44.3 and 58 dB with a sampling rate of 1 GS/s. The FoMW and FoMS are 24.7 fJ/conv-step and 150.7 dB, respectively.

Keywords: analog-to-digital converter (ADC); hybrid-domain quantization; high speed; voltage-to-time converter (VTC); time-to-digital converter (TDC)

1. Introduction

The higher data receiving rate in communication systems increases the demand for high-speed ADCs in recent years. SAR ADCs are popular because of the excellent power efficiency. To increase the sampling rate of SAR ADCs, time interleaving technique [1-4] is used by multiplexing several converters in parallel. As the fastest architecture, pipelined ADC is combined to further contribute to the conversion speed of time interleaving ADC [5]. However, the time interleaving multiplies power consumption and the area, the mismatch between channels magnifies dynamic errors as well. Compared with traditional SAR ADCs, time-domain quantization has better performance in terms of high-speed conversion, lowvoltage design, and reduction of mismatch. In terms of high-speed conversion, the SAR ADC needs to perform charge redistribution every time it completes 1 bit of quantization. In order to ensure that the voltage is fully established, it is generally necessary to reserve a sufficient conversion time. Especially when the number of quantization bits is high, the capacitance in the Digital-to-Analog Converter (DAC) will also increase exponentially, which limits the improvement of the conversion speed. In the time domain quantization, according to the working principle of TDC, each conversion cycle can complete multi-bit quantization. Compared with the single-bit quantization method based on the comparator, the number of charge redistribution is reduced, and the sampling rate is increased, accordingly. Analog-to-digital converters (ADCs) employing time-to-digital converters (TDCs) combined with traditional voltage-domain ADCs have recently been reported [6] to show reasonable power efficiency. Time-domain quantization [7–9] is suitable for the high-speed SAR ADCs design, because the delay cell is faster due to the process scaling, but the operation in voltage-domain and time-domain is performed in sequence, with the



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Copyright: © 2021 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (https:// creativecommons.org/licenses/by/ 4.0/). improvement in speed limited. There are three critical timings in a typical SAR ADCs: the comparator decision/resolving time, the CDAC settling time, and the digital logic delay [10,11]. The comparator decision/resolving time is a function of the input voltage, but the relationship is not utilized in most ADCs.

In this work, a two-stage SAR ADC is achieved by utilizing the voltage-domain and time-domain conversion and pseudo-pipelined operation. Different from the conventional hybrid quantization method, the signal is converted in voltage- and time-domain almost simultaneously, which increases the sampling rate obviously. In Section 2 the architecture and timing are introduced. Moreover, a variable gain voltage-to-time converter (VTC) and a segmented time-to-digital converter (STDC) are proposed in Section 3 to overcome the nonlinearity of the time-domain conversion. In Section 4 the simulation results are presented. Finally, the conclusion is given in Section 5.

2. Proposed ADC Architecture

2.1. Architecture

The proposed high-speed ADC architecture, as shown in Figure 1, comprises a voltage ADC (VADC), a time ADC (TADC), and a digital logic. The converter has a total of 9-bit output. The 2-MSB quantization is completed in the voltage-domain and the 7-LSB quantization is completed in the time domain. It is expected to achieve a sampling rate of 1 GS/s.



Figure 1. Architecture of the proposed two-stage ADC.

The voltage-domain component operation as a traditional 2-bit SAR ADC is used to quantify MSBs. The input signal uses a differential form to reduce common-mode noise and the even harmonics of the output and utilizes the capacitor's top plate to sample the input to increase the ADC conversion speed. In the time-domain component, the voltage residue is converted to a time-domain signal through the VTC, and the STDC is used to complete the LSBs quantization. The input of the comparator CMP₂ is connected to the upper plate of the capacitor in the VADC to compare the magnitude of the voltage residue at both ends of the differential. The output of the VADC is connected to the VTC through a transmission gate; an AND gate and an inverter are added to the next stage. The conversion results of the two time-domain signals are combined into one as the input of the STDC. After the voltage residue is converted into the corresponding time signal TR, a 7-LSB quantization result is produced under the action of the STDC. The thermometer-to-binary converter circuit (T-B) is used to convert the output of the STDC into binary and superimpose it with the sign bit, which produces the conversion result of the TADC.

2.2. Timing

The timing diagram of the proposed ADC is illustrated in Figure 2. During the sampling phase Φ_S , the input voltages are sampled into the DAC in VADC. When Φ_{C1} is high level, the sampling completed and the comparator CMP₁ converts the MSBs. The comparator operates twice, and the quantization of the voltage-domain is completed. Before the next convert cycle, the voltage residue is generated by the CDAC and transferred to the TADC while Φ_T is low; the transmission gate in the VTC is turned off. Meanwhile, Φ_{C2} goes high; the comparator CMP₂ discriminates the polarity of the voltage residue and generates a sign bit; the conversion result *TR* is outputted by VTC under the control of Φ_{VTC} . The rising edge interval of Φ_{VTC} and *TR* is the inputs of the STDC. Utilizing a phase interpolation circuit, the 4-bit time signal *RI* [3:0] is extended by *TR* and the interval between adjacent RI signals is equal to one-fourth of the unit delay td of TDC. Consequently, the TADC completes the 7-bit quantization expeditiously.



Figure 2. Timing diagram of the proposed two-stage ADC.

Since the negative edge of the clock Φ_T is slightly earlier than the positive edge of the sampling clock Φ_S , the connection between VTC and VADC was disconnected before the next sampling cycle. The last conversion residue is not affected by the new input voltage. Therefore, the TADC converts the previous residue in time-domain, and the VADC samples the next voltage input signal and determines the MSBs.

The pseudo-pipeline operation is realized. The voltage-domain and the time-domain quantization are carried out almost at the same time, and the two-stage conversion process is completed in only one clock cycle, which improves the sampling rate of the ADC effectively.

3. Circuit Implementation

3.1. Capacitive DAC

A 2-bit capacitive DAC samples input voltage and generates voltage residue. The circuit architecture of the capacitive DAC is shown in Figure 3. The load of the DAC in the conventional SAR ADC is a comparator. However, the DAC in the VADC is connected to the VTC and the comparator CMP₂; an additional parasitic capacitor is generated between the top plate and the ground. The parasitic capacitor is equivalent to increasing the dummy capacitance C_{DM} . According to the principle of charge redistribution, if there is an error in the dummy capacitor, the voltage of the top plate will change incorrectly, and the voltage residue is affected. To reduce the error, this paper divides the C_{DM} into two parts: one is a capacitor of 3C, and its bottom plate is always connected to the common mode voltage; the other contains 4 MOS capacitors with digital adjustment, the capacitance value ratio is

1:2:4:8. The capacitance of the C_{DM} can be adjusted by changing the 4-bit control signal D_{CAL} [3:0] to ensure that the C_{DM} is near 4*C*.



Figure 3. Capacitive DAC.

3.2. Voltage-to-Time Converter (VTC)

The VTC builds the interface between the voltage-domain and time-domain conversions. The circuit structure of the traditional voltage type VTC is shown in Figure 4a. The input voltage is directly connected to the output node through the switch. In the sampling phase, the voltage input $V_{\rm IP}$ and $V_{\rm IN}$ are collected into the parasitic capacitance $C_{\rm P}$. During the conversion phase, the top switch is turned off, and M₁-M₄ are turned on. Since the gate voltages of M₁ and M₂ are provided by the DC bias $V_{\rm b}$, both ends will discharge $C_{\rm P}$ with the same current $I_{\rm C}$. As shown in Figure 4b, different input voltages change the initial point of the discharge. After the voltage drops to $V_{\rm IL}$, TDC is triggered and the conversion from voltage to time is completed. The proposed structure is based on the voltage type VTC, and the operation principle is shown in Figure 5a,b. When $\Phi_{\rm T}$ is low, VTC collects the voltage residue, the output $V_{\rm P}$ and $V_{\rm N}$ of the VADC are transmitted to the nodes $V_{\rm RP}$ and $V_{\rm RN}$ through the source followers to pre-charge the dummy capacitor. When $\Phi_{\rm T}$ is high, the VTC converts the voltage residue and CMOS switch M₅-M₈ are turned off. Voltage $V_{\rm RP}$ and $V_{\rm RN}$ decrease at a constant rate of discharge current provided by M₉ and M₁₀. The relationship between time and output voltage $V_{\rm OP}$ can be expressed as:

$$V_{\rm OP} = VDD - \frac{K(V_{\rm CAL} - V_{\rm TH})^2}{C_{\rm P}} \cdot (1 + \lambda V_{\rm OP})t \tag{1}$$

Here $K = \frac{1}{2}\mu_n C_{\text{ox}}W/L$, assuming $K_{\text{VTC}} = \frac{K(V_{\text{CAL}} - V_{\text{TH}})^2}{C_{\text{P}}}$, then $V_{\text{OP}} = VDD - K_{\text{VTC}}$ (1 + λV_{OP})*t*, the relationship between the output time and the input voltage is expressed as:

$$T_{\text{out}} = \frac{VDD - V_{\text{IL}}}{K_{\text{VTC}}(1 + \lambda V_{\text{IL}})} + \frac{1}{\lambda K_{\text{VTC}}} - \frac{\lambda VDD + 1}{\lambda^2 K_{\text{VTC}} \left(V_{P0} + \frac{1}{\lambda}\right)}$$
(2)

where V_{IL} is the triggered voltage of the inverter, and V_{P0} is the input voltage. A wider output range of VTC is desired to reduce the requirement for TDC. M₁₁ and M_{CAL} are utilized as voltage dividers to reduce the gate voltage V_{CAL} of M₉ and M₁₀, thereby reduce the discharge current and extend the output time range. M_{CAL} contains three parallel transistors, by switching the 3-b codes Cal [2:0], V_{CAL} and charging current are changed. The linearity of VTC will be severely affected by PVT, e.g., V_{TH} , μ_n . It can be seen from the above formula that V_{TH} , μ_n are included in K_{VTC} , so the influence of PVT on the conversion characteristics of VTC can be eliminated by changing V_{CAL} .



Figure 4. (a) VTC circuit based on variable voltage. (b)operation principle.





Figure 5. (a) Design of the proposed VTC and (b) timing diagram.

3.3. 6-Bit TDC

Due to the secondary effect of the circuit, the output of VTC is nonlinear. As shown in Figure 6b, the slope of the conversion characteristic curve decreases as the voltage rises. In order to reduce the impact of VTC nonlinearity, the conversion from the time-domain to the digital code based on the segment delay line TDC is proposed. The main principle is to split the delay line into two parts, each part has a different delay and resolution to create a nonlinear TDC artificially. If the nonlinearity of VTC and TDC can compensate each other, the linearity of the digital output will be improved. The shaded area between the VTC and TDC characteristic curves means the nonlinear error.



Figure 6. (**a**) Segment TDC. (**b**) Conversion characteristic of the VTC. (**c**) circuit of the phase interpolation.

With the segmented TDC, the total error area is significantly reduced. The delay line circuit of the segmented TDC is shown in Figure 6a. The delay line is divided into two parts; each part contains 8 delay units, and the delays are 14 ps and 12.5 ps, respectively. The overall delay is only 212 ps. It adopts a 4 times phase interpolation structure, the output of each delay line is connected with the input terminals of 4 D-flip-flops, and the clock terminal of D flip-flop is connected with the output of the phase interpolation circuit. Because of the differences in the delays, two-phase interpolation circuits are needed to generate different time intervals, as shown in Figure 6c. The lower 4 bits of RI are generated by the first phase interpolation circuit PI₁ (the maximum time difference is 14 ps), which is connected to the clock terminal of the first half of the TDC; the upper 4 bits of RI are generated by the second phase interpolation circuit in the second half of the TDC. Using this phase interpolation technology, the resolution and conversion speed of the TDC can be improved, and the linearity of time-domain quantization is optimized.

4. Experimental Results

Figure 7 show the ADC layout in a standard 1P9M 65-nm TSMC with an active area of 0.038 mm². The simulated total power consumption of the ADC is 3.277 mW with a 1-V supply. The power consumption breakdown is shown in Figure 8. It can be broken down as follows: the bootstraps use 9% of the power; the VADC and the VTC uses 36%; the digital circuits use 4%; and the TDC use 51%.



Figure 7. Layout of the proposed ADC.





Figure 9 illustrates the simulated spectrum with a conversion rate of 1-GS/s and an input frequency of 163 MHz. The simulated signal-to-noise-and-distortion ratio (SNDR) is 44.3 dB. The static performance of the DNL and INL by post-layout are +1.2/-1.0 and +2.79/-2.89 LSB, respectively, as shown in Figure 10. The error is mainly caused by the nonlinearity of the TADC. The parasitic capacitance of the post-layout affects the conversion gain of the VTC and the unit delay of the TDC, resulting in time-domain quantization errors and missing codes in TDC errors. Although the segmented TDC can compensate for the conversion characteristics of the VTC to a certain extent, it is still unable to eliminate its nonlinear error.

When the sampling rate input F_{IN} is changed from 90 MHz to 390 MHz, the postsimulated SNDR is maintained above 43.8 dB, as shown in Figure 11. The ADC attains a FoM of 24.3 fJ/conv-step at Nyquist rate. Table 1 summarizes the ADC performance and shows the comparison with the recently published GS/s ADCs.



Figure 9. Power spectral density of the proposed ADC.



Figure 10. Post-simulated DNL and INL.



Figure 11. Post-simulated SNDR versus input frequency.

				This Work Simulated
	ISSCC17 [2] Measured	A-SSCC18 [3] Measured	ISCAS18 [5] Simulated	
Туре	TI-SAR	TI-pip-SAR	Pip-SAR	SAR-TDC
CMOS (nm)	65	65	28	65
Active Area (mm ²)	1.7	0.128	0.175	0.038
Supply Voltage (V)	1.2	1.2/2.5	1	1
Power (mW)	44.6	22	16.02	3.277
Sampling Rate (GS/s)	2.8	1	0.8	1
SNDR (dB)	48.2	54.3	60.9	44.3
FoMwalden[fJ/c-s]	75.8	43.7	22.5	24.3

 Table 1. Performance Summary.

5. Conclusions

This paper presents a 9-bit 1-GS/s, single-channel, hybrid, voltage-time, pseudopipelined ADC in a 65-nm CMOS technology. The new hybrid ADC combines the high accuracy of the voltage-domain quantification and the high speed of the time-domain quantification to satisfy the need for high-speed ADCs, reducing the accuracy requirements of the comparator, converting the voltage signal into a time signal, and performing lowbit quantization in the time domain. A variable gain VTC, and segmented delay line TDC based on phase interpolation technique were proposed. The matching and linear conversion between VTC and TDC are guaranteed, and the quantization of the 6-LSB of the time domain only uses 212 ps resulting in an efficient operation. Using a 1-V supply, the prototype ADC dissipates a total power of 3.277 mW and achieves the Nyquist ENOB of 7.07 bits. The Nyquist FOM is 24.3 fJ/conversion-step. This paper shows that the proposed ADC is a good candidate for the implementation of high-speed and high-resolution ADCs.

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